CO503: Practical 1 - System-on-Chip (SoC) Design
Group 4: E/18/077, E/18/397

Part 1: First SoC - LED Counter

The work we have done:

- Created a simple SoC which can display an increasing count on a set of 8 LEDs
- Edited the counter.c file with the base address of led_out PIO device from QSYS

What we have learnt:

- How to use Quartus II application to program the FPGA
- Create design files using BDF
- How to use QSYS tool
- Pin mapping using the pin planner
- How to use Nios II software build tools
- Develop codes to run in the FPGA
- We had to install the drivers for the FPGA manually

➔ The Nios II processor variants (e, s and f),

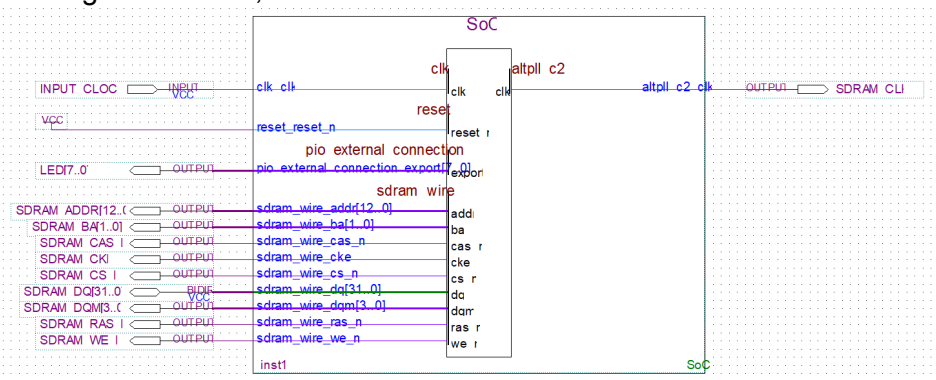
- Nios II/e (economy): Cost-effective, with a reduced instruction set and simpler Memory Management Unit (MMU).
- Nios II/s (standard): Balanced performance and cost, standard instruction set, hardware multiply/divide, and advanced MMU.
- Nios II/f (fast): High performance, full-featured instruction set, advanced instructions (e.g., floating-point), sophisticated MMU, and hardware accelerators.

➔ What do you think the statement IOWR_8DIRECT(LED_BASE,OFFSET,count); does?
It writes the value of "count" to the "led_out" PIO device. (Address given by adding LED_BASE and the OFFSET value.)

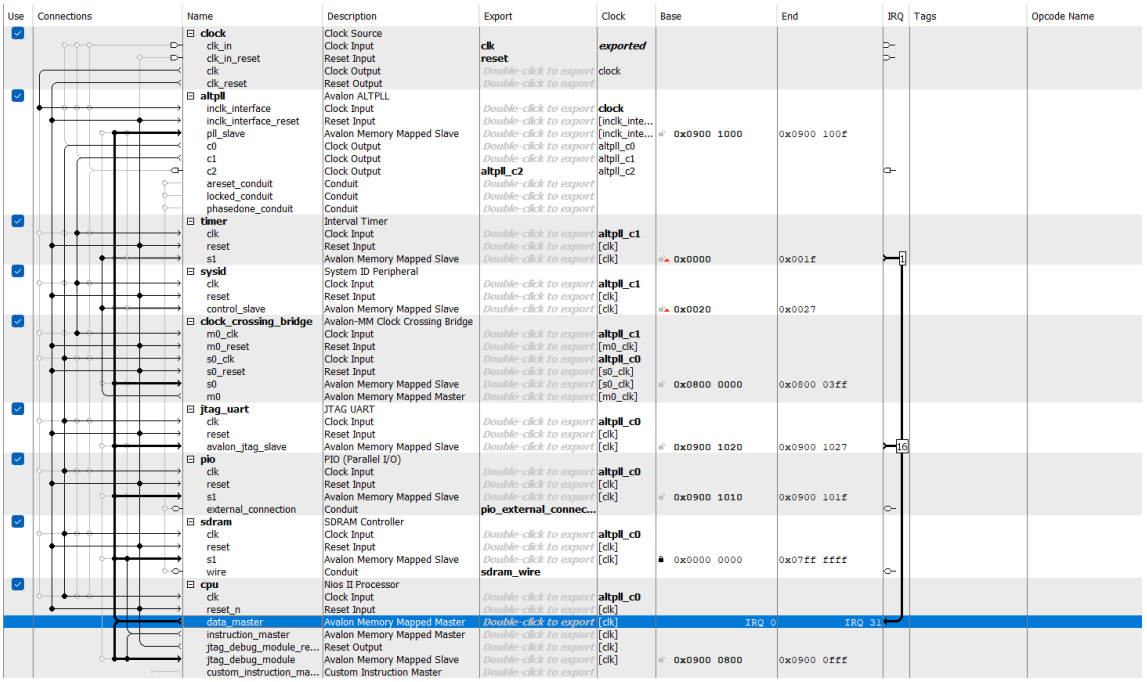
Part 2: JPEG Encoder

The work we have done:

- Created a SoC for JPEG image encoding, using onboard SDRAM of the FPGA as the main memory
- Hardware and software configurations were done according to the lab sheet using Quartus II
- Block diagram created,



- Hardware design created using QSYS,



What we have learnt:

- Use of different clocks,
  - 10MHz Clock for Timer and SysID:
    - Timer uses a slow clock for timing accuracy
    - SysID uses it for stable setup
  - 100MHz Clock for Other SoC Components:
    - Faster clock for processors and devices, making data handling quicker
  - 100MHz Clock with -65 Degree Phase Shift for DRAM Chip:
    - The external DRAM clock is delayed compared to the internal clock due to propagation delays. To fix this, a -65 degree phase shift is introduced to the original clock signal for the DRAM, ensuring proper synchronization and reliable data transfer.

- Below table shows the results of our SoC.

Image Name	Time took for encoding and write back process (in Seconds)	Size of bmp (in kB)	Size of jpg (in kB)
image0.bmp	88	129	31
image1.bmp	254	769	76
image2.bmp	90	193	13
image3.bmp	78	193	13
image4.bmp	43	49	10
image5.bmp	48	49	6
image6.bmp	241	769	80

Table 01: Timings for provided images

This highlights, larger image sizes result in longer processing times and efficiency of JPG format in terms of storage space compared to BMP format.