Lab 9-10 – Nanoprocessor Design Competition

CS1050 Computer Organization and Digital Design

Group 38

- Group Members Names and Index Numbers:

  - Hana A.N.F – 210203M
  - Jayathilake.N.C – 210257F

Lab Task

- ✓ Design a simplified nano processor capable of executing the following assembly instructions:

  - ADD: Add the value in register B to register A.
  - MOV: Move a specific value into register A.
  - NEG: Compute the 2's complement of the value in register R.
  - JZR: Jump to the instruction located at the address in register A if the value in register B is zero.

- ✓ Build the nano processor using the following components:

  - 4-bit Add/Subtract Unit
  - 3-bit Adder
  - 3-bit Program Counter (PC)
  - k-way b-bit Multiplexers
  - Register Bank
  - Program ROM
  - Buses
  - Instruction Decoder

- ✓ Write an assembly program to calculate the sum of numbers 1 to 3.

- ✓ Simulate the addition of 1, 2, and 3 and store the result in register R7 (the 8th register).

- ✓ Test the nano processor's functionality on the BASYS 3 platform.

- ✓ Demonstrate the circuit to the instructor.

Assembly program and Machine code representation

Adding 1 to 3

Assembly program	Machine code
MOV R7 0	"101110000000",
MOV R1 1	"100010000001",
MOV R2 2	"100100000010",
MOV R3 3	"100110000011",
ADD R7 R1	"001110010000",
ADD R7 R2	"001110100000",
ADD R7 R3	"001110110000",
JZR R0 7	"110000000111"

Arithmetic Operations and Conditional Jumps

Assembly program	Machine code
MOV R1 3	"100010000011"
MOV R2 1	"100100000001"
NEG R2	"010100000000"
ADD R7 R1	"001110010000"
ADD R1 R2	"000010100000"
JZR R1 7	"110010000111"
JZR R0 3	"110000000011"
JZR R0 7	"110000000111"

VHDL Codes

Nano processor

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
   Port ( Clk : in STD_LOGIC;
          Res : in STD_LOGIC;
          C : out STD_LOGIC:='0';
          Z : out STD_LOGIC;
          R7_out : out STD_LOGIC_VECTOR (3 downto 0);
          S7_seg : out STD_LOGIC_VECTOR (6 downto 0);
          Anode : out STD_LOGIC_VECTOR (3 downto 0));
end Nano;

architecture Behavioral of Nano is
   component Way2_4bit_MUX
      Port ( A : in STD_LOGIC_VECTOR (3 downto 0);--LS=0; D = A
             B : in STD_LOGIC_VECTOR (3 downto 0);
             LS : in STD_LOGIC;
             D : out STD_LOGIC_VECTOR (3 downto 0));
   end component;

   component Register_Bank
      Port ( Clk : in STD_LOGIC;
             Res : in STD_LOGIC;
             Reg_In : in STD_LOGIC_VECTOR (3 downto 0);
             En : in STD_LOGIC_VECTOR (2 downto 0);
             R0 : out STD_LOGIC_VECTOR (3 downto 0);
             R1 : out STD_LOGIC_VECTOR (3 downto 0);
             R2 : out STD_LOGIC_VECTOR (3 downto 0);
             R3 : out STD_LOGIC_VECTOR (3 downto 0);
             R4 : out STD_LOGIC_VECTOR (3 downto 0);
             R5 : out STD_LOGIC_VECTOR (3 downto 0);
             R6 : out STD_LOGIC_VECTOR (3 downto 0);
             R7 : out STD_LOGIC_VECTOR (3 downto 0));
   end component;

   component Adder_Subtractor_2
      Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
             B : in STD_LOGIC_VECTOR (3 downto 0);
             C_in : in STD_LOGIC;
             C_out : out STD_LOGIC;
             S : out STD_LOGIC_VECTOR (3 downto 0);
```

```
        Zero : out STD_LOGIC);
end component;

component  Way8_4_MUX
   Port ( D0 : in STD_LOGIC_VECTOR (3 downto 0);
          D1 : in STD_LOGIC_VECTOR (3 downto 0);
          D2 : in STD_LOGIC_VECTOR (3 downto 0);
          D3 : in STD_LOGIC_VECTOR (3 downto 0);
          D4 : in STD_LOGIC_VECTOR (3 downto 0);
          D5 : in STD_LOGIC_VECTOR (3 downto 0);
          D6 : in STD_LOGIC_VECTOR (3 downto 0);
          D7 : in STD_LOGIC_VECTOR (3 downto 0);
          S : in STD_LOGIC_VECTOR (2 downto 0);
          Y : out STD_LOGIC_VECTOR (3 downto 0));
end component;

component RCA_3
   Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
         --B : in STD_LOGIC_VECTOR (2 downto 0);
          S : out STD_LOGIC_VECTOR (2 downto 0);
          C_in : in STD_LOGIC;
          C_out : out STD_LOGIC);
end component;

component Way2_3_Mux
   Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
          B : in STD_LOGIC_VECTOR (2 downto 0);
          JF : in STD_LOGIC;
          To_PC : out STD_LOGIC_VECTOR (2 downto 0));

end component;

component LUT_16_7
  Port ( address : in STD_LOGIC_VECTOR (3 downto 0);
         data : out STD_LOGIC_VECTOR (6 downto 0));
end component;

component Program_Counter
   Port ( Input : in STD_LOGIC_VECTOR (2 downto 0):= "000";
          Output : out STD_LOGIC_VECTOR (2 downto 0);
          Clk : in STD_LOGIC;
          Reset : in STD_LOGIC);
end component;
```

```
    component Instruction_Decoder
        Port ( Ins : in STD_LOGIC_VECTOR (11 downto 0);
               Reg_Chk : in STD_LOGIC_VECTOR (3 downto 0);
               AS_S : out STD_LOGIC;
               LS : out STD_LOGIC;
               Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
               Reg_S1 : out STD_LOGIC_VECTOR (2 downto 0);
               Reg_S2 : out STD_LOGIC_VECTOR (2 downto 0);
               JF : out STD_LOGIC;
               J_AD : out STD_LOGIC_VECTOR (2 downto 0);
               Im_Val : out STD_LOGIC_VECTOR (3 downto 0));
    end component;

    component ROM
        Port ( PC : in STD_LOGIC_VECTOR (2 downto 0);
               Ins : out STD_LOGIC_VECTOR (11 downto 0));
    end component;

    component Slow_Clk
        Port ( Clk_in : in STD_LOGIC;
               Clk_out : out STD_LOGIC);
    end component;


    signal  Clk_slow, Load_S, AS_S, J_F : std_logic;
    signal AS_out, I_val, Reg_in, R0, R1, R2, R3, R4, R5, R6, R7, Y1, Y2 :
    std_logic_vector (3 downto 0);
    signal Reg_En, Reg_S1, Reg_S2, MUX2_3_in, J_Ad, PC_in, PC_out : std_logic_vector
        (2 downto 0);--removed Q
    signal I_Bus: std_logic_vector (11 downto 0);

begin
Way2_4bit_MUX_0:Way2_4bit_MUX
      Port map( A => AS_out,
                B => I_val,
                LS => Load_S,
                D => Reg_in);

Reg_Bank : Register_Bank
       port map(Clk => Clk_slow,
                Res => Res,
                Reg_In => Reg_in,
                En => Reg_En,
                R0 => R0,
```

```
            R1 => R1,
            R2 => R2,
            R3 => R3,
            R4 => R4,
            R5 => R5,
            R6 => R6,
            R7 =>R7);

AS_Unit:  Adder_Subtractor_2
        Port map ( A => Y1,
             B =>Y2,
             C_in => AS_S,
             C_out => C,
             S => AS_out,
             Zero => Z);

Way8_4_MUX_0:Way8_4_MUX
       Port map ( D0 => R0,
            D1 => R1,
            D2 => R2,
            D3 => R3,
            D4 => R4,
            D5 => R5,
            D6 => R6,
            D7 => R7,
            S => Reg_S1,
            Y => Y1);


Way8_4_MUX_1:Way8_4_MUX
       Port map ( D0 => R0,
            D1 => R1,
            D2 => R2,
            D3 => R3,
            D4 => R4,
            D5 => R5,
            D6 => R6,
            D7 => R7,
            S => Reg_S2,
            Y => Y2);

RCA_3_0 : RCA_3
        Port map( A => PC_out,
           S =>MUX2_3_in,
```

```
            C_in =>'0');


Way2_3_Mux_0: Way2_3_Mux
  Port map(A => J_Ad,
           B => MUX2_3_in,
           JF =>J_F,
           To_PC => PC_in);

LUT_16_7_0 : LUT_16_7
    Port map (
        address => R7,
        data=> S7_seg);

PC : Program_Counter
    Port map (
       Input =>PC_in,
       Output => PC_out,
       Clk => CLk_slow,
       Reset => Res);

I_Decoder: Instruction_Decoder
        Port map
        ( Ins => I_Bus,
          Reg_Chk => Y1,
          AS_S =>AS_S,
          LS =>Load_S,
          Reg_EN => Reg_En,
          Reg_S1 =>Reg_S1,
          Reg_S2=> Reg_S2,
          JF => J_F,
          J_AD => J_Ad,
          Im_Val => I_val);

ROM_0 : ROM
    POrt map(
       PC => PC_out,
       Ins => I_Bus);

S_clk: Slow_Clk
    Port map
    ( Clk_in => Clk,
      Clk_out => Clk_slow);
```

```
R7_out <=R7;
Anode <="1110";

end Behavioral;
```

2 way 4-but MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Way2_4bit_MUX is
   Port ( A : in STD_LOGIC_VECTOR (3 downto 0);--LS=0; D = A
          B : in STD_LOGIC_VECTOR (3 downto 0);
          LS : in STD_LOGIC;
          D : out STD_LOGIC_VECTOR (3 downto 0));
end Way2_4bit_MUX;

architecture Behavioral of Way2_4bit_MUX is
   component MUX_2to1
   Port ( MUX2_1_In : in STD_LOGIC_VECTOR (1 downto 0);
          EN : in STD_LOGIC;
          MUX2_1_Out : out STD_LOGIC);
   end component;

begin

   MUX_2_to_1_0: MUX_2to1
      PORT MAP(
         MUX2_1_In(0)=>A(0),
         MUX2_1_In(1)=>B(0),
         MUX2_1_Out=>D(0),
         EN=> LS
         );

   MUX_2_to_1_1: MUX_2to1
      PORT MAP(
         MUX2_1_In(0)=>A(1),
         MUX2_1_In(1)=>B(1),
         MUX2_1_Out=>D(1),
         EN=> LS
         );
   MUX_2_to_1_2: MUX_2to1
      PORT MAP(
         MUX2_1_In(0)=>A(2),
         MUX2_1_In(1)=>B(2),
```

```
        MUX2_1_Out=>D(2),
        EN=> LS
        );
   MUX_2_to_1_3: MUX_2to1
      PORT MAP(
        MUX2_1_In(0)=>A(3),
        MUX2_1_In(1)=>B(3),
        MUX2_1_Out=>D(3),
        EN=> LS
        );
end Behavioral;
```

2 to 1 MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX_2to1 is
   Port ( MUX2_1_In : in STD_LOGIC_VECTOR (1 downto 0);
        EN : in STD_LOGIC;
        MUX2_1_Out : out STD_LOGIC);
end MUX_2to1;

architecture Behavioral of MUX_2to1 is

begin
   MUX2_1_Out<=((NOT EN) AND MUX2_1_In(1)) OR (EN AND MUX2_1_In(0));


end Behavioral;
```

Register Bank

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Register_Bank is
   Port ( Clk : in STD_LOGIC;
        Res : in STD_LOGIC;
        Reg_In : in STD_LOGIC_VECTOR (3 downto 0);
        En : in STD_LOGIC_VECTOR (2 downto 0);
        R0 : out STD_LOGIC_VECTOR (3 downto 0);
```

```
        R1 : out STD_LOGIC_VECTOR (3 downto 0);
        R2 : out STD_LOGIC_VECTOR (3 downto 0);
        R3 : out STD_LOGIC_VECTOR (3 downto 0);
        R4 : out STD_LOGIC_VECTOR (3 downto 0);
        R5 : out STD_LOGIC_VECTOR (3 downto 0);
        R6 : out STD_LOGIC_VECTOR (3 downto 0);
        R7 : out STD_LOGIC_VECTOR (3 downto 0));
end Register_Bank;

architecture Behavioral of Register_Bank is
Component Register_4_bit
   Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
        Clk : in STD_LOGIC;
        Res : in STD_LOGIC;
        En : in STD_LOGIC;
        Q : out STD_LOGIC_VECTOR (3 downto 0));
end Component;
Component Decoder_3_to_8
   Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
        EN : in STD_LOGIC;
        Y : out STD_LOGIC_VECTOR (7 downto 0));
end Component;

Signal y : STD_LOGIC_VECTOR (7 downto 0);

begin
Decoder_3_to_8_1 : Decoder_3_to_8
    Port Map(
        I => En,
        EN => '1',
        Y => y);

Register_4_bit_0 : Register_4_bit
    Port Map(
    D => "0000",
    Clk => Clk,
    Res => Res,
    En => y(0),
    Q => R0
    );
Register_4_bit_1 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
```

```
Res => Res,
En => y(1),
Q => R1
);
Register_4_bit_2 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(2),
Q => R2
);
Register_4_bit_3 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(3),
Q => R3
);
Register_4_bit_4 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(4),
Q => R4
);
Register_4_bit_5 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(5),
Q => R5
);
Register_4_bit_6 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(6),
Q => R6
);
```

```
Register_4_bit_7 : Register_4_bit
    Port Map(
D => Reg_In,
Clk => Clk,
Res => Res,
En => y(7),
Q => R7
);

end Behavioral;
```

3 to 8 decoder

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Decoder_3_to_8 is
   Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
          EN : in STD_LOGIC;
          Y : out STD_LOGIC_VECTOR (7 downto 0));
end Decoder_3_to_8;

architecture Behavioral of Decoder_3_to_8 is
    component Decoder_2_to_4
    port(
       I: in STD_LOGIC_VECTOR;
       EN: in STD_LOGIC;
       Y: out STD_LOGIC_VECTOR );
   end component;
     signal I0,I1 : STD_LOGIC_VECTOR (1 downto 0);
     signal Y0,Y1 : STD_LOGIC_VECTOR (3 downto 0);
     signal en0,en1, I2 : STD_LOGIC;

begin
   Decoder_2_to_4_0 : Decoder_2_to_4
   port map(
   I => I0,
   EN => en0,
   Y => Y0 );
   Decoder_2_to_4_1 : Decoder_2_to_4
   port map(
   I => I1,
   EN => en1,
   Y => Y1 );
   en0 <= NOT(I(2)) AND EN;
   en1 <= I(2) AND EN;
```

```
   I0 <= I(1 downto 0);
   I1 <= I(1 downto 0);
   I2 <= I(2);
   Y(3 downto 0) <= Y0;
   Y(7 downto 4) <= Y1;

end Behavioral;
```

Register

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Register_4_bit is
   Port ( D : in STD_LOGIC_VECTOR (3 downto 0);
          Clk : in STD_LOGIC;
          Res : in STD_LOGIC;
          En : in STD_LOGIC;
          Q : out STD_LOGIC_VECTOR (3 downto 0));
end Register_4_bit;

architecture Behavioral of Register_4_bit is

begin
process(Clk)
begin
   if (rising_edge(Clk)) then
      if (Res = '1') then
         Q <= "0000";
      elsif (En = '1') then
         Q <= D;
      end if;
    end if;
end process;

end Behavioral;
```

4bit Add/Substract Unit

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Adder_Subtractor_2 is
   Port ( A : in STD_LOGIC_VECTOR (3 downto 0);
          B : in STD_LOGIC_VECTOR (3 downto 0);
          C_in : in STD_LOGIC;
          C_out : out STD_LOGIC;
```

```
        S : out STD_LOGIC_VECTOR (3 downto 0);
        Zero : out STD_LOGIC);
end Adder_Subtractor_2;

architecture Behavioral of Adder_Subtractor_2 is
    component FA
    port( A : in STD_LOGIC;
          B : in STD_LOGIC;
          C_in : in STD_LOGIC;
          S : out STD_LOGIC;
          C_Out : out STD_LOGIC);
     end component;

     signal FA0_C,FA1_C,FA2_C, FA3_C :STD_LOGIC;
     signal FA0_B,FA1_B,FA2_B,FA3_B :STD_LOGIC;
     signal S_0,S_1,S_2,S_3 :STD_LOGIC;



begin
   FA0 : FA
   PORT MAP(
   A => A(0),
   B => FA0_B,
   S => S_0,
   C_in => C_in,
   C_Out => FA0_C);

FA1 : FA
       PORT MAP(
       A => A(1),
       B => FA1_B,
       S => S_1,
       C_in => FA0_C,
       C_Out => FA1_C);

FA2 : FA
   PORT MAP(
   A => A(2),
   B => FA2_B,
   S => S_2,
   C_in => FA1_C,
   C_Out => FA2_C);
```

```
FA3 : FA
    PORT MAP(
    A => A(3),
    B => FA3_B,
    S => S_3,
    C_in => FA2_C,
    C_Out => FA3_C);

FA0_B <= B(0) XOR C_in;
FA1_B <= B(1) XOR C_in;
FA2_B <= B(2) XOR C_in;
FA3_B <= B(3) XOR C_in;

--S_0 <= FA0_B XOR A(0) XOR C_in;
--S_1 <= FA1_B XOR A(1) XOR FA0_C;
--S_2 <= FA2_B XOR A(2) XOR FA1_C;
--S_3 <= FA3_B XOR A(3) XOR FA2_C;

S(0) <= S_0;
S(1) <= S_1;
S(2) <= S_2;
S(3) <= S_3;

Zero <= not(S_0 or S_1 or S_2 or S_3);


C_out <= FA3_C;
end Behavioral;
```

8 way4-bit MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Way8_4_MUX is
   Port ( D0 : in STD_LOGIC_VECTOR (3 downto 0);
          D1 : in STD_LOGIC_VECTOR (3 downto 0);
          D2 : in STD_LOGIC_VECTOR (3 downto 0);
          D3 : in STD_LOGIC_VECTOR (3 downto 0);
          D4 : in STD_LOGIC_VECTOR (3 downto 0);
          D5 : in STD_LOGIC_VECTOR (3 downto 0);
          D6 : in STD_LOGIC_VECTOR (3 downto 0);
          D7 : in STD_LOGIC_VECTOR (3 downto 0);
          S : in STD_LOGIC_VECTOR (2 downto 0);
          Y : out STD_LOGIC_VECTOR (3 downto 0));
end Way8_4_MUX;
```

```
architecture Behavioral of Way8_4_MUX is
   component Mux_8_to_1
   Port ( S : in STD_LOGIC_VECTOR (2 downto 0);
          D : in STD_LOGIC_VECTOR (7 downto 0);
          EN : in STD_LOGIC;
          Y : out STD_LOGIC);
   end component;


begin
   Mux_8_to_1_0: Mux_8_to_1
   PORT MAP(
      D(0)=>D0(0),
      D(1)=>D1(0),
      D(2)=>D2(0),
      D(3)=>D3(0),
      D(4)=>D4(0),
      D(5)=>D5(0),
      D(6)=>D6(0),
      D(7)=>D7(0),
      S=>S,
      EN=>'1',
      Y=>Y(0)
      );
    Mux_8_to_1_1: Mux_8_to_1
      PORT MAP(
      D(0)=>D0(1),
      D(1)=>D1(1),
      D(2)=>D2(1),
      D(3)=>D3(1),
      D(4)=>D4(1),
      D(5)=>D5(1),
      D(6)=>D6(1),
      D(7)=>D7(1),
      S=>S,
      EN=>'1',
      Y=>Y(1)
      );
    Mux_8_to_1_2: Mux_8_to_1
      PORT MAP(
      D(0)=>D0(2),
      D(1)=>D1(2),
      D(2)=>D2(2),
```

```
      D(3)=>D3(2),
      D(4)=>D4(2),
      D(5)=>D5(2),
      D(6)=>D6(2),
      D(7)=>D7(2),
      S=>S,
      EN=>'1',
      Y=>Y(2)
      );
   Mux_8_to_1_3: Mux_8_to_1
      PORT MAP(
      D(0)=>D0(3),
      D(1)=>D1(3),
      D(2)=>D2(3),
      D(3)=>D3(3),
      D(4)=>D4(3),
      D(5)=>D5(3),
      D(6)=>D6(3),
      D(7)=>D7(3),
      S=>S,
      EN=>'1',
      Y=>Y(3)
      );

end Behavioral;
```

3 bit-RCA

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity RCA_3 is
   Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
        --B : in STD_LOGIC_VECTOR (2 downto 0);
         S : out STD_LOGIC_VECTOR (2 downto 0);
         C_in : in STD_LOGIC;
         C_out : out STD_LOGIC);
end RCA_3;

architecture Behavioral of RCA_3 is
COMPONENT FA
    port(
        A: in std_logic;
        B: in std_logic;
        C_in: in std_logic;
```

```
        S: out std_logic;
        C_out: out std_logic);
END COMPONENT;
SIGNAL FA0_S, FA0_C, FA1_S, FA1_C, FA2_S : std_logic;

begin
   FA_0 : FA
    port map (
    A => A(0),
    B => '1',
    C_in => '0',-- Set to ground
    S => S(0),
    C_Out => FA0_C);

   FA_1 : FA
    port map (
    A => A(1),
    B => '0',
    C_in => FA0_C,
    S => S(1),
    C_Out => FA1_C);

   FA_2 : FA
    port map (
    A => A(2),
    B => '0',
    C_in => FA1_C,
    S => S(2),
    C_Out => C_out);


end Behavioral;
```

2 way3-Bit MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Way2_3_Mux is
   Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
        B : in STD_LOGIC_VECTOR (2 downto 0);
        JF : in STD_LOGIC;
        To_PC : out STD_LOGIC_VECTOR (2 downto 0));
end Way2_3_Mux;

architecture Behavioral of Way2_3_Mux is
```

```
    component MUX_2to1
    Port ( MUX2_1_In : in STD_LOGIC_VECTOR (1 downto 0);
           EN : in STD_LOGIC;
           MUX2_1_Out : out STD_LOGIC);
    end component;

begin
    MUX_2_1_0 : MUX_2to1
    PORT MAP(
       MUX2_1_In(0)=>A(0),
       MUX2_1_In(1)=>B(0),
       EN=>JF,
       MUX2_1_Out=>To_PC(0));

   MUX_2_1_1 : MUX_2to1
   PORT MAP(
      MUX2_1_In(0)=>A(1),
      MUX2_1_In(1)=>B(1),
      EN=>JF,
      MUX2_1_Out=>To_PC(1));

   MUX_2_1_2 : MUX_2to1
   PORT MAP(
     MUX2_1_In(0)=>A(2),
     MUX2_1_In(1)=>B(2),
     EN=>JF,
     MUX2_1_Out=>To_PC(2));

end Behavioral;
```

Program Counter

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Program_Counter is
    Port ( Input : in STD_LOGIC_VECTOR (2 downto 0):="000";
           Output : out STD_LOGIC_VECTOR (2 downto 0);
           Clk : in STD_LOGIC;
           Reset : in STD_LOGIC);
end Program_Counter;

architecture Behavioral of Program_Counter is
    component D_FF
       Port( D : in STD_LOGIC;
          Res : in STD_LOGIC;
```

```
        Clk : in STD_LOGIC;
        Q : out STD_LOGIC;
        Qbar : out STD_LOGIC);
    end component;
begin
    D_FF_0: D_FF
        PORT MAP(
        D=>Input(0),
        Res=> Reset,
        Clk=>Clk,
        Q=>Output(0));

    D_FF_1: D_FF
        PORT MAP(
        D=>Input(1),
        Res=> Reset,
        Clk=>Clk,
        Q=>Output(1));

     D_FF_2: D_FF
       PORT MAP(
       D=>Input(2),
       Res=> Reset,
       Clk=>Clk,
       Q=>Output(2));

end Behavioral;
```

Instruction Decoder

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Instruction_Decoder is
    Port ( Ins : in STD_LOGIC_VECTOR (11 downto 0);
           Reg_Chk : in STD_LOGIC_VECTOR (3 downto 0);
           AS_S : out STD_LOGIC;
           LS : out STD_LOGIC;
           Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
           Reg_S1 : out STD_LOGIC_VECTOR (2 downto 0);
           Reg_S2 : out STD_LOGIC_VECTOR (2 downto 0);
           JF : out STD_LOGIC;
           J_AD : out STD_LOGIC_VECTOR (2 downto 0);
           Im_Val : out STD_LOGIC_VECTOR (3 downto 0));
end Instruction_Decoder;
```

```
architecture Behavioral of Instruction_Decoder is

    signal func : STD_LOGIC_VECTOR (1 downto 0);
    signal reg_1 , reg_2: STD_LOGIC_VECTOR (2 downto 0);
    signal I_Val : STD_LOGIC_VECTOR (3 downto 0);
    signal Jump_AD : STD_LOGIC_VECTOR (2 downto 0);


begin

 process (func,reg_1,reg_2,Jump_AD,I_Val,Reg_Chk)
 begin
 JF <= '0';
 Reg_EN <= "000";
 if  (func = "10") then
    Im_Val <= I_Val;
    Reg_EN <= reg_1;
    LS <= '0';

elsif (func="00") then
    AS_S<='0';
    Reg_S1<=reg_1;
    Reg_S2<=reg_2;
    Reg_EN<=reg_1;
    LS<='1';


elsif (func="01") then
        AS_S<='1';
        Reg_S1<="000";
        Reg_S2<=reg_1;
        Reg_EN<=reg_1;
        LS<='1';

elsif (func="11") then

        Reg_S1<=reg_1;
        if (Reg_Chk = "0000") then
           JF <= '1';
           J_AD <= Jump_AD;
           LS <= '0';
        end if ;
 end if ;
```

```
end process;

  func <= Ins(11 downto 10);
  reg_1 <= Ins(9 downto 7);
  reg_2 <= Ins(6 downto 4);
  I_Val <= Ins(3 downto 0);
  Jump_AD <= Ins(2 downto 0);


end Behavioral;
```

ROM

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;
entity ROM is
    Port ( PC : in STD_LOGIC_VECTOR (2 downto 0);
           Ins : out STD_LOGIC_VECTOR (11 downto 0));
end ROM;

architecture Behavioral of ROM is

type rom_type is array (0 to 7) of std_logic_vector(11 downto 0);

signal ROM: rom_type := (

          "101110000000",
          "100010000001",
          "100100000010",
          "100110000011",
          "001110010000",
          "001110100000",
          "001110110000",
          "110000000111");

begin

    Ins<= ROM(to_integer(unsigned(PC)));

end Behavioral;
```

Slow Clock

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Slow_Clk is
   Port ( Clk_in : in STD_LOGIC;
          Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count: integer :=1;
signal clk_status : std_logic :='0';

begin

   process (Clk_in) begin
      if(rising_edge (Clk_in)) then
         count<=count+1;
         if (count = 50 000 000) then
            clk_status <= not clk_status;
            Clk_out <= clk_status;
            count<=1;
         end if;
      end if;
   end process;

end Behavioral;
```

TEST BENCH FILES

Nano processor

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_Nano is
--  Port ( );
end TB_Nano;

architecture Behavioral of TB_Nano is
   component Nano
```

```
    port(     Clk : in STD_LOGIC;
              Res : in STD_LOGIC;
              C : out STD_LOGIC;
              Z : out STD_LOGIC;
              R7_out : out STD_LOGIC_VECTOR (3 downto 0);
              S7_seg : out STD_LOGIC_VECTOR (6 downto 0);
              Anode : out STD_LOGIC_VECTOR (3 downto 0));
    end component;
    signal R ,c ,z : STD_LOGIC;
    signal r_out,anode : STD_LOGIC_VECTOR (3 downto 0);
    signal S : STD_LOGIC_VECTOR (6 downto 0);
    signal clk : STD_LOGIC := '0';

begin
    UUT : Nano
    port map(
          Clk => clk,
          Res => R,
          C => c,
          Z => z,
          R7_out => r_out,
          S7_seg => S,
          Anode => anode);
process
begin
    clk <= NOT (clk);
    wait for 2ns;
end process;


process
begin
        R <= '1';
        wait for 40ns;

         R <= '0';
         wait;
end process;

end Behavioral;
```

2 way 4-bit MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_Way2_4_MUX is
--  Port ( );
end TB_Way2_4_MUX;

architecture Behavioral of TB_Way2_4_MUX is
    component Way2_4bit_MUX
      Port ( A : in STD_LOGIC_VECTOR (3 downto 0);--LS=0; D = A
             B : in STD_LOGIC_VECTOR (3 downto 0);
             LS : in STD_LOGIC;
             D : out STD_LOGIC_VECTOR (3 downto 0));
    end component;

    signal A, B, D : STD_LOGIC_VECTOR (3 downto 0);
    signal LS: STD_LOGIC;

begin
   UUT: Way2_4bit_MUX
      Port MAP(
         A=>A,
         B=>B,
         LS=> LS,
         D=> D);

process
   begin
      A<="1010";
      B<="0010";
      LS<='0';
      wait for 30ns;

      LS<='1';
      wait for 30ns;

      A<="1111";
      B<="0101";
      LS<='0';
      wait for 30ns;

      LS<='1';
      wait for 30ns;
```

```
        A<="1000";
        B<="1110";
        LS<='0';
        wait for 30ns;

        LS<='1';
        wait for 30ns;

        A<="1110";
        B<="0110";
        LS<='0';
        wait for 30ns;

        LS<='1';
        wait for 30ns;

        A<="1001";
        B<="0101";
        LS<='0';
        wait for 30ns;

        LS<='1';
        wait for 30ns;

        A<="1011";
        B<="1110";
        LS<='0';
        wait for 30ns;

        LS<='1';
        wait for 30ns;
    end process;

end Behavioral;
```

2to1 MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_2_1_MUX is
--  Port ( );
```

```
end TB_2_1_MUX;

architecture Behavioral of TB_2_1_MUX is
   component  MUX_2to1
      Port ( MUX2_1_In : in STD_LOGIC_VECTOR (1 downto 0);
           EN : in STD_LOGIC;
           MUX2_1_Out : out STD_LOGIC);
   end component;

signal MUX2_1_In: STD_LOGIC_VECTOR;
signal EN, MUX2_1_Out: STD_LOGIC;

begin

   UUT: MUX_2to1
     PORT MAP(
      MUX2_1_In=>MUX2_1_In,
      EN=>EN,
      MUX2_1_Out=> MUX2_1_Out);

process
begin
   MUX2_1_In(0)<='0';
   MUX2_1_In(1)<='1';
   EN<='1';
   wait for 40ns;

   MUX2_1_In(0)<='1';
   MUX2_1_In(1)<='0';
   EN<='1';
   wait for 40ns;

   MUX2_1_In(0)<='0';
   MUX2_1_In(1)<='1';
   EN<='0';
   wait for 40ns;

   MUX2_1_In(0)<='0';
   MUX2_1_In(1)<='1';
   EN<='1';
   wait for 40ns;

end process;
```

```
end Behavioral;
```

Register Bank

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_Register_Bank is
--  Port ( );
end TB_Register_Bank;

architecture Behavioral of TB_Register_Bank is
component Register_Bank
        port( Clk : in STD_LOGIC;
          Res : in STD_LOGIC;
          Reg_In : in STD_LOGIC_VECTOR (3 downto 0);
          En : in STD_LOGIC_VECTOR (2 downto 0);
          R0 : out STD_LOGIC_VECTOR (3 downto 0);
          R1 : out STD_LOGIC_VECTOR (3 downto 0);
          R2 : out STD_LOGIC_VECTOR (3 downto 0);
          R3 : out STD_LOGIC_VECTOR (3 downto 0);
          R4 : out STD_LOGIC_VECTOR (3 downto 0);
          R5 : out STD_LOGIC_VECTOR (3 downto 0);
          R6 : out STD_LOGIC_VECTOR (3 downto 0);
          R7 : out STD_LOGIC_VECTOR (3 downto 0));
end component;
signal Clk :  STD_LOGIC := '0';
signal Res :  STD_LOGIC;
signal Reg_In :  STD_LOGIC_VECTOR (3 downto 0);
signal En :  STD_LOGIC_VECTOR (2 downto 0);
signal R0,R1,R2,R3,R4,R5,R6,R7 :  STD_LOGIC_VECTOR (3 downto 0);


begin
UUT : Register_Bank
    PORT MAP(Clk => Clk,
            Res => Res,
            Reg_In => Reg_In,
            En => En,
            R0 => R0,
            R1 => R1,
            R2 => R2,
            R3 => R3,
            R4 => R4,
            R5 => R5,
            R6 => R6,
```

```
            R7 => R7);

Process
begin
   wait for 5ns;
   Clk <= NOT(Clk);
end Process;

process
begin
   Res <= '1';
   wait for 50ns;
   Res <= '0';
   R0 <= "0000";
   Reg_In <= "0110";
   En <= "001";
   wait for 50ns;
   En <= "010";
   wait for 50ns;
   En <= "011";
   wait for 50ns;
   En <= "100";
   wait for 50ns;
   En <= "101";
   wait for 50ns;
   En <= "110";
   wait for 50ns;
   En <= "111";
   wait for 50ns;
   wait;
end process;

end Behavioral;
```

4bit Add/Substractor Unit

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_Adder_Subtrator_2 is
--  Port ( );
end TB_Adder_Subtrator_2;

architecture Behavioral of TB_Adder_Subtrator_2 is
     component Adder_Subtractor_2
```

```
    port(     A : in STD_LOGIC_VECTOR (3 downto 0);
              B : in STD_LOGIC_VECTOR (3 downto 0);
              C_in : in STD_LOGIC;
              C_out : out STD_LOGIC;
              S : out STD_LOGIC_VECTOR (3 downto 0);
              Zero : out STD_LOGIC);
    end component;
    signal C_in , C_out , Zero : STD_LOGIC;
    signal A,B,S : STD_LOGIC_VECTOR (3 downto 0);

begin
UUT : Adder_Subtractor_2
   port map(
   A => A,
   B => B,
   S => S,
   C_in => C_in,
   C_out => C_out,
   Zero => Zero);

 process
 begin
 C_in <= '0';
 A <= "1001";
 B <= "0111";
 WAIT FOR 100ns;

 A <= "1000";
  B <= "0011";
   WAIT FOR 100ns;

    A <= "1001";
   B <= "1011";
    WAIT FOR 100ns;

    C_in <= '1';
     A <= "1111";
    B <= "1101";
     WAIT FOR 100ns;

      A <= "1101";
     B <= "1001";
      WAIT FOR 100ns;
```

```
      A <= "1011";
     B <= "0111";
      WAIT FOR 100ns;

    A <= "1001";
   B <= "1000";
    WAIT FOR 100ns;
  wait;
 end process;

end Behavioral;
```

8Way 4bit MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Way8_TB is
--  Port ( );
end Way8_TB;

architecture Behavioral of Way8_TB is
   component Way8_4_MUX
   Port ( D0, D1, D2, D3, D4, D5, D6, D7 : in STD_LOGIC_VECTOR (3 downto 0);
          S : in STD_LOGIC_VECTOR (2 downto 0);
          Y : out STD_LOGIC_VECTOR (3 downto 0));
   end component;

   signal D0, D1, D2, D3, D4, D5, D6, D7 : STD_LOGIC_VECTOR (3 downto 0);
   signal S: STD_LOGIC_VECTOR (2 downto 0);
   signal Y: STD_LOGIC_VECTOR (3 downto 0);

begin
   UUT: Way8_4_MUX
   PORT MAP(
      D0=>D0,
      D1=>D1,
      D2=>D2,
      D3=>D3,
      D4=>D4,
      D5=>D5,
      D6=>D6,
      D7=>D7,
      S=>S,
      Y=>Y
```

```
    );
  process

  begin
  D0<="0000";
  D1<="0001";
  D2<="0010";
  D3<="0011";
  D4<="0100";
  D5<="0101";
  D6<="0110";
  D7<="0111";

  S<="000";
  wait for 100ns;
  S<="001";
  wait for 50ns;
  S<="010";
  wait for 50ns;
  S<="011";
  wait for 50ns;
  S<="100";
  wait for 50ns;
  S<="101";
  wait for 50ns;
  S<="110";
  wait for 50ns;
  S<="111";
  wait;
  end process;

end Behavioral;
```

3 bit RCA

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_RCA_3 is
--  Port ( );
end TB_RCA_3;

architecture Behavioral of TB_RCA_3 is
COMPONENT RCA_3
PORT(A : in STD_LOGIC_VECTOR (2 downto 0);
```

```
        S : out STD_LOGIC_VECTOR (2 downto 0);
        C_in : in STD_LOGIC;
        C_out : out STD_LOGIC);
END COMPONENT;
SIGNAL C_out : STD_LOGIC;
SIGNAL A,S:  STD_LOGIC_VECTOR (2 downto 0);

begin
UUT : RCA_3 PORT MAP(
 A(0) =>A(0),
 A(1)=>A(1),
 A(2)=>A(2),

 C_in =>'0',

 S(0) =>S(0),
 S(1) =>S(1),
 S(2) =>S(2),

 C_out =>C_out);

process
begin
---------------------------- Index No =210203M----------- 0011 0011 0101 0001 1011------
-- 0001 +1011
 A(0)<= '1';
 A(1)<= '0';
 A(2)<= '0';

 wait for 100ns;

 A(0)<= '1';
 A(1)<= '1';
 A(2)<= '0';

 wait for 100ns;

  A(0)<= '1';
 A(1)<= '0';
 A(2)<= '1';

 wait for 100ns;

  A(0)<= '1';
```

```
 A(1)<= '0';
 A(2)<= '1';

 wait for 100ns;

 A(0)<= '0';
 A(1)<= '0';
 A(2)<= '1';

 wait for 100ns;
 end process;

end Behavioral;
```

2 way 3 bit MUX

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity TB_2way_3bit_MUX is
--  Port ( );
end TB_2way_3bit_MUX;

architecture Behavioral of TB_2way_3bit_MUX is
   component Way2_3_Mux
      Port ( A : in STD_LOGIC_VECTOR (2 downto 0);
           B : in STD_LOGIC_VECTOR (2 downto 0);
           JF : in STD_LOGIC;
           To_PC : out STD_LOGIC_VECTOR (2 downto 0));
   end component;

   signal A,B, To_PC : STD_LOGIC_VECTOR(2 downto 0);
   signal JF: STD_LOGIC;

begin
   UUT: Way2_3_Mux
      PORT MAP(
         A=>A,
         B=>B,
         JF=>JF,
         To_PC=>To_PC);
   process
   begin
      A<="001";
```

```
        B<="100";
        JF<='1';

        wait for 40ns;

        A<="001";
        B<="100";
        JF<='0';

        wait for 40ns;

        A<="101";
        B<="111";
        JF<='1';

        wait for 40ns;

        A<="101";
        B<="111";
        JF<='0';

        wait for 40ns;

        A<="011";
        B<="110";
        JF<='1';

        wait for 40ns;

        A<="011";
        B<="110";
        JF<='0';

        wait for 40ns;
    end process;
end Behavioral;
```

Program Counter

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_PC is
--  Port ( );
end TB_PC;

architecture Behavioral of TB_PC is
```

```
    component Program_Counter
    Port ( Input : in STD_LOGIC_VECTOR (2 downto 0);
           Output : out STD_LOGIC_VECTOR (2 downto 0);
           Clk : in STD_LOGIC;
           Reset : in STD_LOGIC);
    end component;

    signal Input, Output : STD_LOGIC_VECTOR(2 downto 0);
    signal Res : STD_LOGIC;
    signal clk: STD_LOGIC := '0';


begin
    UUT : Program_Counter
       PORT MAP(
           Input=>Input,
           Output=>Output,
           Clk=>clk,
           Reset=>Res);

process
begin
    clk<= NOT(clk);
    wait for 10ns;
end process;

process
begin
    Input<="000";
    Res<='1';
    wait for 50ns;

    Res<='0';
    wait for 50ns;

    Input<="001";
    wait for 50ns;

    Input<="110";
    wait for 50ns;

    Input<="011";
    wait for 50ns;
```

```
   Input<="111";
   wait for 50ns;

end process;

end Behavioral;
```

Instruction Decoder

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_Instruction_Decoder is
--  Port ( );
end TB_Instruction_Decoder;

architecture Behavioral of TB_Instruction_Decoder is
component Instruction_Decoder
Port(
        Ins : in STD_LOGIC_VECTOR (11 downto 0);
         Reg_Chk : in STD_LOGIC_VECTOR (3 downto 0);
         AS_S : out STD_LOGIC;
         LS : out STD_LOGIC;
         Reg_EN : out STD_LOGIC_VECTOR (2 downto 0);
         Reg_S1 : out STD_LOGIC_VECTOR (2 downto 0);
         Reg_S2 : out STD_LOGIC_VECTOR (2 downto 0);
         JF : out STD_LOGIC;
         J_AD : out STD_LOGIC_VECTOR (2 downto 0);
         Im_Val : out STD_LOGIC_VECTOR (3 downto 0));
 end component;

 signal Ins : STD_LOGIC_VECTOR (11 downto 0);
 signal Reg_Chk, Im_Val : STD_LOGIC_VECTOR (3 downto 0);
 signal Reg_EN,Reg_S1, Reg_S2, J_AD : STD_LOGIC_VECTOR (2 downto 0);
 signal LS , AS_S,JF : STD_LOGIC;


begin
UUT : Instruction_Decoder
   PORT MAP(
       Ins => Ins,
       Reg_Chk => Reg_Chk,
       AS_S => AS_S,
       LS => LS,
       Reg_EN => Reg_EN,
```

```
        Reg_S1 => Reg_S1,
        Reg_S2 => Reg_S2,
        JF => JF,
        J_AD => J_AD,
        Im_Val => Im_Val);
 process
 begin
    Reg_Chk <= "0000";
    Ins <= "100010000001";
    wait for 50ns;

    Reg_Chk <= "0001";
    Ins <= "100100000011";
    wait for 50ns;

    Ins <= "001110100000";
    wait for 50ns;

    Ins <=  "110100000111";
    wait for 50ns;

    Reg_Chk <= "0000";
    Ins <="110000000011";
    wait for 50ns;
end process;
end Behavioral;
```

ROM

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity TB_ROM is
--  Port ( );
end TB_ROM;

architecture Behavioral of TB_ROM is
   component ROM
   Port ( PC : in STD_LOGIC_VECTOR (2 downto 0);
          Ins : out STD_LOGIC_VECTOR (11 downto 0));
   end component;

   signal PC: STD_LOGIC_VECTOR (2 downto 0);
   signal Ins : STD_LOGIC_VECTOR (11 downto 0);
```

```
begin
   UUT: ROM
      PORT MAP(
         PC=>PC,
         Ins=>Ins);

process
begin

   PC<="000";
   wait for 50ns;

   PC<="001";
   wait for 50ns;

   PC<="010";
   wait for 50ns;

   PC<="011";
   wait for 50ns;

   PC<="100";
   wait for 50ns;

   PC<="101";
   wait for 50ns;

end process;

end Behavioral;
```

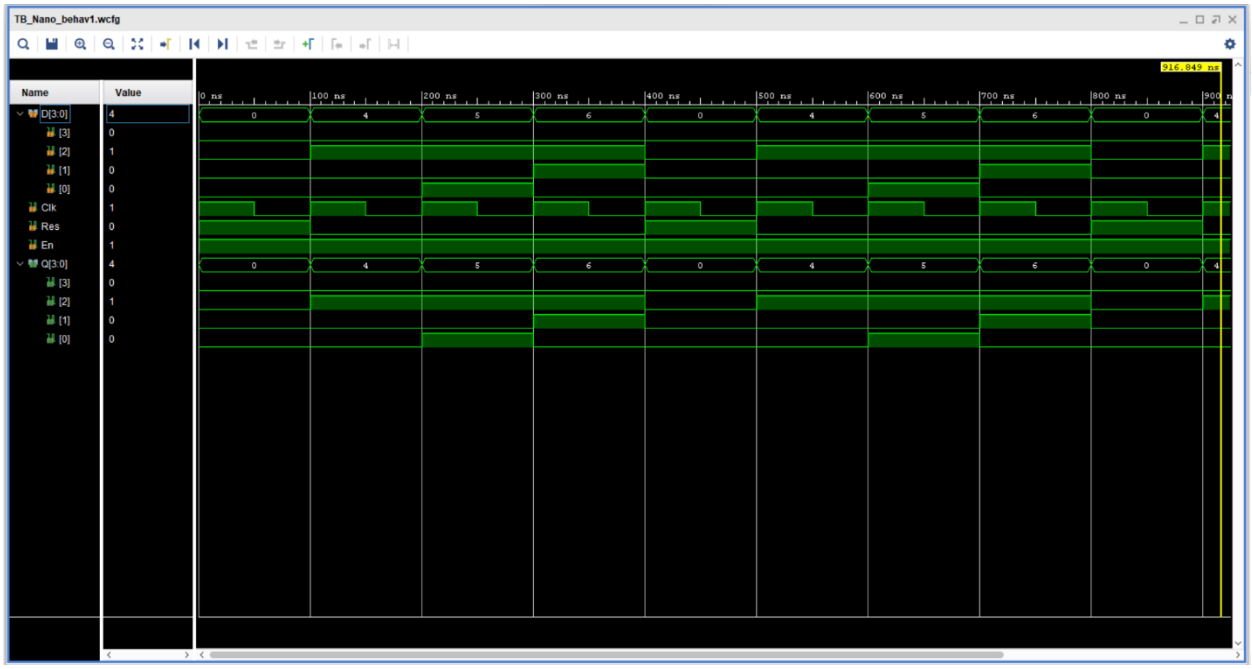
xdc File

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports {Clk}]
          set_property IOSTANDARD LVCMOS33 [get_ports {Clk}]
          create_clock-add-name sys_clk_pin-period 10.00-waveform {0 5} [get_ports {Clk}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {R7_out[0]}]
          set_property IOSTANDARD LVCMOS33 [get_ports {R7_out[0]}]
```

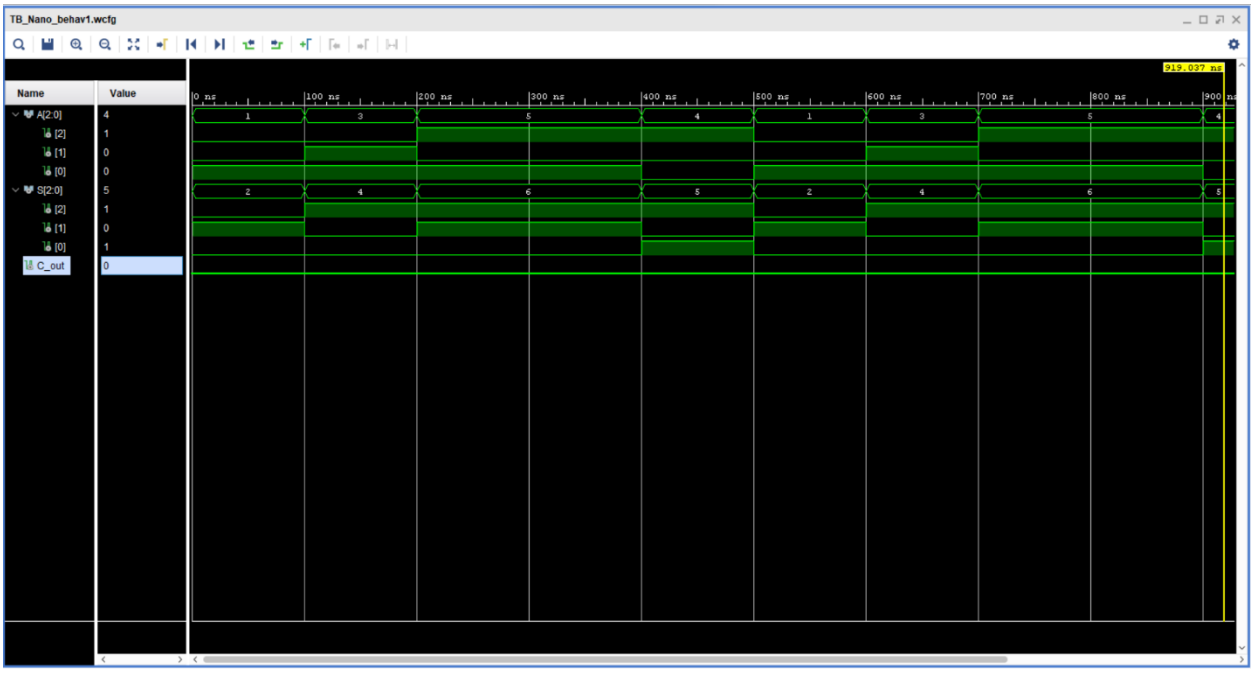
```
set_property PACKAGE_PIN E19 [get_ports {R7_out[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {R7_out[1]}]
set_property PACKAGE_PIN U19 [get_ports {R7_out[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {R7_out[2]}]
set_property PACKAGE_PIN V19 [get_ports {R7_out[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {R7_out[3]}]

set_property PACKAGE_PIN P1 [get_ports {Z}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Z}]
set_property PACKAGE_PIN L1 [get_ports {C}]
        set_property IOSTANDARD LVCMOS33 [get_ports {C}]

##7 segment display
set_property PACKAGE_PIN W7 [get_ports {S7_seg[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {S7_seg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {S7_seg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {S7_seg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {S7_seg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {S7_seg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {S7_seg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {S7_seg[6]}]

set_property PACKAGE_PIN U2 [get_ports {Anode[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode[0]}]
set_property PACKAGE_PIN U4 [get_ports {Anode[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode[1]}]
set_property PACKAGE_PIN V4 [get_ports {Anode[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode[2]}]
set_property PACKAGE_PIN W4 [get_ports {Anode[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode[3]}]




##Buttons
set_property PACKAGE_PIN U18 [get_ports {Res}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Res}]
```

Timing Diagrams

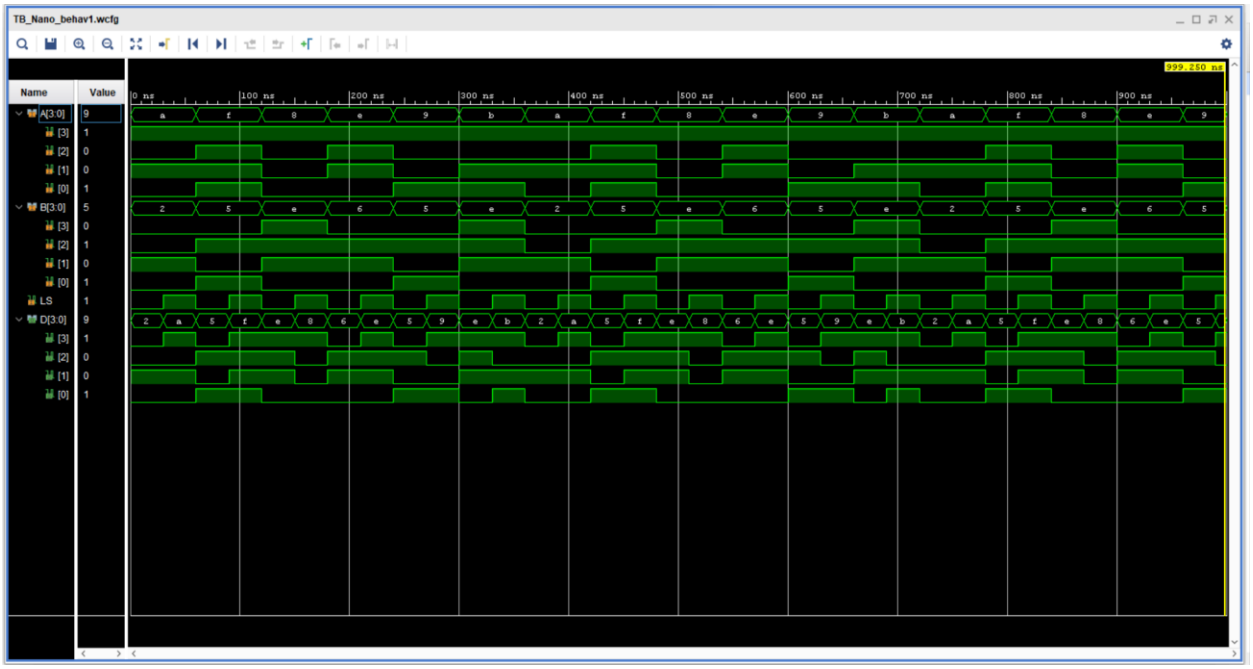
Register 4 bit



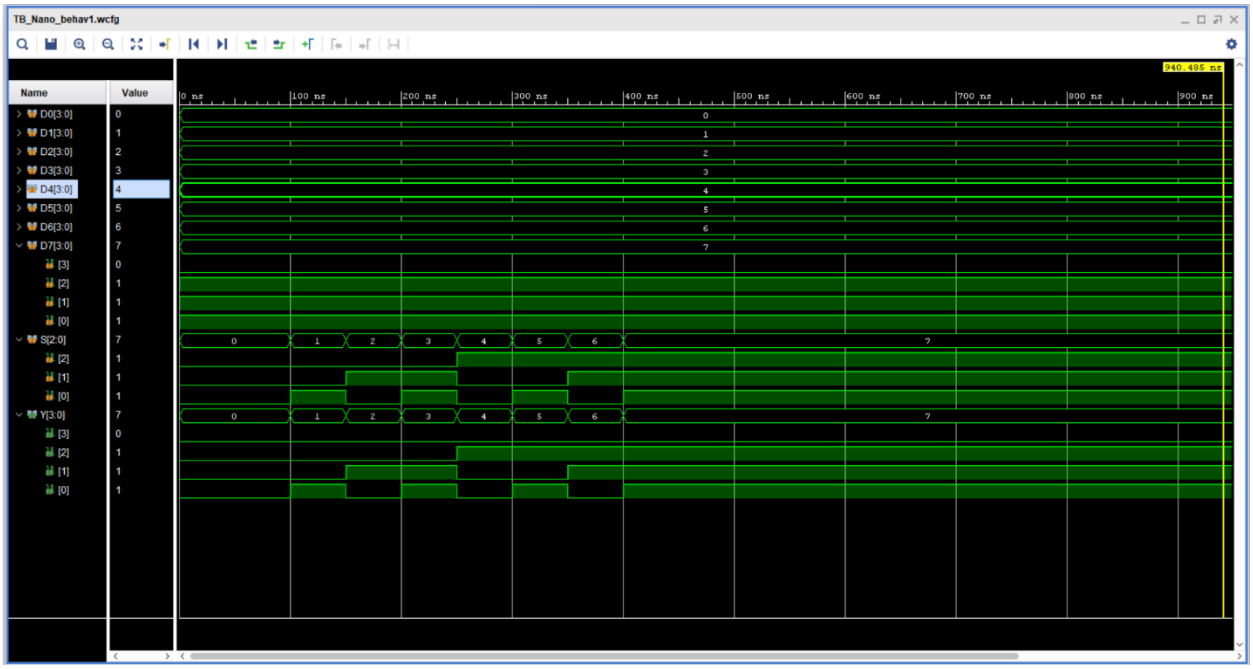
Adder 3 bit



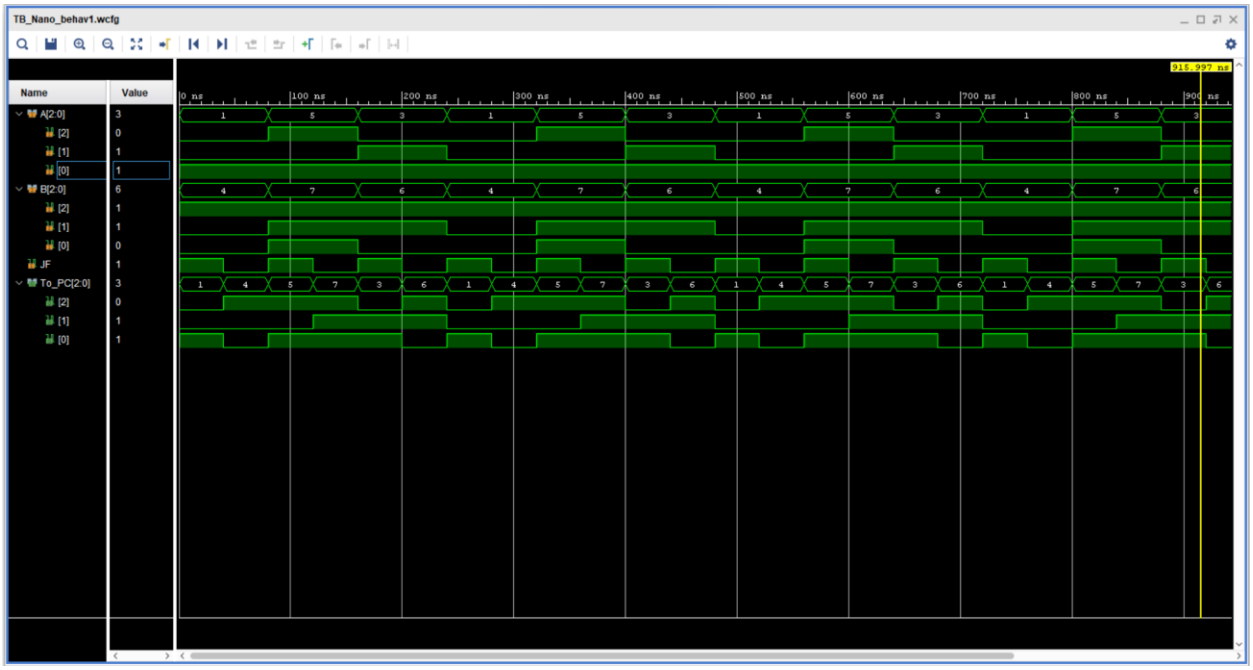
2 way 4 bit Multiplexer



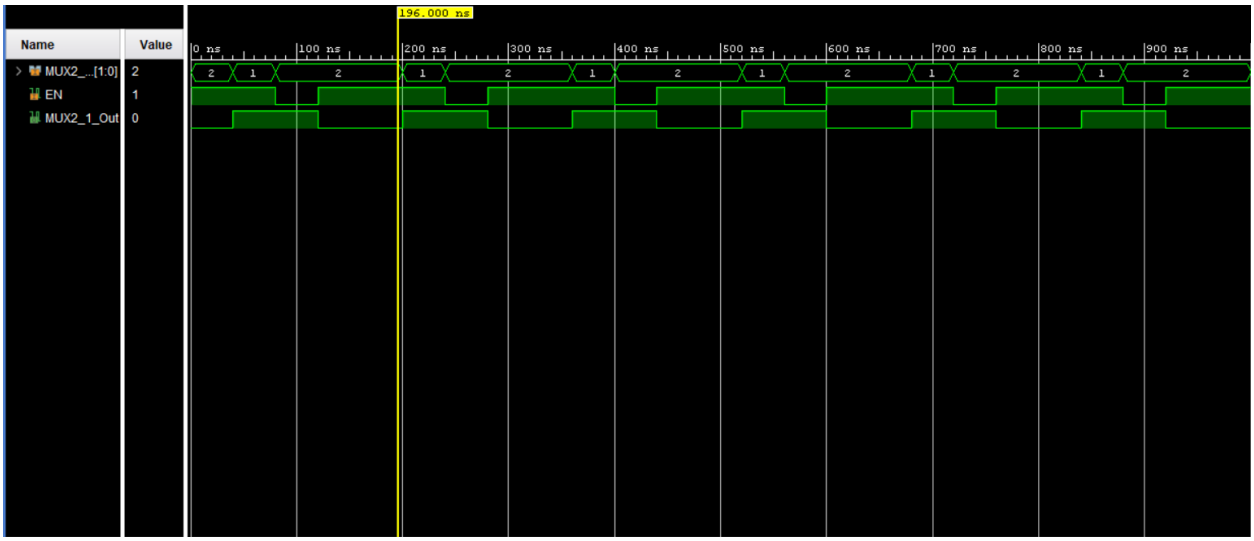
8 way 4 bit Multiplexer



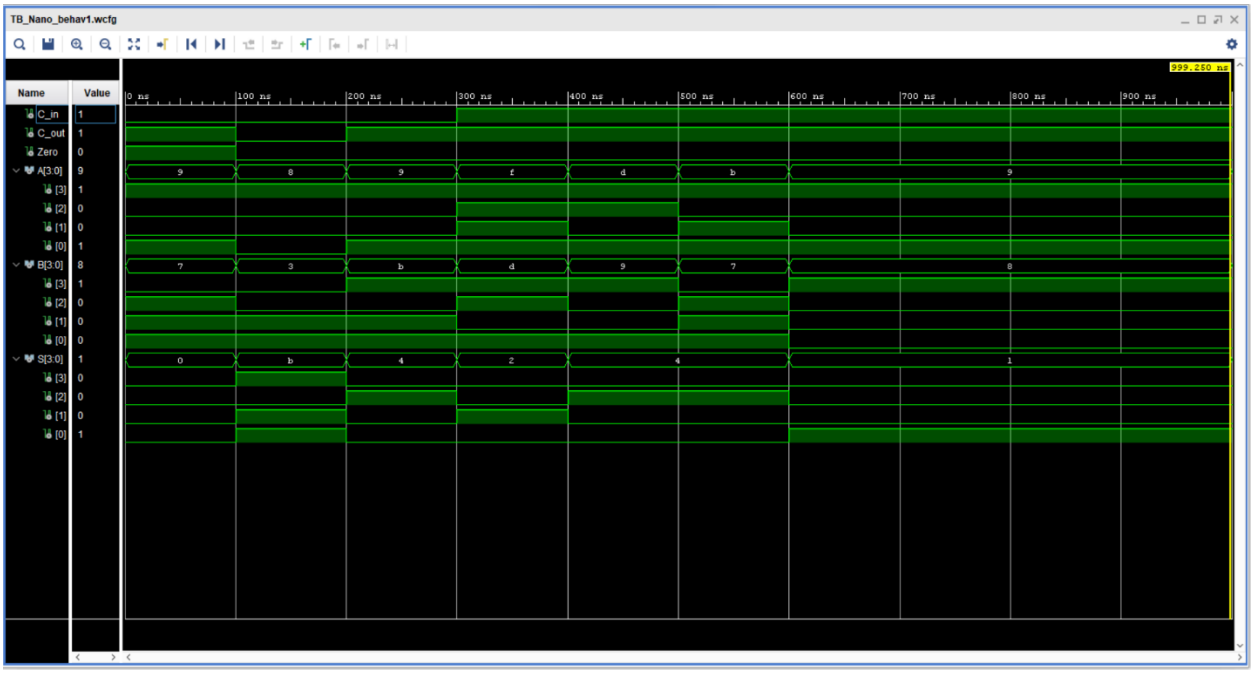
2 way 3 bit Multiplexer



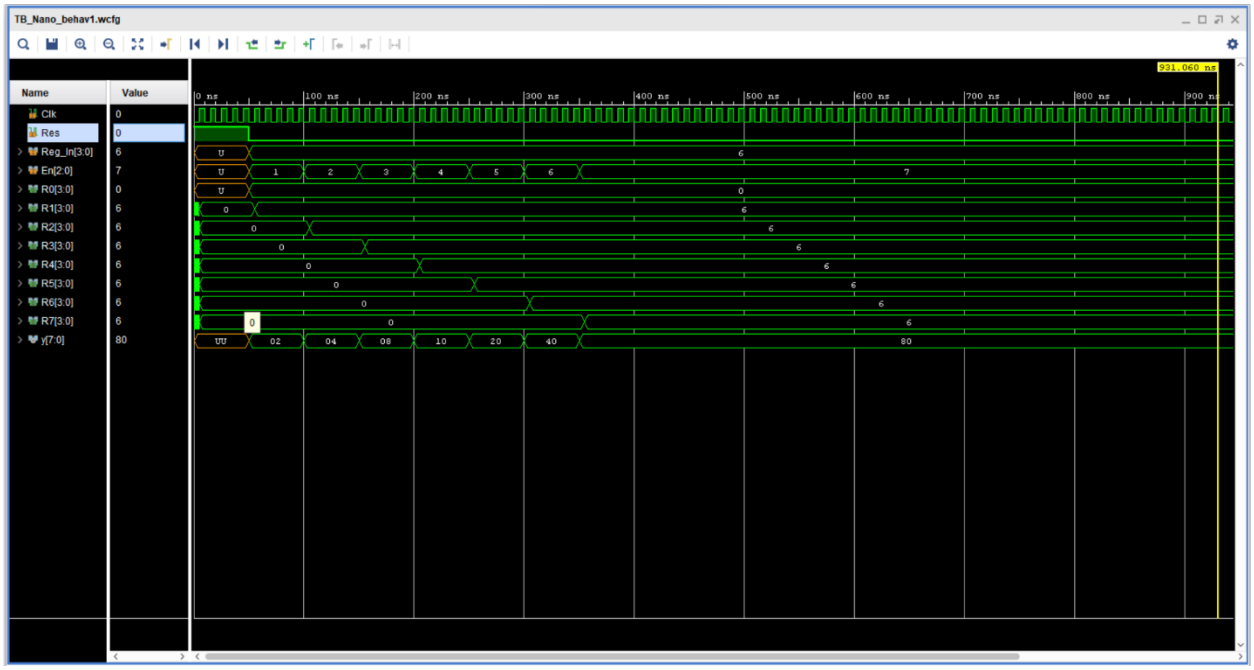
2 way 1 bit Multiplexer



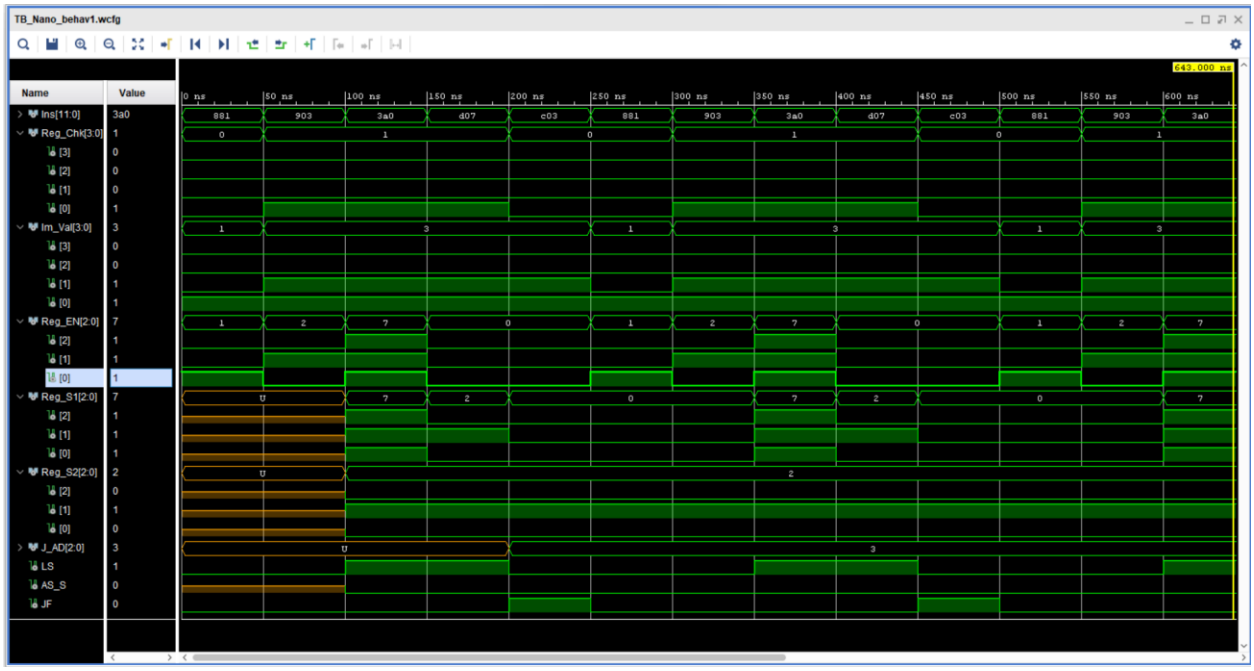
Adder Subtractor Unit



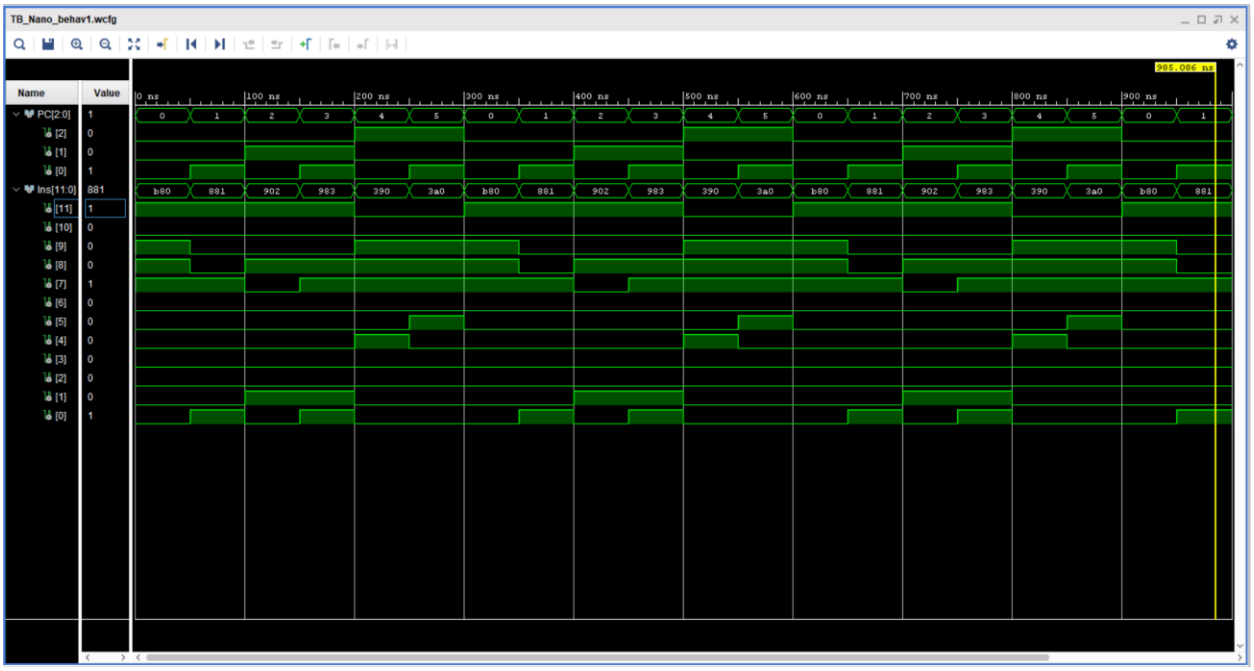
Register Bank



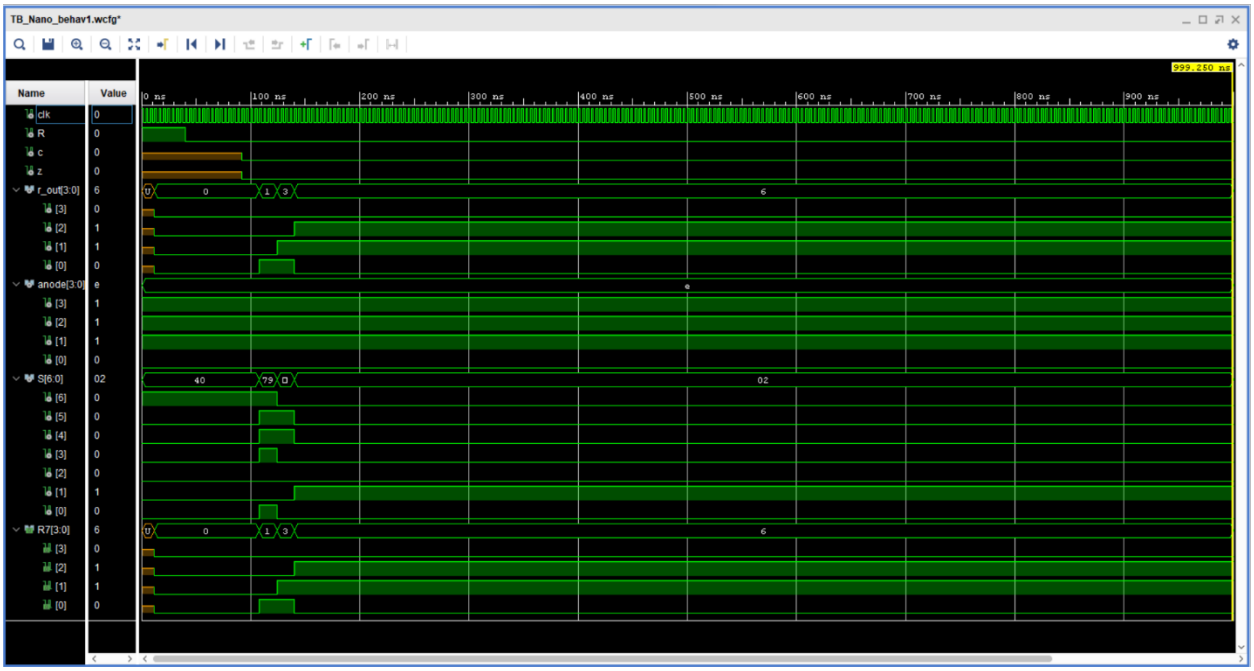
Instruction Decoder



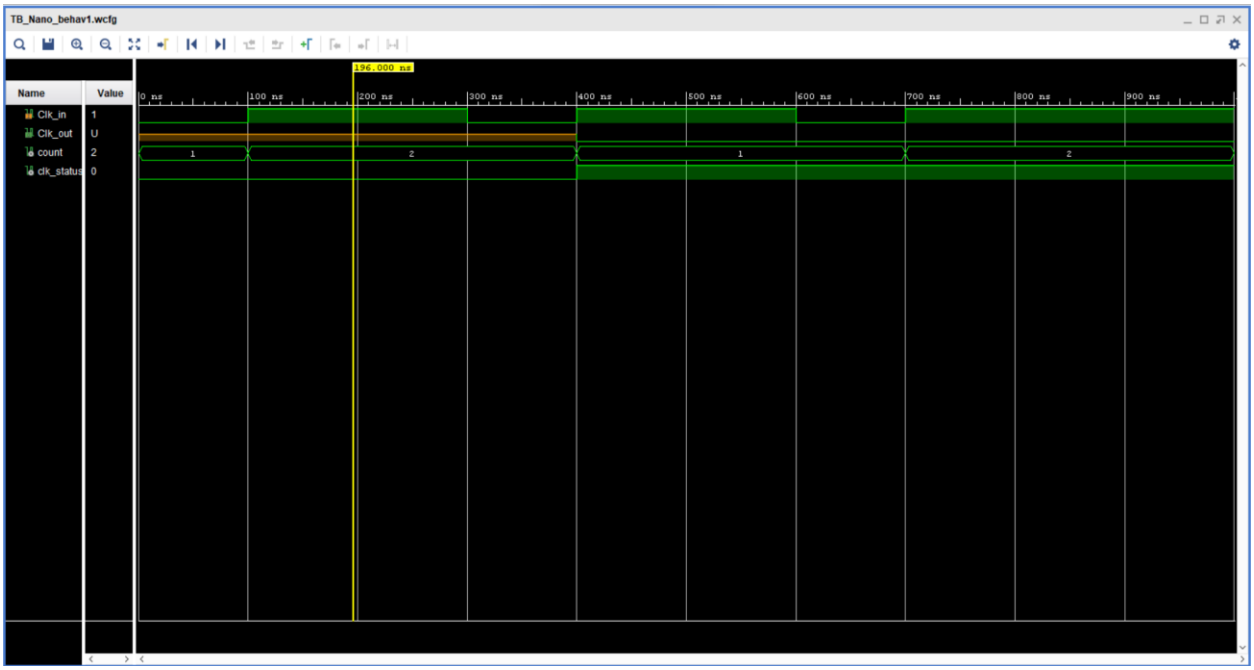
ROM



Nano Processor



Slow Clock



Conclusion

- Building a k-way n-bit multiplexer (MUX): It is possible to construct a k-way n-bit MUX by combining n individual k-to-1 MUXs. This allows for selecting one of k inputs based on the control signals.

- Handling larger arithmetic operations: To perform larger arithmetic operations, such as multiplication or division, it is necessary to utilize larger buses and registers. Increasing the width of the data buses and expanding the size of the registers enables handling larger numbers and more extensive computations.

- Subtraction using 2's complement: Subtraction can be achieved by adding the 2's complement of the number to be subtracted. By taking the 2's complement, the subtraction operation is effectively transformed into an addition operation.

- Expanding the instruction set: The instruction set can be expanded by increasing the size of the instruction bus. This allows for the inclusion of additional instructions to perform more complex operations and provide greater functionality to the nano processor.

- Improving instruction count and functionality: The number of instructions can be increased by expanding the size of the program ROM and program counter. This allows for a larger program memory and enables the execution of more instructions, leading to enhanced functionality.

- Defining a negative flag: A negative flag can be defined by checking the Most Significant Bit (MSB) of a selected register. By examining the MSB, the processor can determine if the value stored in the register is negative.

- Challenges and suggestions for improvement: The project faced time limitations, but there were suggestions for improvement, including introducing new instructions (such as MUL, DIV, INC, CLR), extending the register size and bank, and implementing the remaining components (like DIV and port mapping).

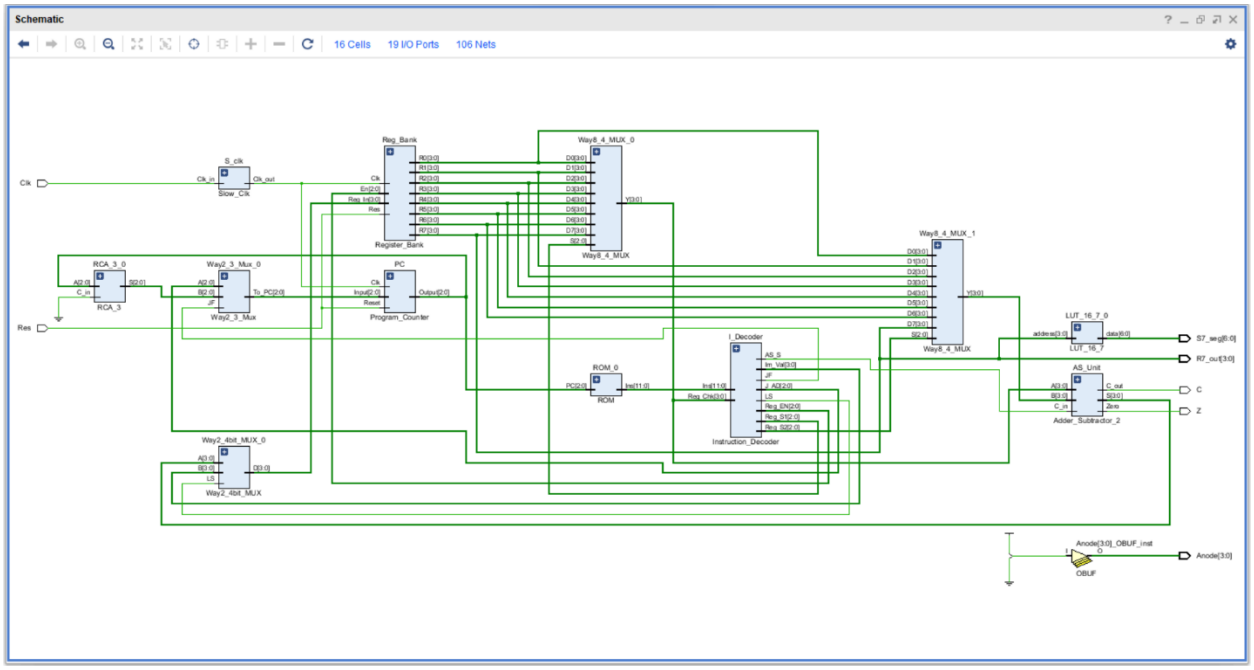
- Overall, the project successfully demonstrated the implementation of a nano processor capable of executing simple assembly instructions.

Individual Contribution

Team member	Contribution
Hana A.N.F	4-bit Add/Subtract unit, 3-bit adder, Register Bank Time spent= >1 day
Jayathilake. N.C.	. 3-bit Program Counter (PC), k-way b-bit multiplexers, Program ROM Time spent=> 1 day

Instruction decoder, report and Nano Processor Design were done as a group.

Schematic design



Synthesis report

```
#-----------------------------------------------------------
# Vivado v2018.1 (64-bit)
# SW Build 2188600 on Wed Apr  4 18:40:38 MDT 2018
# IP Build 2185939 on Wed Apr  4 20:55:05 MDT 2018
# Start of session at: Sun Jun 11 21:10:46 2023
# Process ID: 2324
# Current directory: D:/Downloads/Lab10/project_11/project_11.runs/synth_1
# Command line: vivado.exe-log Nano.vds-product Vivado-mode batch-messageDb vivado.pb-notrace-
source Nano.tcl
# Log file: D:/Downloads/Lab10/project_11/project_11.runs/synth_1/Nano.vds
# Journal file: D:/Downloads/Lab10/project_11/project_11.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source Nano.tcl-notrace
Command: synth_design-top Nano-part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 3588
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 383.566 ;
gain = 97.543
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'Nano'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:44]
INFO: [Synth 8-3491] module 'Way2_4bit_MUX' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_M
UX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:34' bound to instance
'Way2_4bit_MUX_0' of component 'Way2_4bit_MUX'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:149]
INFO: [Synth 8-638] synthesizing module 'Way2_4bit_MUX'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_M
UX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:41]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance
'MUX_2_to_1_0' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_M
UX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:50]
INFO: [Synth 8-638] synthesizing module 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:40]
```

INFO: [Synth 8-256] done synthesizing module 'MUX_2to1' (1#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:40]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance 'MUX_2_to_1_1' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_MUX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:58]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance 'MUX_2_to_1_2' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_MUX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:65]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance 'MUX_2_to_1_3' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_MUX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:72]
INFO: [Synth 8-256] done synthesizing module 'Way2_4bit_MUX' (2#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2Way_4bit_MUX/2Way_4bit_MUX.srcs/sources_1/new/Way2_4bit_MUX.vhd:41]
INFO: [Synth 8-3491] module 'Register_Bank' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:34' bound to instance 'Reg_Bank' of component 'Register_Bank'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:155]
INFO: [Synth 8-638] synthesizing module 'Register_Bank'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:49]
INFO: [Synth 8-3491] module 'Decoder_3_to_8' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:34' bound to instance 'Decoder_3_to_8_1' of component 'Decoder_3_to_8'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:66]
INFO: [Synth 8-638] synthesizing module 'Decoder_3_to_8'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:40]
INFO: [Synth 8-3491] module 'Decoder_2_to_4' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:34' bound to instance 'Decoder_2_to_4_0' of component 'Decoder_2_to_4'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:52]
INFO: [Synth 8-638] synthesizing module 'Decoder_2_to_4'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:41]
INFO: [Synth 8-256] done synthesizing module 'Decoder_2_to_4' (3#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:41]

INFO: [Synth 8-3491] module 'Decoder_2_to_4' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_2_to_4.vhd:34' bound to instance 'Decoder_2_to_4_1' of component 'Decoder_2_to_4' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:57]
INFO: [Synth 8-256] done synthesizing module 'Decoder_3_to_8' (4#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:40]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_0' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:72]
INFO: [Synth 8-638] synthesizing module 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'Register_4_bit' (5#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:42]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_1' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:80]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_2' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:88]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_3' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:96]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_4' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:104]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_5' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:112]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_6' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:120]
INFO: [Synth 8-3491] module 'Register_4_bit' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_4_bit.vhd:34' bound to instance 'Register_4_bit_7' of component 'Register_4_bit' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:128]
INFO: [Synth 8-256] done synthesizing module 'Register_Bank' (6#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Register_Bank.vhd:49]

INFO: [Synth 8-3491] module 'Adder_Subtractor_2' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:34' bound to instance 'AS_Unit' of component 'Adder_Subtractor_2' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:169]
INFO: [Synth 8-638] synthesizing module 'Adder_Subtractor_2' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:43]
INFO: [Synth 8-3491] module 'FA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA0' of component 'FA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:60]
INFO: [Synth 8-638] synthesizing module 'FA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:42]
INFO: [Synth 8-3491] module 'HA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/HA.vhd:34' bound to instance 'HA_0' of component 'HA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:56]
INFO: [Synth 8-638] synthesizing module 'HA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/HA.vhd:41]
INFO: [Synth 8-256] done synthesizing module 'HA' (7#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/HA.vhd:41]
INFO: [Synth 8-3491] module 'HA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/HA.vhd:34' bound to instance 'HA_1' of component 'HA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:62]
INFO: [Synth 8-256] done synthesizing module 'FA' (8#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:42]
INFO: [Synth 8-3491] module 'FA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA1' of component 'FA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:68]
INFO: [Synth 8-3491] module 'FA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA2' of component 'FA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:76]
INFO: [Synth 8-3491] module 'FA' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance 'FA3' of component 'FA' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:84]
INFO: [Synth 8-256] done synthesizing module 'Adder_Subtractor_2' (9#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Adder_Subtractor_2.vhd:43]
INFO: [Synth 8-3491] module 'Way8_4_MUX' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:34' bound to instance 'Way8_4_MUX_0'

of component 'Way8_4_MUX'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:177]
INFO: [Synth 8-638] synthesizing module 'Way8_4_MUX'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:47]
INFO: [Synth 8-3491] module 'Mux_8_to_1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:34' bound to instance 'Mux_8_to_1_0' of component 'Mux_8_to_1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:57]
INFO: [Synth 8-638] synthesizing module 'Mux_8_to_1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:41]
INFO: [Synth 8-3491] module 'Decoder_3_to_8' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Decoder_3_to_8.vhd:34'
bound to instance 'Decoder_3_to_8_0' of component 'Decoder_3_to_8'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:54]
INFO: [Synth 8-256] done synthesizing module 'Mux_8_to_1' (10#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:41]
INFO: [Synth 8-3491] module 'Mux_8_to_1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:34' bound to instance 'Mux_8_to_1_1' of component 'Mux_8_to_1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:71]
INFO: [Synth 8-3491] module 'Mux_8_to_1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:34' bound to instance 'Mux_8_to_1_2' of component 'Mux_8_to_1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:85]
INFO: [Synth 8-3491] module 'Mux_8_to_1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab_4_new1/Lab_4.srcs/sources_1/new/Mux_8_to_1.vhd:34' bound to instance 'Mux_8_to_1_3' of component 'Mux_8_to_1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:99]
INFO: [Synth 8-256] done synthesizing module 'Way8_4_MUX' (11#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:47]
INFO: [Synth 8-3491] module 'Way8_4_MUX' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Way_8_4bit_Mux/Way_8_4bit_Mux.srcs/sources_1/new/Way8_4_MUX.vhd:34' bound to instance 'Way8_4_MUX_1'
of component 'Way8_4_MUX'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:189]

INFO: [Synth 8-3491] module 'RCA_3' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:34' bound to instance
'RCA_3_0' of component 'RCA_3'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:201]
INFO: [Synth 8-638] synthesizing module 'RCA_3'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:42]
INFO: [Synth 8-3491] module 'FA' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance
'FA_0' of component 'FA'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:54]
INFO: [Synth 8-3491] module 'FA' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance
'FA_1' of component 'FA'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:62]
INFO: [Synth 8-3491] module 'FA' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/FA.vhd:34' bound to instance
'FA_2' of component 'FA'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:70]
INFO: [Synth 8-256] done synthesizing module 'RCA_3' (12#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/RCA_3.vhd:42]
INFO: [Synth 8-3491] module 'Way2_3_Mux' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:34' bound to instance
'Way2_3_Mux_0' of component 'Way2_3_Mux'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:207]
INFO: [Synth 8-638] synthesizing module 'Way2_3_Mux'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:41]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance
'MUX_2_1_0' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:49]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance
'MUX_2_1_1' of component 'MUX_2to1'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:56]
INFO: [Synth 8-3491] module 'MUX_2to1' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX
/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/MUX_2to1.vhd:34' bound to instance
'MUX_2_1_2' of component 'MUX_2to1'

[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:63]
INFO: [Synth 8-256] done synthesizing module 'Way2_3_Mux' (13#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/2way3bitMUX/Way2_bit3_MUX/Way2_bit3_MUX.srcs/sources_1/new/Way2_3_Mux.vhd:41]
INFO: [Synth 8-3491] module 'LUT_16_7' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab7_new/Lab7_new.srcs/sources_1/new/LUT_16_7.vhd:35' bound to instance 'LUT_16_7_0' of component 'LUT_16_7' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:213]
INFO: [Synth 8-638] synthesizing module 'LUT_16_7' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab7_new/Lab7_new.srcs/sources_1/new/LUT_16_7.vhd:40]
INFO: [Synth 8-256] done synthesizing module 'LUT_16_7' (14#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab7_new/Lab7_new.srcs/sources_1/new/LUT_16_7.vhd:40]
INFO: [Synth 8-3491] module 'Program_Counter' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:34' bound to instance 'PC' of component 'Program_Counter' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:218]
INFO: [Synth 8-638] synthesizing module 'Program_Counter' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:41]
INFO: [Synth 8-3491] module 'D_FF' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:34' bound to instance 'D_FF_0' of component 'D_FF' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:50]
INFO: [Synth 8-638] synthesizing module 'D_FF' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:42]
INFO: [Synth 8-256] done synthesizing module 'D_FF' (15#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:42]
INFO: [Synth 8-3491] module 'D_FF' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:34' bound to instance 'D_FF_1' of component 'D_FF' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:57]
INFO: [Synth 8-3491] module 'D_FF' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:34' bound to instance 'D_FF_2' of component 'D_FF' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:64]
INFO: [Synth 8-256] done synthesizing module 'Program_Counter' (16#1) [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/new/Program_Counter.vhd:41]
INFO: [Synth 8-3491] module 'Instruction_Decoder' declared at 'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:34' bound to

```
instance 'I_Decoder' of component 'Instruction_Decoder'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:225]
INFO: [Synth 8-638] synthesizing module 'Instruction_Decoder'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:47]
INFO: [Synth 8-256] done synthesizing module 'Instruction_Decoder' (17#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:47]
INFO: [Synth 8-3491] module 'ROM' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Program_RO
M/Program_ROM.srcs/sources_1/new/ROM.vhd:35' bound to instance 'ROM_0' of component 'ROM'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:238]
INFO: [Synth 8-638] synthesizing module 'ROM'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Program_RO
M/Program_ROM.srcs/sources_1/new/ROM.vhd:40]
INFO: [Synth 8-256] done synthesizing module 'ROM' (18#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/nanoprocessor/Program_RO
M/Program_ROM.srcs/sources_1/new/ROM.vhd:40]
INFO: [Synth 8-3491] module 'Slow_Clk' declared at
'D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5  _ new 1/Lab
5.srcs/sources_1/new/Slow_Clk.vhd:34' bound to instance 'S_clk' of component 'Slow_Clk'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:243]
INFO: [Synth 8-638] synthesizing module 'Slow_Clk'
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5  _ new 1/Lab
5.srcs/sources_1/new/Slow_Clk.vhd:39]
INFO: [Synth 8-256] done synthesizing module 'Slow_Clk' (19#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5  _ new 1/Lab
5.srcs/sources_1/new/Slow_Clk.vhd:39]
INFO: [Synth 8-256] done synthesizing module 'Nano' (20#1)
[D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Nano.vhd:44]
WARNING: [Synth 8-3917] design Nano has port Anode[3] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[2] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[1] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[0] driven by constant 0
WARNING: [Synth 8-3331] design RCA_3 has unconnected port C_in
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 439.672 ;
gain = 153.648
---------------------------------------------------------------------------------

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
```

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 439.672 ; gain = 153.648

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed = 00:00:05 . Memory (MB): peak = 439.672 ; gain = 153.648

INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [D:/Downloads/Lab10/project_11/project_11.srcs/constrs_1/imports/computer organization/Basys3Labs.xdc]
Finished Parsing XDC File [D:/Downloads/Lab10/project_11/project_11.srcs/constrs_1/imports/computer organization/Basys3Labs.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [D:/Downloads/Lab10/project_11/project_11.srcs/constrs_1/imports/computer organization/Basys3Labs.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/Nano_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/Nano_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 772.281 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:08 ; elapsed = 00:00:16 . Memory (MB): peak = 772.281 ; gain = 486.258

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:08 ; elapsed = 00:00:16 . Memory (MB): peak = 772.281 ; gain = 486.258

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:08 ; elapsed = 00:00:16 . Memory (MB): peak = 772.281 ; gain = 486.258

INFO: [Synth 8-5544] ROM "sevenSegment_ROM" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "JF" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "Im_Val" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "LS" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "AS_S" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "ROM" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
INFO: [Synth 8-5545] ROM "count" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "clk_status" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
WARNING: [Synth 8-327] inferring latch for variable 'AS_S_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:90]
WARNING: [Synth 8-327] inferring latch for variable 'LS_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:83]
WARNING: [Synth 8-327] inferring latch for variable 'Reg_S1_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:91]
WARNING: [Synth 8-327] inferring latch for variable 'Reg_S2_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:92]
WARNING: [Synth 8-327] inferring latch for variable 'J_AD_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:109]
WARNING: [Synth 8-327] inferring latch for variable 'Im_Val_reg' [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/new/Instruction_Decoder.vhd:81]

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:08 ; elapsed = 00:00:16 . Memory (MB): peak = 772.281 ; gain = 486.258

Report RTL Partitions:

```
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

Start RTL Component Statistics

Detailed RTL Component Info :

```
+---Adders :
            2 Input     32 Bit      Adders := 1
+---XORs :
            2 Input      1 Bit       XORs := 18
+---Registers :
                       32 Bit    Registers := 1
                        4 Bit    Registers := 8
                        1 Bit    Registers := 8
+---Muxes :
            2 Input     32 Bit       Muxes := 1
            9 Input     12 Bit       Muxes := 1
           17 Input      7 Bit       Muxes := 1
            4 Input      3 Bit       Muxes := 1
            2 Input      3 Bit       Muxes := 3
            2 Input      1 Bit       Muxes := 12
            4 Input      1 Bit       Muxes := 1
            5 Input      1 Bit       Muxes := 2
            3 Input      1 Bit       Muxes := 1
```

Finished RTL Component Statistics

Start RTL Hierarchical Component Statistics

Hierarchical RTL Component report

Module Register_4_bit

Detailed RTL Component Info :

```
+---Registers :
                        4 Bit    Registers := 1
```

Module HA

Detailed RTL Component Info :

```
+---XORs :
            2 Input      1 Bit       XORs := 1
```

Module Adder_Subtractor_2

Detailed RTL Component Info :

```
+---XORs :
```

```
            2 Input      1 Bit        XORs := 4
Module LUT_16_7
Detailed RTL Component Info :
+---Muxes :
           17 Input      7 Bit       Muxes := 1
Module D_FF
Detailed RTL Component Info :
+---Registers :
                      1 Bit    Registers := 2
Module Instruction_Decoder
Detailed RTL Component Info :
+---Muxes :
            4 Input      3 Bit       Muxes := 1
            2 Input      3 Bit       Muxes := 3
            2 Input      1 Bit       Muxes := 11
            4 Input      1 Bit       Muxes := 1
            5 Input      1 Bit       Muxes := 2
            3 Input      1 Bit       Muxes := 1
Module ROM
Detailed RTL Component Info :
+---Muxes :
            9 Input     12 Bit       Muxes := 1
Module Slow_Clk
Detailed RTL Component Info :
+---Adders :
            2 Input     32 Bit      Adders := 1
+---Registers :
                    32 Bit    Registers := 1
                     1 Bit    Registers := 2
+---Muxes :
            2 Input     32 Bit       Muxes := 1
            2 Input      1 Bit       Muxes := 1
---------------------------------------------------------------------------------
Finished RTL Hierarchical Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
```

Start Cross Boundary and Area Optimization

Warning: Parallel synthesis criteria is not met
WARNING: [Synth 8-6014] Unused sequential element PC/D_FF_0/Qbar_reg was removed. [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:49]
WARNING: [Synth 8-6014] Unused sequential element PC/D_FF_1/Qbar_reg was removed. [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:49]
WARNING: [Synth 8-6014] Unused sequential element PC/D_FF_2/Qbar_reg was removed. [D:/Downloads/Lab10/project_11/project_11.srcs/sources_1/imports/DELL/Lab 5 _ new 1/Lab 5.srcs/sources_1/new/D_FF.vhd:49]
INFO: [Synth 8-5545] ROM "S_clk/count" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
INFO: [Synth 8-5545] ROM "S_clk/clk_status" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
WARNING: [Synth 8-3917] design Nano has port Anode[3] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[2] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[1] driven by constant 1
WARNING: [Synth 8-3917] design Nano has port Anode[0] driven by constant 0
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\I_Decoder/Im_Val_reg[3])
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_0/Q_reg[3]' (FDRE) to 'Reg_Bank/Register_4_bit_0/Q_reg[2]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_0/Q_reg[2]' (FDRE) to 'Reg_Bank/Register_4_bit_0/Q_reg[1]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_0/Q_reg[1]' (FDRE) to 'Reg_Bank/Register_4_bit_0/Q_reg[0]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Reg_Bank/Register_4_bit_0/Q_reg[0])
WARNING: [Synth 8-3332] Sequential element (I_Decoder/Im_Val_reg[3]) is unused and will be removed from module Nano.
WARNING: [Synth 8-3332] Sequential element (Reg_Bank/Register_4_bit_0/Q_reg[0]) is unused and will be removed from module Nano.

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:09 ; elapsed = 00:00:17 . Memory (MB): peak = 772.281 ; gain = 486.258

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

```
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:13 ; elapsed = 00:00:24 . Memory (MB):
peak = 772.281 ; gain = 486.258
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak =
785.605 ; gain = 499.582
---------------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_4/Q_reg[1]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[1]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_4/Q_reg[0]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[0]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_4/Q_reg[3]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[3]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_4/Q_reg[2]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[2]'
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_6/Q_reg[1]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[1]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\Reg_Bank/Register_4_bit_5/Q_reg[1] )
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_6/Q_reg[0]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[0]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\Reg_Bank/Register_4_bit_5/Q_reg[0] )
INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_6/Q_reg[3]' (FDRE) to
'Reg_Bank/Register_4_bit_5/Q_reg[3]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(\Reg_Bank/Register_4_bit_5/Q_reg[3] )
```

INFO: [Synth 8-3886] merging instance 'Reg_Bank/Register_4_bit_6/Q_reg[2]' (FDRE) to 'Reg_Bank/Register_4_bit_5/Q_reg[2]'
INFO: [Synth 8-3333] propagating constant 0 across sequential element (\Reg_Bank/Register_4_bit_5/Q_reg[2])
WARNING: [Synth 8-3332] Sequential element (Reg_Bank/Register_4_bit_5/Q_reg[1]) is unused and will be removed from module Nano.
WARNING: [Synth 8-3332] Sequential element (Reg_Bank/Register_4_bit_5/Q_reg[0]) is unused and will be removed from module Nano.
WARNING: [Synth 8-3332] Sequential element (Reg_Bank/Register_4_bit_5/Q_reg[3]) is unused and will be removed from module Nano.
WARNING: [Synth 8-3332] Sequential element (Reg_Bank/Register_4_bit_5/Q_reg[2]) is unused and will be removed from module Nano.

Finished Technology Mapping : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+

```
|     |Item             |Errors |Warnings |Status |Description       |
+------+-----------------+-------+---------+-------+------------------+
|1    |multi_driven_nets |     0|       0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+------------------+
```

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Report RTL Partitions:

```
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
```

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Start Writing Synthesis Report

Report BlackBoxes:

	BlackBox name	Instances

Report Cell Usage:

	Cell	Count
1	BUFG	1
2	CARRY4	8
3	LUT1	2
4	LUT3	18
5	LUT4	14
6	LUT5	14
7	LUT6	18
8	FDRE	53
9	LD	13
10	LDCP	1
11	IBUF	2
12	OBUF	17

Report Instance Areas:

	Instance	Module	Cells
1	top		161
2	I_Decoder	Instruction_Decoder	35
3	PC	Program_Counter	21
4	D_FF_0	D_FF	6
5	D_FF_1	D_FF_3	9
6	D_FF_2	D_FF_4	6
7	Reg_Bank	Register_Bank	31
8	Register_4_bit_1	Register_4_bit	4
9	Register_4_bit_2	Register_4_bit_0	12
10	Register_4_bit_3	Register_4_bit_1	4
11	Register_4_bit_7	Register_4_bit_2	11

```
|12   | S_clk           |Slow_Clk          |   54|
+-----+-----------------+------------------+-----+
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582

Synthesis finished with 0 errors, 0 critical warnings and 19 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:07 ; elapsed = 00:00:19 . Memory (MB): peak = 785.605 ; gain = 166.973
Synthesis Optimization Complete : Time (s): cpu = 00:00:13 ; elapsed = 00:00:25 . Memory (MB): peak = 785.605 ; gain = 499.582
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 24 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 1 inverter(s) to 3 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 14 instances were transformed.
  LD => LDCE: 10 instances
  LD => LDCE (inverted pins: G): 3 instances
  LDCP => LDCP (GND, LUT3, LUT3, LDCE, VCC): 1 instances

INFO: [Common 17-83] Releasing license: Synthesis
126 Infos, 24 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:15 ; elapsed = 00:00:28 . Memory (MB): peak = 785.605 ; gain = 511.488
INFO: [Common 17-1381] The checkpoint 'D:/Downloads/Lab10/project_11/project_11.runs/synth_1/Nano.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file Nano_utilization_synth.rpt -pb Nano_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.016 . Memory (MB): peak = 785.605 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Sun Jun 11 21:11:19 2023...