

$$\begin{aligned}
 1) \quad F &= xy'z + x'y'z + w'xy + wx'y + wxy \\
 &= xy'z(z+x') + xy(w'+w) + wx'y \\
 &= xy'z + xy + wx'y
 \end{aligned}$$

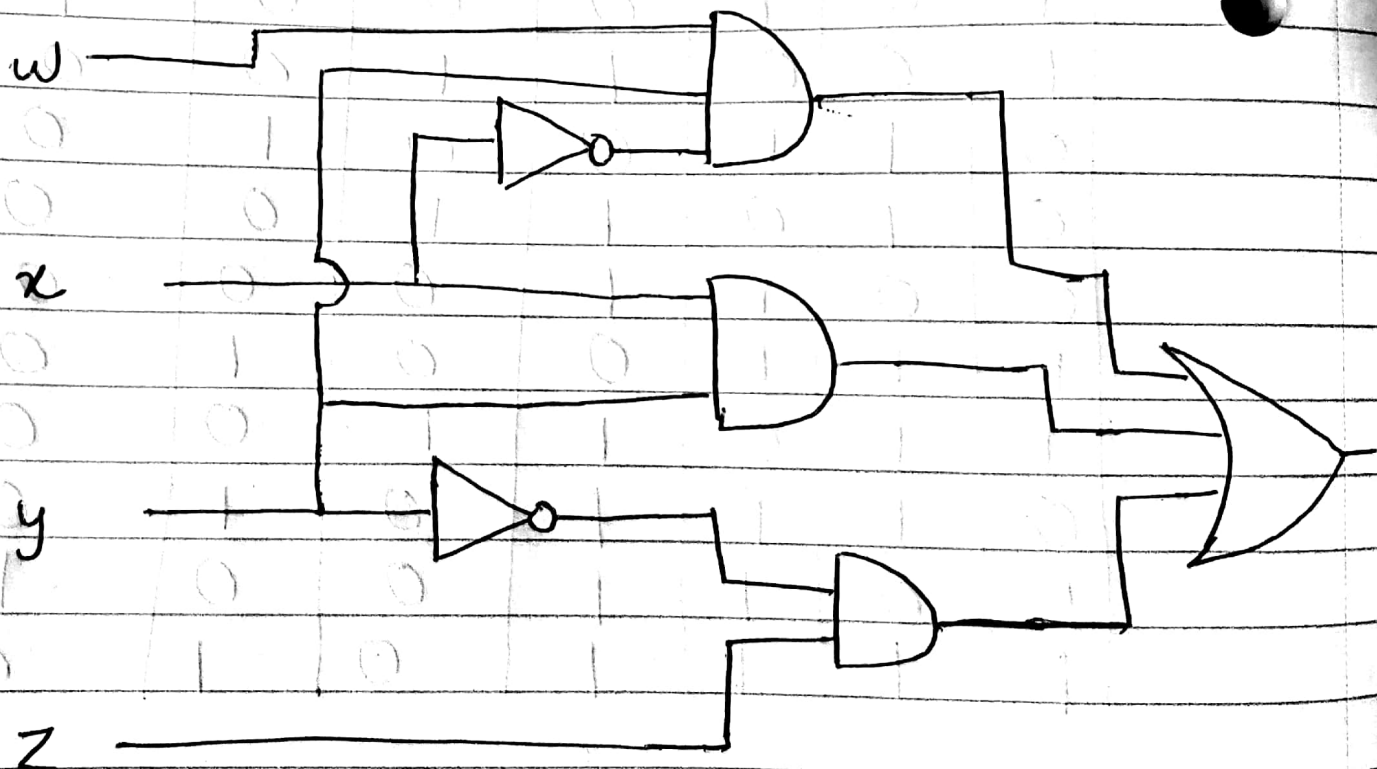
a)

w	x	y	z	y'z	xy	wx'y	F
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0
1	0	1	0	0	0	1	1
1	0	0	1	1	0	0	1
0	1	1	0	0	1	0	1
0	1	0	1	1	0	0	1
0	0	1	1	0	0	0	0
1	1	1	0	0	1	0	1
1	1	0	1	1	0	0	1
0	1	1	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	1	1	0	1	0	1

K-map

w \ yz	00	01	11	10
00		1		
01		1	1	1
11		1	1	1
10		1	1	1

b)



2a) $2k \times 16$
 ~~$= 2 \times 10$~~ $= 2^1 \times 2^{10} \times 16$

$(10+1) = 11$ is the address line
 $(10+1) + 16 = 27$ is the I/O line

b) $64k \times 8$
 $= 2^6 \times 2^{10} \times 8$

Address line : $(6+10) = 16$

I/O line : $(6+10)+8 = 24$

c) $16M \times 32$
 $= 2^4 \times 2^{20} \times 32$

Address line = $(4+20) = 24$

I/O line = $(4+20+32) = 56$

d) $4G \times 64$
 $= 2^2 \times 2^{30} \times 64$

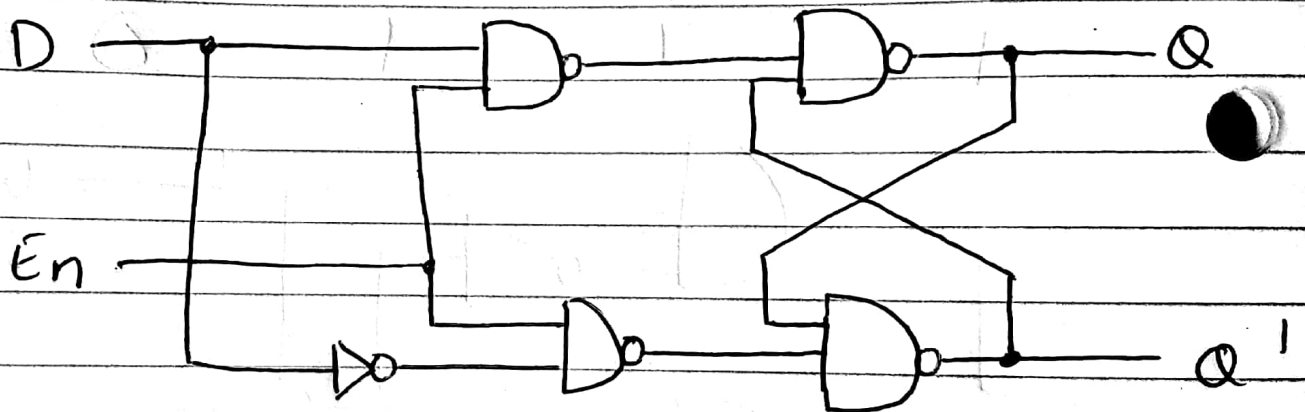
Address line = $(2+30) = 32$

I/O line = $(2+30+64) = 96$

3) Truth table for D flip-flop

Clock (C)	Input (En)	Output (Q)
0	X	0
1	0	0
1	1	1

Logic diagram for D flip flop



JK flip flop

Q	J	K	Q'
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

JK flip flop

Q	J	K	Q'
0	0	0	0
0	0	1	0
1	0	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0