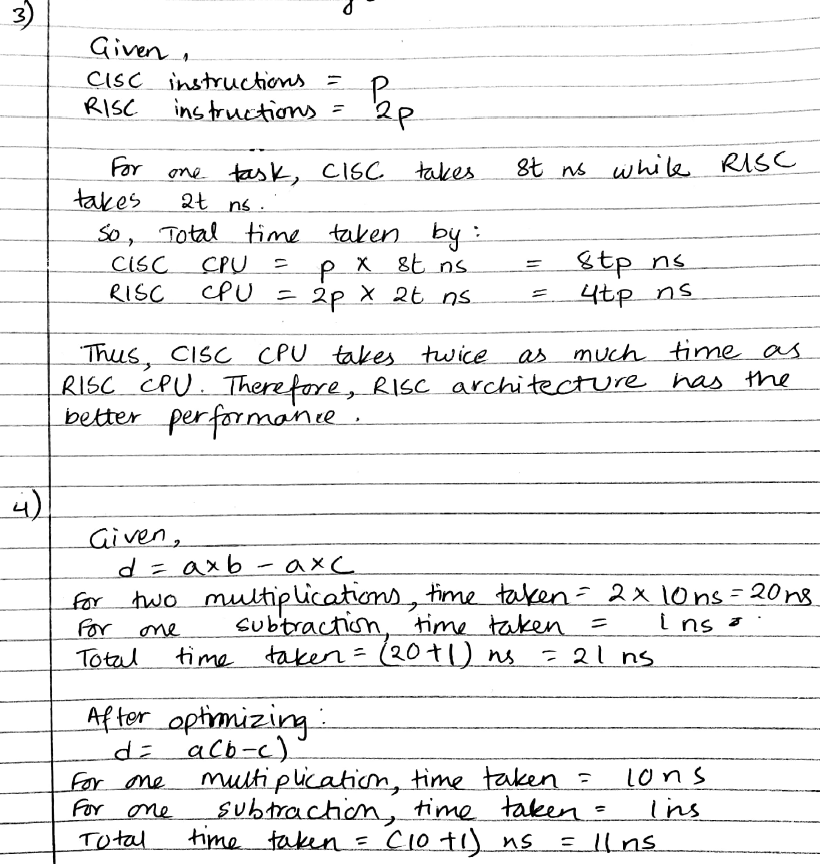
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Assignment 2



**MIPS**

MIPS, short for Microprocessor without Interlocked Pipelined Stages, is a RISC(Reduced Instruction Set Computer) ISA(Instruction Set Architecture). It was developed by MIPS Computer Systems. It is a very simple and scalable RISC architecture. The main features of MIPS is large number of registers, large number and characters of instruction, and visible pipeline delay slots. These features have allowed MIPS to provide the best performance. The MIPS architecture is one of the most widely supported of all processor architectures, with a broad infrastructure of standard tools, software and services to help ensure rapid, reliable, cost effective development. Microprocessor developers who want maximum flexibility from processor IP have a solution in the MIPS architecture.

During the 80s, microprocessors were turning out towards more complex builds and mechanisms. Additionally, 32-bit designs were already on the lime light by then. For the usage of such designs, John Hennessey and his team launched a company named MIPS Computer Systems to start producing MIPS chips. John Hennessey and a bunch of graduate students at Stanford University decided to think about the way the processors were working during that time. Their numerous hours of thinking and analyzing contributed in the production of MIPS. In 1985, the company produced their first ever product R2000 and gradually produced a second generation processor R3000 in 1988. Today, there are multiple versions of MIPS viz. MIPS I, MIPS II, MIPS III, MIPS IV, MIPS V, MIPS32 and MIPS64. The 64-bit versions were produced only on the later part of the history. Today the MIPS Family has been popularly used throughout the world. The newer versions R10000, R12000, R14000 and R16000 have even more space for cache and greater speeds DRAM interfaces.

The reason for MIPS to gain so much popularity is that the fact that the Stanford research group involved in the brainstorming for MIPS had a very high level knowledge about compilers. Their strong background helped them to create a processor whose aim was to function by lowering the compiler level to the hardware level. The concept opposed the design philosophy (raising of hardware to software level) of that time. This shifted the traditional way of creating processors to the kind that MIPS uses. The MIPS team also had to adopt a new design philosophy alongside developing and selling their new product. MIPS processor implemented a smaller and simpler instruction set where each instruction included in the chip design ran just in a single clock cycle. MIPS processor was built on a new technique called “pipelining” which allowed the instructions to process taking lesser time and hence, much more efficiently.

The first MIPS processor used total of 32 registers. Each of those registers are 32 bits wide a bit pattern which is commonly referred to as a word. The instruction set for MIPS comprises of more than 100 instructions out of which majority are arithmetic instructions. There are total of 21 arithmetic instructions, eight each of logical and bit manipulation instructions, 15 load instructions, and ten store instructions and so on. Given is an example of MIPS instructions: add $s1, $s3, $s4. This instructs the processor to subtract add the values in register 3 and 4, and store the sum in register 1.

MIPS could be a secluded engineering supporting up to four coprocessors (CP0/1/2/3). In MIPS wording, CP0 is the Framework Control Coprocessor (an fundamental portion of the processor that's implementation-defined in MIPS I–V), CP1 is an discretionary floating-point unit (FPU) and CP2/3 are discretionary implementation-defined coprocessors (MIPS III expelled CP3 and reused its opcodes for other purposes). For case, within the PlayStation video diversion comfort, CP2 is the Geometry Change Motor (GTE), which quickens the preparing of geometry in 3D computer graphics.

The MIPS engineering has a few discretionary expansions. MIPS-3D which could be a straightforward set of floating-point SIMD informational committed to common 3D tasks, MDMX (MaDMaX) which could be a more broad numbers SIMD instruction set utilizing the 64-bit floating-point registers, MIPS16e which includes compression to the instruction stream to form programs take up less room, and MIPS MT, which includes multithreading capability. In In December 2018, Wave Computing, the new owner of the MIPS architecture (see [MIPS Technologies](https://en.wikipedia.org/wiki/MIPS_Technologies)), announced that MIPS ISA will be open-sourced in a program dubbed the MIPS Open initiative. The program being planned for 2019 is intended to open up access to the most recent versions of both the 32-bit and 64-bit designs making them available without any licensing or royalty fees as well as granting participants licenses to existing MIPS patents.

The most known usage of MIPS can be found in systems such as routers and residential gateways. At the beginning MIPS was used for general computing, but gradually, its usage began to expand the bracket. Many top technological companies such a as DEC (Digital Equipment Corporation), NEC, SiCortex, etc. started to use MIPS in extended manner. MIPS was being rapidly popular. The other popular usage of MIPS can be seen in gaming consoles such as PS2 (Play Station 2) and PSP (Play Station Portable). The popularity of MIPS led to extensively large production of MIPS. During the mid-90s, its production dominated the market. Out of random three RISC microprocessors chosen, one would be MIPS.

Work Cited

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