ESS 102 Digital Design Assignment 2

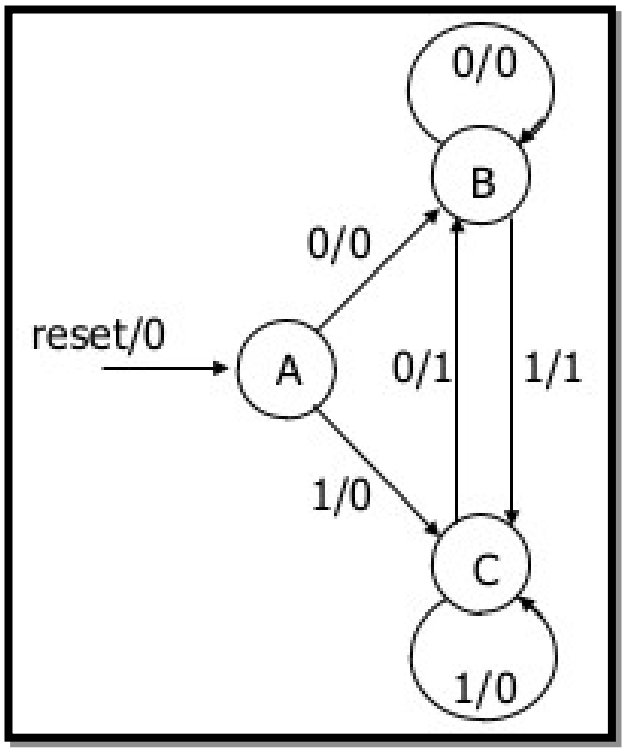
VERILOG Based Individual Assignment – 10 marks

Deadline – 17th February 2023, 11.59 pm

Q1. (Marks: 3 for code + 3 for testbench)

Write a Verilog code to **define the FSM** given in the diagram below. **Write a Testbench** for it which should test all the states and possible combinations.

For eg- 0/0 in the FSM means, input = 0 in that state and output=0



Q2. Debug and Complete codes (2 + 2 marks)

a. 1 verilog file of **ALU,** with errors, has been uploaded. You are required to debug the errors, and fix them. What to upload –

a Upload the erroneous code file with comments on how you corrected it.
b Upload the corrected code file which simulates.
c Upload the waveforms after simulating your corrected code.

b. An **incomplete half subtractor** code has been given. Complete the code as per the given comments. What to upload -

a. Upload completed verilog code of half subtractor.
b. Upload the waveforms for the half subtractor.

What to submit on LMS:

- Submit the code and testbench along with snapshot of waveforms.

- If you are getting an error and unable to get waveform, submit snapshot of error.
- Rename the individual Verilog files (.v) as: rollnumber1_filename.v. For e.g., IMT< >_filename.v
- Now, upload all these files (renamed Verilog, snapshot of waveforms etc.) as separate files in Verilog assignment link on LMS.
- **Do not submit vcd files**.
- Important - DO NOT COMPRESS THESE FILES INTO ZIP/TAR. UPLOAD THE FILES INDIVIDUALLY INTO THE LMS LINK.

All codes will go through Turnitin- for Plagiarism check. Codes which are similar, will get a zero for the entire assignment.