Assignment 1

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Q1)

i) Resource utilization report:

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	DSPs (90)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
N MAC_Operation	3.00%	2.89%	3.91%	2.88%	0.25%	1.11%	0.94%	6.25%	25.00%
dbg_hub (dbg_hub)	2.16%	1.78%	2.72%	2.04%	0.25%	0.00%	0.00%	3.13%	25.00%
dsp (dsp_macro_0)	0.00%	0.15%	0.21%	0.00%	0.00%	1.11%	0.00%	0.00%	0.00%
your_instance_name (vio_0)	0.84%	0.95%	1.12%	0.84%	0.00%	0.00%	0.00%	0.00%	0.00%

ii) Timing summary:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	26.036 ns	Worst Hold Slack (WHS):	0.068 ns	Worst Pulse Width Slack (WPWS):	15.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

iii) Dsp block mapping:

Q2)

i) Resource utilization report:

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
MAC_Operation	4.74%	3.17%	5.29%	4.63%	0.25%	0.94%	6.25%	25.00%
dbg_hub (dbg_hub)	2.16%	1.78%	2.75%	2.04%	0.25%	0.00%	3.13%	25.00%
dsp (dsp_macro_0)	1.75%	0.44%	1.51%	1.75%	0.00%	0.00%	0.00%	0.00%
your_instance_name (vio_0)	0.84%	0.95%	1.28%	0.84%	0.00%	0.00%	0.00%	0.00%

ii) Timing Summary

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	26.918 ns	Worst Hold Slack (WHS):	0.093 ns	Worst Pulse Width Slack (WPWS):	15.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

Observations:

- In task 1, we utilized a dedicated DSP block in the FPGA to handle the multiply-accumulate (MAC) operations, which resulted in better timing performance as indicated by a lower worst negative slack (WNS). This is because DSP blocks are optimized for such operations, allowing the design to achieve a higher operating frequency.
- In contrast, in task 2, the MAC operations were implemented using LUTs (Look-Up Tables), which are more general-purpose and not specifically tailored for MAC operations, leading to higher WNS and lower operational frequency.
- The resource utilization report further supports this observation, showing that the percentage of DSP usage is 0% in task 2, while task 1 indicates some level of DSP utilization.

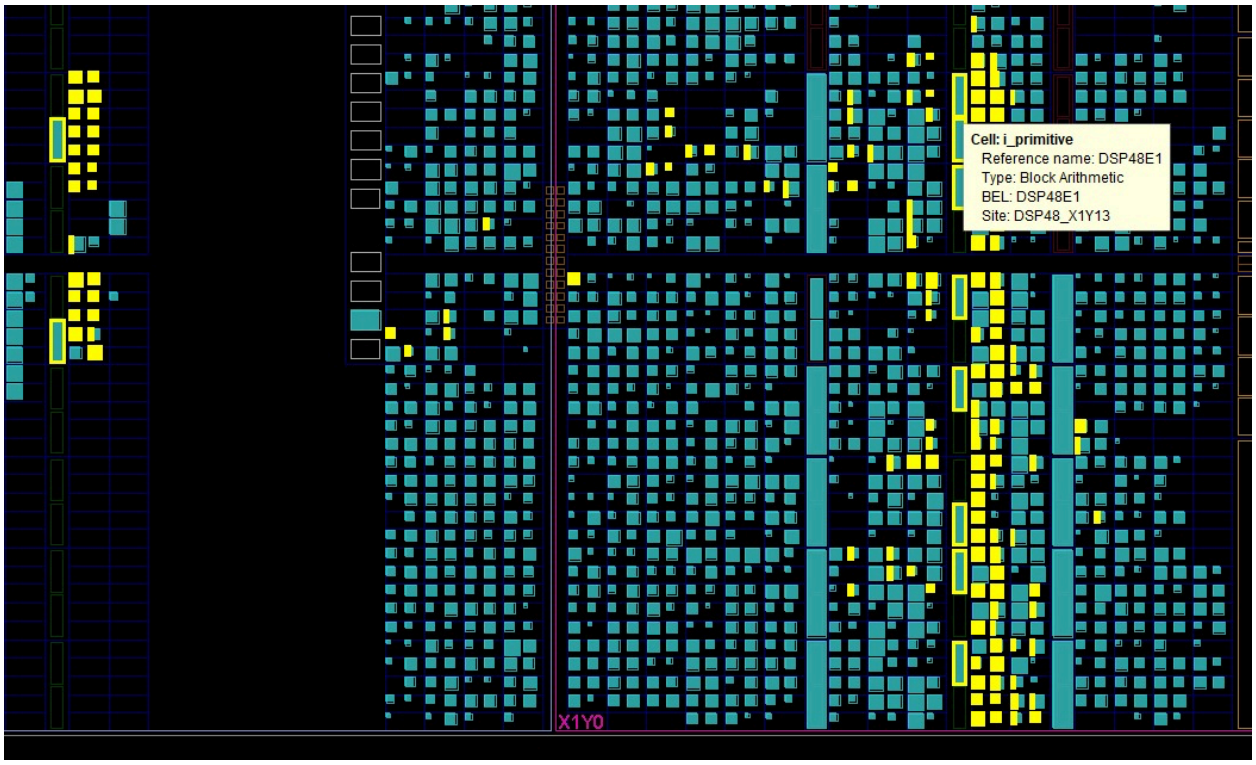
Q3)

Resource utilization report:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	DSPs (90)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
N MAC_Operations_Parallel	3317	5913	134	32	1532	2725	592	16	10	1	2	1
dbg_hub (dbg_hub)	449	741	0	0	233	425	24	0	0	0	1	1
dsp1 (dsp_macro_1)	0	64	0	0	14	0	0	0	1	0	0	0
dsp2 (dsp_macro_1_HD21)	0	64	0	0	15	0	0	0	1	0	0	0
dsp3 (dsp_macro_1_HD32)	0	64	0	0	15	0	0	0	1	0	0	0
dsp4 (dsp_macro_1_HD43)	0	64	0	0	15	0	0	0	1	0	0	0
dsp5 (dsp_macro_1_HD54)	0	64	0	0	17	0	0	0	1	0	0	0
dsp	0	64	0	0	15	0	0	0	1	0	0	0
dsp7 (dsp_macro_1_HD76)	0	64	0	0	22	0	0	0	1	0	0	0
dsp8 (dsp_macro_1_HD87)	0	64	0	0	20	0	0	0	1	0	0	0
dsp9 (dsp_macro_1_HD98)	0	64	0	0	16	0	0	0	1	0	0	0
dsp10 (dsp_macro_1_HD10)	0	64	0	0	15	0	0	0	1	0	0	0
mem0 (blk_mem_gen_0)	0	0	0	0	0	0	0	1.5	0	0	0	0
mem1 (blk_mem_gen_1)	0	0	0	0	0	0	0	1.5	0	0	0	0
mem2 (blk_mem_gen_2)	0	0	0	0	0	0	0	1.5	0	0	0	0
your_instance_name (ila_0)	2866	4530	134	32	1234	2298	568	11.5	0	0	0	0

- We can observe each DSP which we initialized is using dedicated DSP slice

DSP blocks mapping:



1) i) Maximum number of MACs: 90

Resource	Utilization	Available	Utilization %
LUT	3317	20800	15.95
LUTRAM	592	9600	6.17
FF	5913	41600	14.21
BRAM	16	50	32.00
DSP	10	90	11.11
IO	1	106	0.94

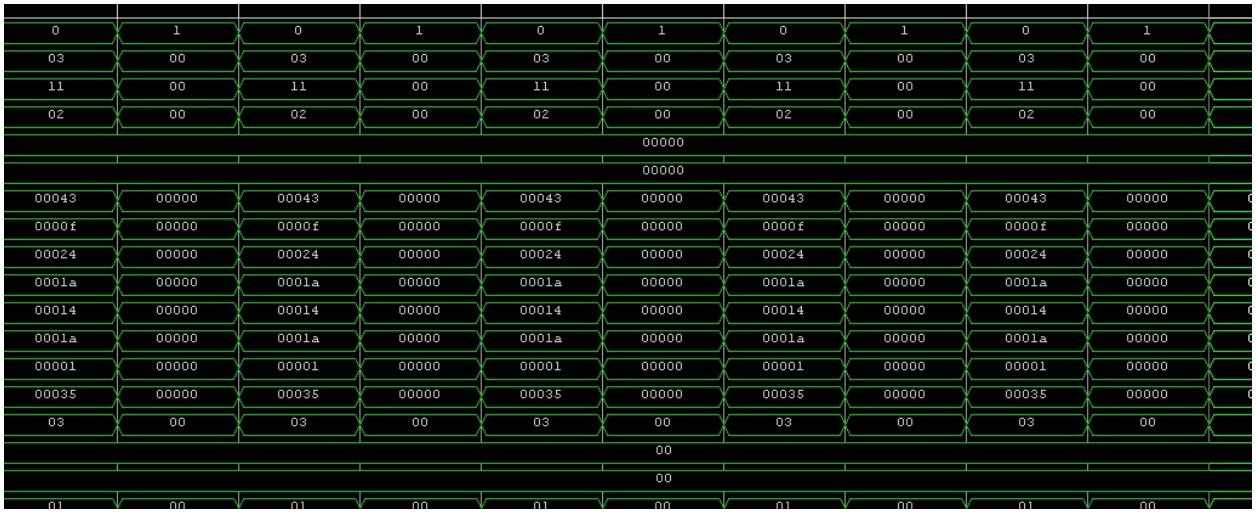
ii) Timing summary(positive time slack)

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	26.454 ns	Worst Hold Slack (WHS):	0.090 ns	Worst Pulse Width Slack (WPWS):	15.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

2) Throughput: number of MAC operations per second



Time period(T) = 10ns

- Each DSP takes 4 clock cycles for an operation

Calculations:

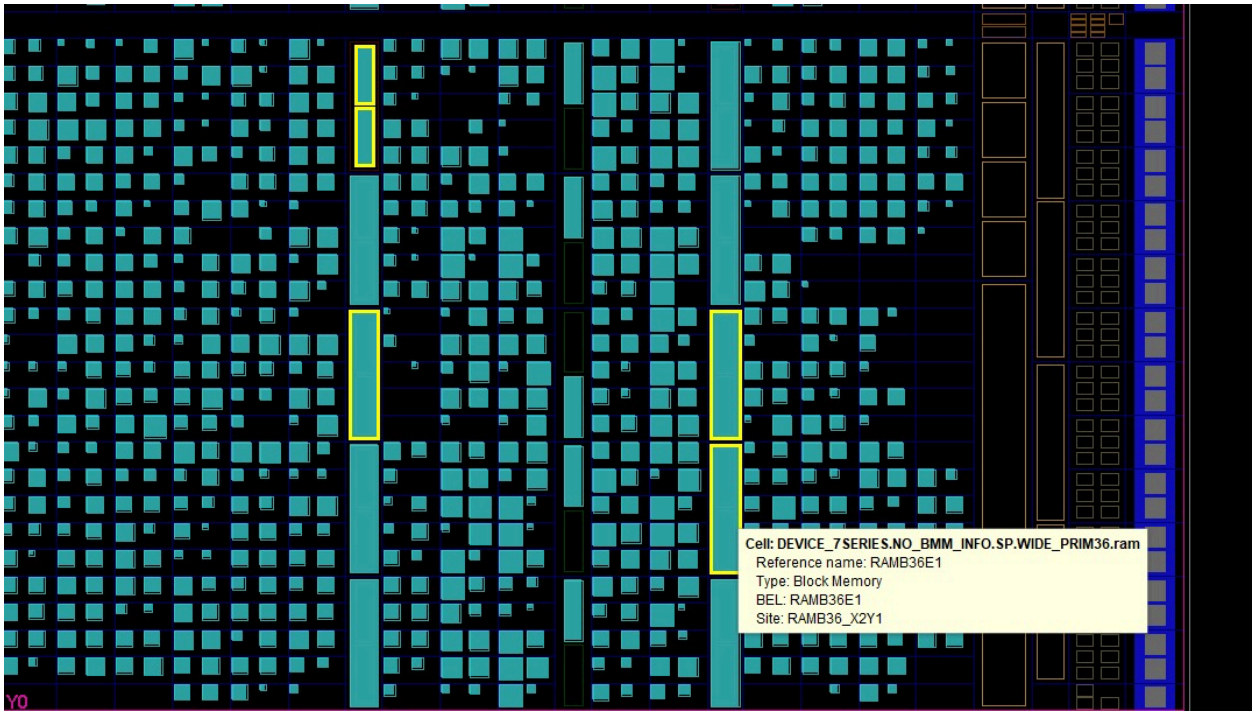
Delay for 1 MAC operation = 4T

Mac operations/sec = 1 / 4T sec (T = 10 x 10^-9 sec)

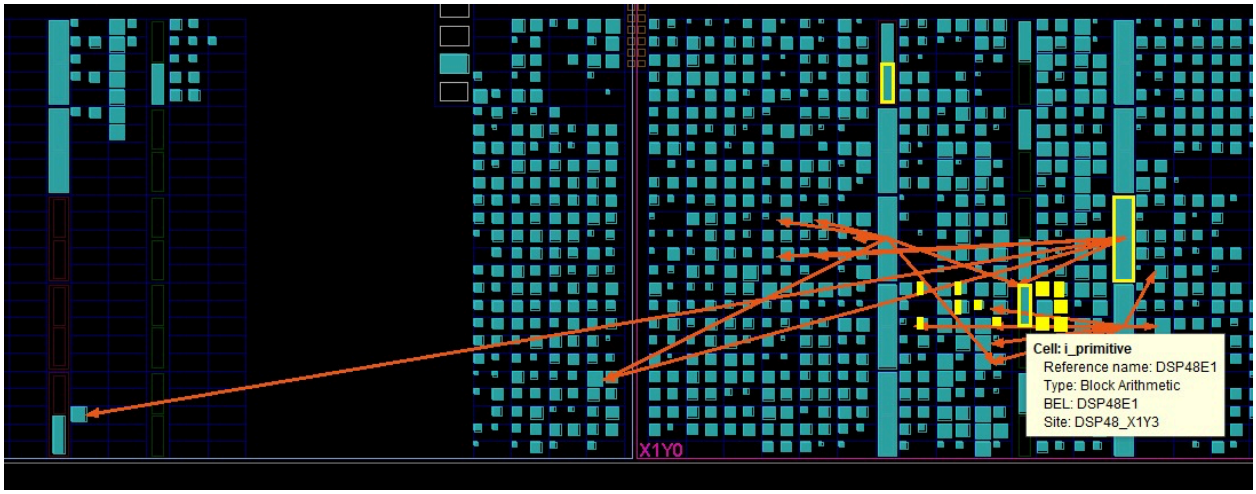
So Throughput for 10 MACs is 10 / 4T = 25 x 10^8 Operations per secs.

Q4)

i) Block ram location:



ii) Connection between MAC-DSP to the Block-RAM



iii) What is the wire-delay? How can you reduce the wire-delay?

- **Wire delay** is the time it takes for a signal to travel through the physical interconnections (wires) between components in a circuit, such as between logic elements, memory blocks, or DSP slices in an FPGA or SoC.
- It is caused by the resistance and capacitance of the wires, and it affects the overall timing of the circuit.
- It can be reduced by changing the pin constraints so the configuration is mapped elsewhere and delay is reduced. Basically We want to make the pins closer to the logic.

iv) Net delay of BRAM to a DSP