MAVEN SILICON HACKATHON
LEVEL 2

Submitted by

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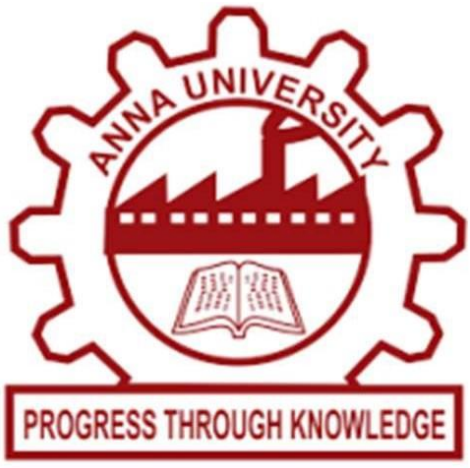
ELECTRONICS AND COMMUNICATION ENGINEERING



COLLEGE OF ENGINEERING, GUINDY
CHENNAI -600025

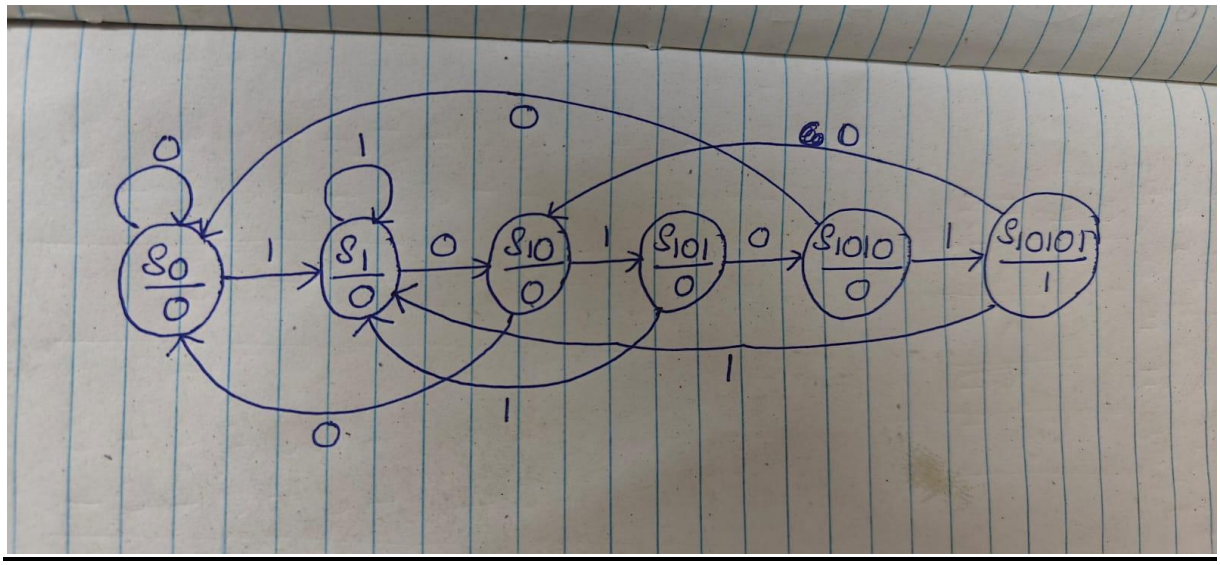
AIM

To design a sequence detector that detects the overlapping sequence “10101” from the input datastream with MSB detected first using Moore State Machine.

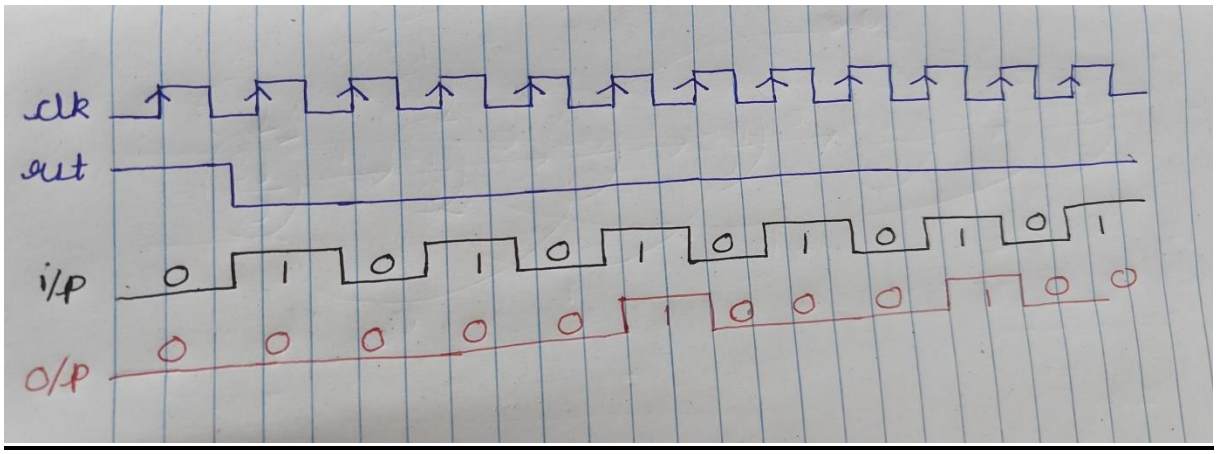
SOFTWARE REQUIRED

Xilinx Vivado

STATE DIAGRAM:



EXPECTED WAVEFORM:



VERILOG CODE:

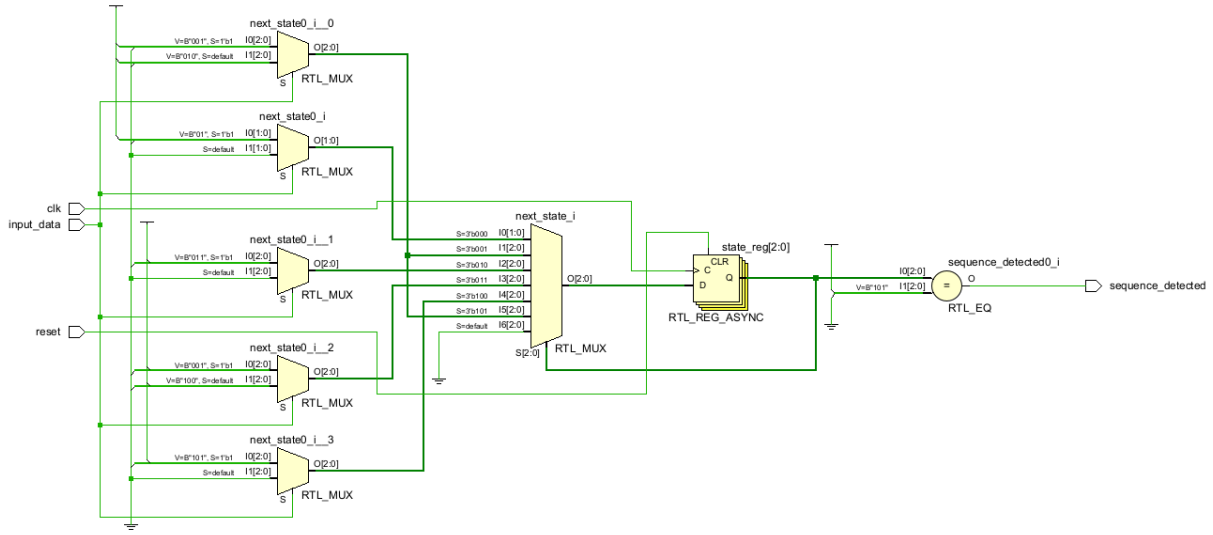
```
`timescale 1ns / 1ps

module Sequence_10101_detector(
    input clk,
    input reset,
    input input_data,
    output reg sequence_detected
);
    parameter S0     = 3'b000,
              S1     = 3'b001,
              S10    = 3'b010,
              S101   = 3'b011,
              S1010  = 3'b100,
              S10101 = 3'b101;

    reg [2:0] state, next_state;
    always @(posedge clk or posedge reset) begin
        if (reset)
            state <= S0;
        else
            state <= next_state;
    end


    always @(*) begin
        case (state)
            S0:     next_state = input_data ? S1 : S0;
            S1:     next_state = input_data ? S1 : S10;
            S10:    next_state = input_data ? S101 : S0;
            S101:   next_state = input_data ? S1 : S1010;
            S1010:  next_state = input_data ? S10101 : S0;
            S10101: next_state = input_data ? S1 : S10;
            default: next_state = S0;
        endcase
    end

        always @(*) begin
        sequence_detected = (state == S10101);
    end

endmodule
```

TEST BENCH:

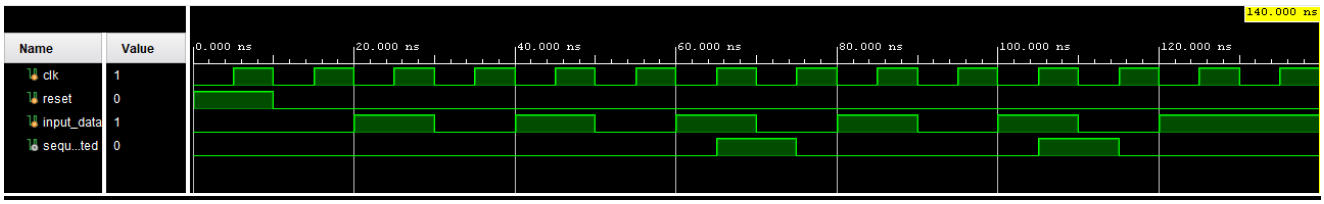
```
`timescale 1ns / 1ps
module Sequence_10101_detector_tb;
    reg clk;
    reg reset;
    reg input_data;
    wire sequence_detected;
    // Instantiation
    Sequence_10101_detector uut (
        .clk(clk),
        .reset(reset),
        .input_data(input_data),
        .sequence_detected(sequence_detected)
    );
    always #5 clk = ~clk;
    initial begin
        clk = 0;
        reset = 1;
        input_data = 0;
        #10;
        reset = 0;
        #10 input_data = 1;
        #10 input_data = 0;
        #10 input_data = 1;
        #10 input_data = 0;
        #10 input_data = 1; // (sequence_detected = 1)
        #10 input_data = 0;
        #10 input_data = 1;
        #10 input_data = 0;
```

```
        #10 input_data = 1;
        #10 input_data = 0;
        #10 input_data = 1; // (sequence_detected = 1)
        #20;
        $finish;
    end
endmodule
```

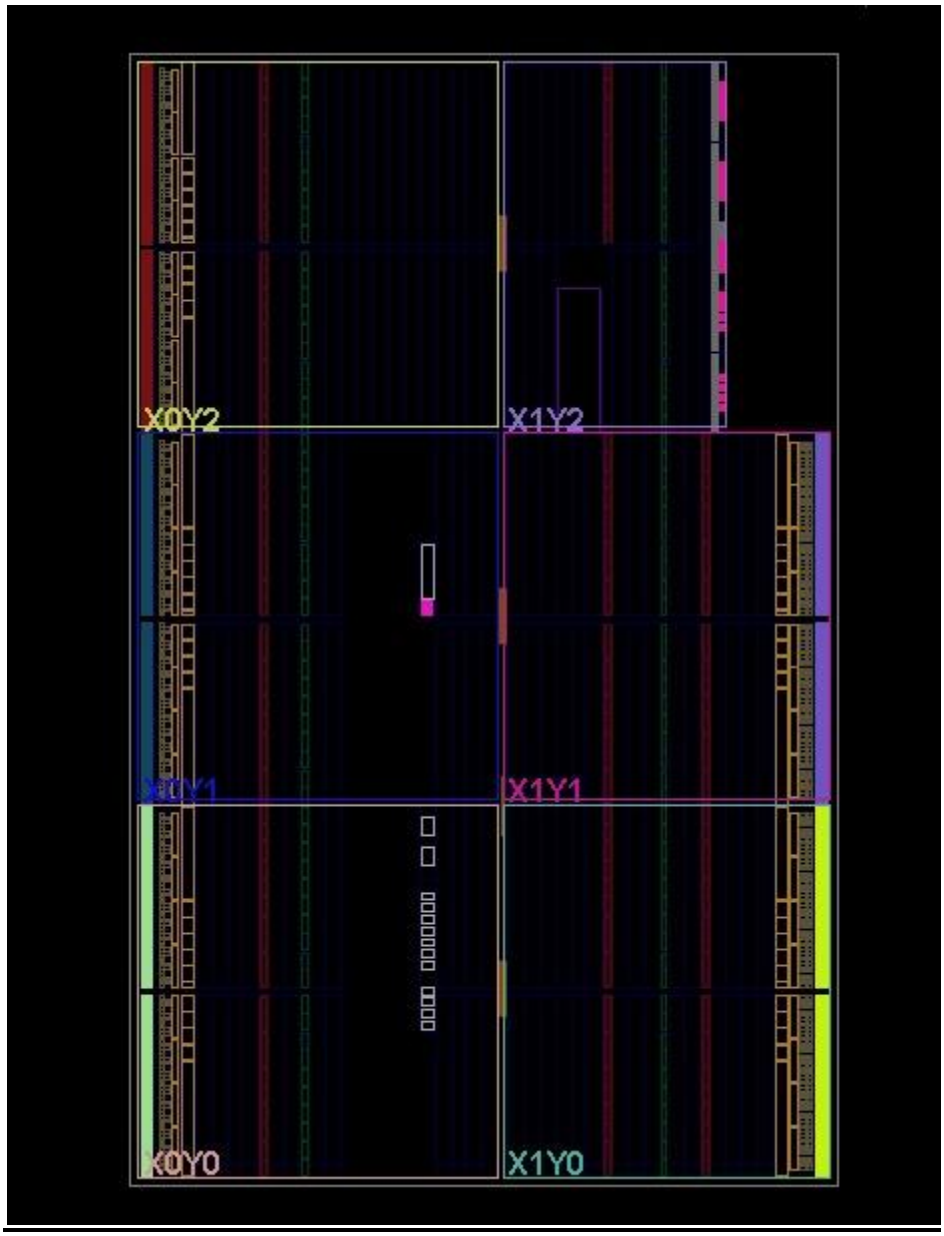
RTL SCHEMATIC:



SIMULATION :



SYNTHESIS:



RESULT:

The sequence detector has been implemented using a Moore state machine logic. The corresponding Verilog code and testbench were developed, simulated, and successfully verified.