Implementation of serial adder using Verilog

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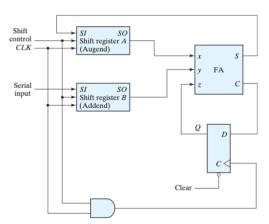
Abstract—This document briefly explains the implementation of a serial adder using the popular hardware description language Verilog. (Abstract)

Keywords— Shift registers, D filp-flops, Full adder, Digital Electronics, Verilog (key words)

I. INTRODUCTION

Serial adder is an interesting circuit that performs the addition between two binary numbers in serial form. Serial binary adder performs bit by bit addition. Two shift registers are used to store the binary numbers that are to be added. A single full adder is used to add one pair of bits at a time along with the carry. The carry output from the full adder is applied to D flip flop. After that output is used as carry for the next significant bits. The sum bit from the output of the full adder is transferred to one of the two shift register.

II. CIRCUIT DIAGRAM



Block diagram of serial adder (Ref. Morris Mano)

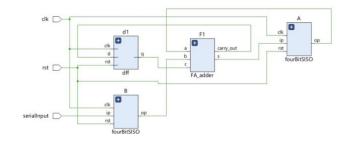
III. VERILOG CODING

Used hierarchical approach to model a serial adder in Verilog. Designed every block using structural modelling and even behavioral modelling in some places. Verified the working of every structure individually using iverilog and Edaplayground.

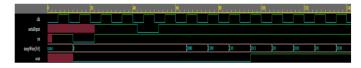
After designing a serial adder, for testing purpose I have written a testbench which performs addition of two 4-bit binary numbers serially. Here the serial adder is capable of adding 4 bits serially. Hence a 4-bit serial adder.

IV. OUTPUTS

For testing, the two shift registers are loading with two 4-bit binary numbers. They are 1011 and 1111. Addition of these two numbers produce 1010 as sum and 1 as carry. The designed serial adder is simulated using Xilinx Vivado.



RTL layout



Timing diagram

From the timing diagram, the outputs can be verified as mentioned before.

REFERENCES

 Digital Design | with an introduction to the Verilog HDL,VHDL, and SystemVerilog | Sixth Edition | By M. Morris Mano and Micheal D. Ciletti