DIGISIM

PROBLEM STATEMENT

Theme:

Tetris is primarily composed of a field of play in which pieces of different geometric forms, called "Tetriminos", descend from the top of the field. During this descent, the player can move the pieces laterally and rotate them until they touch the bottom of the field or land on a piece that had been placed before it. The player can neither slow down the falling pieces nor stop them, but can accelerate them in most versions. The objective of the game is to use the pieces to create as many horizontal lines of blocks as possible. When a line is completed, it disappears, and the blocks placed above fall one rank.

Task Description:

Tetris we will be considering will follow below mentioned rules:

- Player can move pieces left or right. (one step at a time) Rotation of pieces is not allowed.
- Player can neither slow down the falling pieces nor stop them but can skip rows. (one row at a time)
- There will only be single colored blocks (black).
- In digital system, block will be represented by 1 and blank spaces will be represented by 0.
- Figure above represent a 10x20 Tetris.
- Blocks should be considered as connected if there is no blank space be tween them.

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Example 1 :

0000
0110
0000
0000

— is a 2 x1 block on left shift it will become.

0000
0000
1100
0000

— and no further left shifts would be possible.

Example 2:

0100
0110
0000
0000

— is a L shaped block.

0000
0000
0100
0110

— If a jump is executed it.

In the above figure **0000001110** i.e. 10th line from bottom is the Top layer.

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Round Details

Round 2:

1. Consider a 8x10 Tetris in which falling blocks can be shifted left, right or jump a row.
2. In this Tetris lowest completed row (all 1) disappears and above rows falls on the rank..
3. Data for the upcoming block will be saved in a ROM. Blocks can be of any shape.
4. **Design a Proteus simulation of circuit for above mentioned Tetris game. Tetris should be shown using logic probes arranged in matrix form.**
5. Simulation files and a detailed explanation of working should be submitted in pdf format by mailing it to **vishrut.bohara.ece17@itbhu-.ac.in** with subject as "TeamName_Digisim_Round2".

Note: In Round 1 your circuit (state diagram) is a player and we are the game. In Round 2 your circuit is the game and we are the players.

The participants are advised to make use of the following ICs for uniformity:

- **COMPARATOR:** Comparator-74HC85
- **BUFFER:**
  - Quadruple buffer gate with tristate outputs-74HC125
  - Octal Buffer with tristate outputs-74HC241

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- **FLIP FLOPS:**
  - Dual Positive Edge triggered D -Type flip flops-74LS74
  - Quadruple D type Positive Triggered Flip-Flops with clear-74LS175
  - Octal D type Positive Triggered Flip-Flops with clear-74LS273
  - Dual J-K Positive Edge Triggered Flip-flops with clear and preset-74LS109
- **MULTIPLEXER:**
  - Quadruple 1 of 2 Data Selectors /Multiplexer-74LS157
  - Dual 4 to 1 Selector/Multiplexer- 74LS153
- **COUNTERS:**
  - Synchronous 4-bit binary counters-74LS161
  - 8 bit binary Counter with tristate output registers-74LS590
  - 4 bit Synchronous up/down Binary Counters-74LS169
  - Synchronous 4 bit Binary Counters-74163
- **ADDER:** 4 bit Binary Full Adders with Fast Carry-74LS283
- **ROM:** ROM (4K*8) -2732

Some important details:

CPC = Clock cycles used per command

Cost of various components:

- ROM - 20
- J-K,D Flip Flop(74LS74) – 0.5,
- Binary Full Adder, MUX, Quad D Flip Flop - 2
- 8 bit counter, Octal D Flip Flop, Comparator - 4
- Logic Gates, CLOCK – 0.2
- LOGICPROBE, LOGICSTATE – 0

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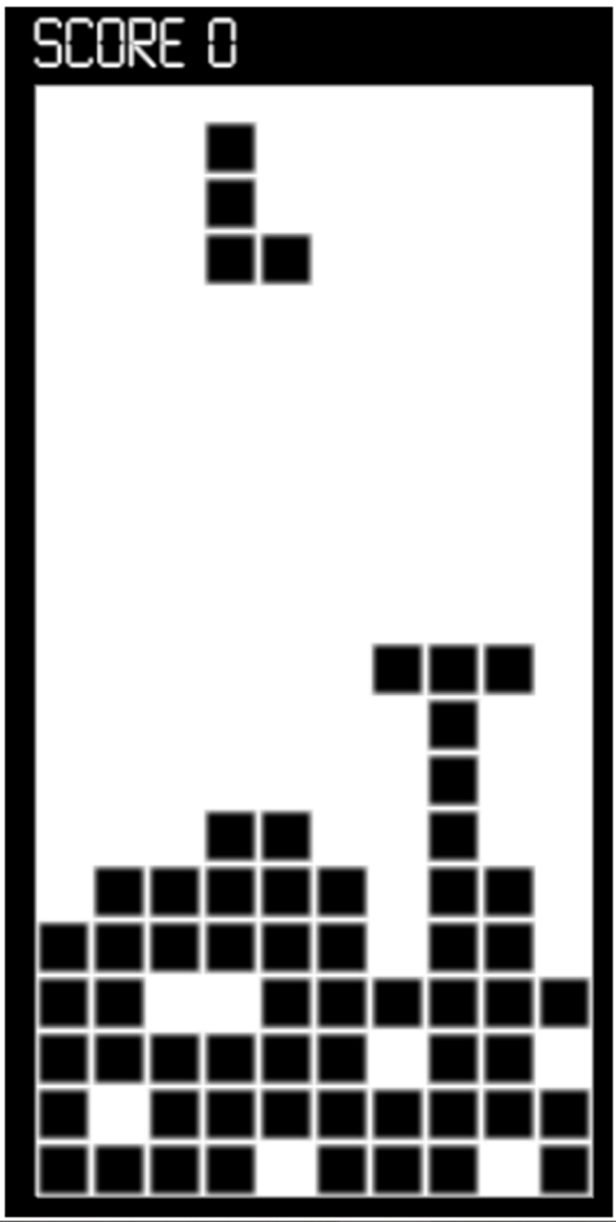
Round Details



0000000000
0001000000
0001000000
0001100000
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0000000000
0000000000
0000000000
0000000000
0000001110
0000000100
0000000100
0001100100
0111110110
1111110110
1100111111
1111110110
1011111111
1111011101

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Scoring

Awards:

- **30 points** will be awarded to the team on the basis of **workshop performance.**
- **70 points** will be awarded to the team on completion of **Round 1 successfully.**
- **300 points** will be awarded to the team on completion of **Round 2 successfully.**
- **30*(CPC) points** will be deducted from **Round 2** score.
- **10 points** will be added to **Round 2** score for every new features added.
- Total **cost** of the circuit will be **deducted from Round 2** score.
- **Final Score = Workshop score + Round 1 score + Round 2 score**
- **Workshop score = Quiz score + 5*(no. of workshop attended)**
- **Round 1 score = 70 (if submitted successfully).**
- **Positions** will be decided on the basis of **Final Score.**

Rules

Event Rules:

- The final solutions must be submitted to the event coordinator in the format specified.
- Submission are accepted till 5th April 2020.

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General Rules:

• The organizers reserve the right to change the rules as they deem fit. Change in rules, if any, will be highlighted on the website and notified on the Whatsapp group.
• The decision of the organizers shall be final and binding.
• In case of any type of cheating suspected, the team will be immediately disqualified and no certificate will be given.
• Only Proteus simulation file will be accepted in this Round.

Round Rules:

• **Only one ROM and one clock should be used in Round 2.**
• Simulations based on components other than specified will not be accepted.

Certification Policy:

• The top three teams will be awarded a certificate of excellence.
• All teams qualifying the first round will be awarded a certificate of participation.
• Disqualified teams will not be considered for any certificates.