

# SPI (Serial Peripheral Interface)

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## Introduction

- The Serial Peripheral Interface (SPI) is a synchronous serial communication protocol commonly used in embedded systems for communication between microcontrollers and peripheral devices.
- It is a full-duplex, master-slave communication protocol that utilizes multiple wires for data transfer, including a clock signal (SCK), a master-out-slave-in (MOSI) line, a master-in-slave-out (MISO) line, and a chip select (CS) line.
- The SPI interface is widely adopted due to its simplicity, high data transfer rates, and support for multiple devices on the same bus.



## **Applications**

#### • Flash Memory and SD Cards

• SPI is often used to interface with external memory devices, such as Flash memory and SD cards, for data storage and retrieval.

#### • Display Modules

• Some graphical LCDs and display modules use SPI for efficient communication with microcontrollers.

#### Wireless Modules

• SPI is employed in communication with wireless modules, such as Wi-Fi and Bluetooth modules, to enable wireless connectivity in embedded systems.

### • Sensor Interfacing

• Many sensors, including accelerometers, gyroscopes, and pressure sensors, use SPI for data transfer to microcontrollers.

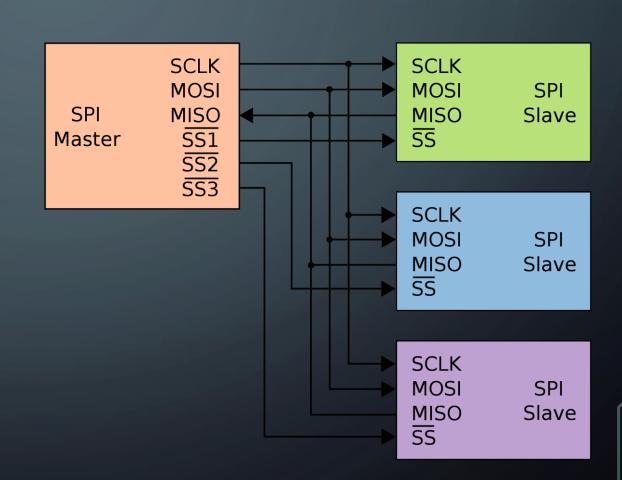
### • Digital-to-Analog Converters (DACs) and Analog-to-Digital Converters (ADCs)

• SPI is often utilized for interfacing with DACs and ADCs to convert analog and digital signals.



## **Properties**

- Connection Type: Serial
- Communication Type: Full-Duplex
- Data Type: Byte
- Synchronize: Sync
- Channel Type: Copper Wire
- Voltage State: TTL
- Bit Order: MSB First
- Hardware Addressing



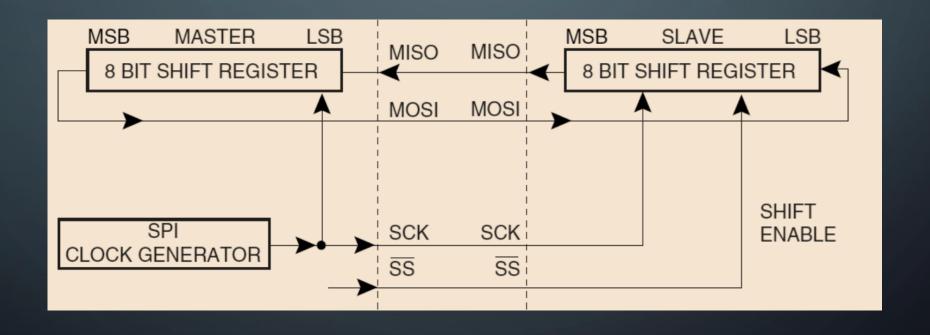


## Registers

- SPI\_CR1 (Control Register 1)
  - Configures the SPI mode, clock polarity, phase, and other parameters.
- SPI\_CR2 (Control Register 2)
  - Configures the data frame format, frame size, and other parameters.
- SPI\_DR (Data Register)
  - Contains the data to be transmitted or received.
- SPI\_SR (Status Register)
  - Indicates the status of the SPI communication, including flags for transmission and reception.
- SPI\_CPSR (Clock Prescaler Register)
  - Sets the clock speed of the SPI communication.



## **Data Flow**



# Modes

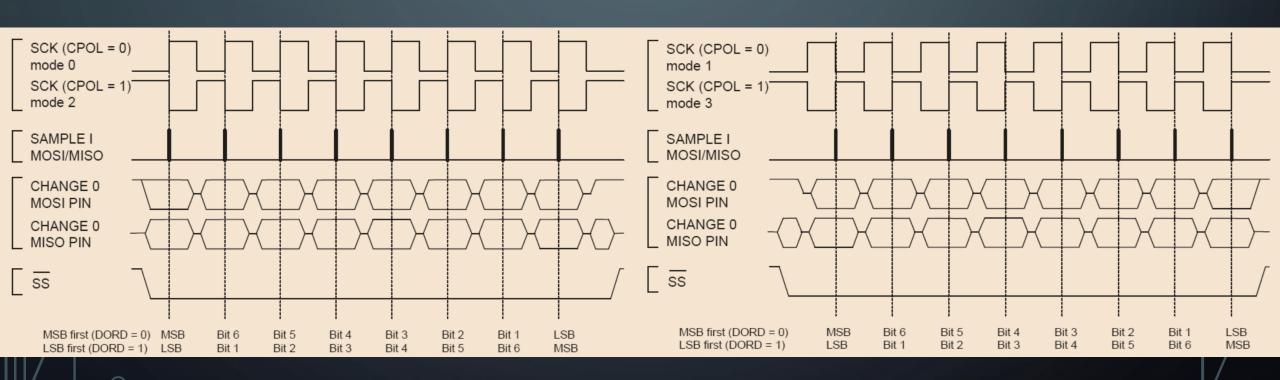
-	<b>Leading Edge</b>	Trailing Edge	Mode	
$\mathbf{CPOL} = 0,  \mathbf{CPHA} = 0$	Sample (Rising)	Setup (Falling)	0	
$\mathbf{CPOL} = 0,  \mathbf{CPHA} = 1$	Setup (Rising)	Sample (Falling)	1	
$\mathbf{CPOL} = 1,  \mathbf{CPHA} = 0$	Sample (Falling)	Setup (Rising)	2	
$\mathbf{CPOL} = 1, \mathbf{CPHA} = 1$	Setup (Falling)	Sample (Rising)	3	



## Modes



### CPHA = 1





# Read/Write

Write Only	MOSI	Data	Data	Data	Data	Data
	MISO	X	X	X	X	X
Read Only	MOSI	X	X	X	X	X
	MISO	Data	Data	Data	Data	Data
Write/Read	MOSI	Cmd	Cmd	X	X	X
	MISO	X	X	Data	Data	Data

# **Process States**

- 1. Set CS to LOW
- 2. Transmit/Receive Byte(s)
- 3. Set CS to HIGH