Computer Organisation and Architecture Laboratory

Assignment: 7

KGP-RISC

Group: 20

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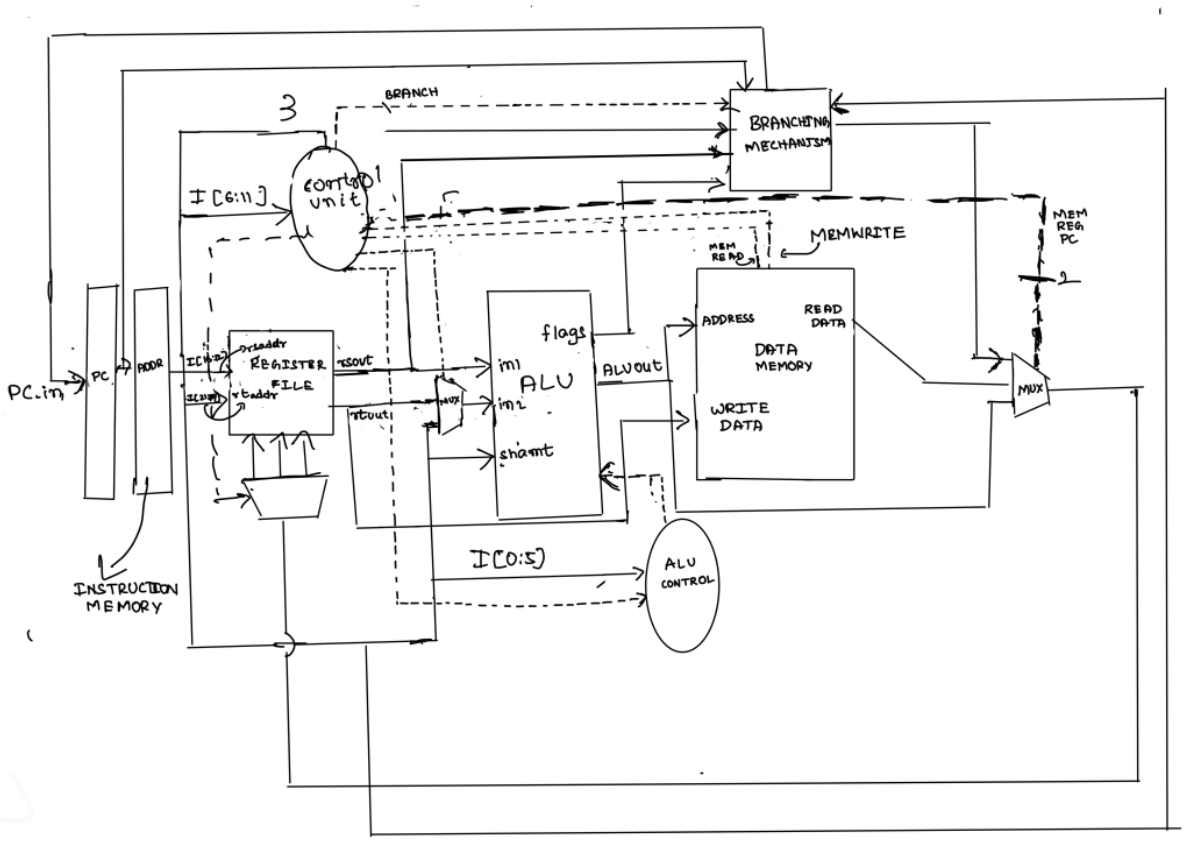
Instruction Format Encoding

Numbers of Regs = 32

Arithmetic, Logical and Shift, Immediate Op				
Func	OPCODE	Source Reg	Target Reg	Shamt
6 bits	6 bits	5 bits	5 bits	10 bits

Branch Operation			
Func	OPCODE	rs	addrs
6 bits	6 bits	5 bits	15 bits



Operation	Op code	Fn code(in decimal)
add	000001	0
comp	000001	1
and	000001	2
xor	000001	3
addi	000010	1
compi	000010	2
shllv	000011	1
shrlv	000011	2
shrav	000011	3
shll	000100	1
shrl	000100	2
shra	000100	3
lw	000101	1
sw	000111	1
b	001000	1
bltz	001000	2
bnz	001000	3

bz	001000	4
bcy	001000	5
bncy	001000	6
br	001001	1
bl	001010	1
diff	001011	1

Control Unit

Takes as input 6 bits OPCODE and assign values to the different control lines. See diagram on next page.

OPCODE	ALU_op	ALU Source	WriteReg	MemWrite	MemRead	MemRegPC	Branch
000001	0001	0	01	0	0	01	00
000010	0010	1	01	0	0	01	00
000011	0011	0	01	0	0	01	00
000100	0100	1	01	0	0	01	00
000101	0101	1	10	0	1	01	00
000111	0110	1	00	1	0	00	00
001000	0111	x	xx	0	0	xx	01
001001	xxxx	x	xx	0	0	xx	10
001010	1001	x	11	0	0	11	01
001011	1010	0	01	0	0	01	00

ALU Control

ALUop	Fn_code	ALU Control signal (in decimal)
0001	000001	0
0001	000010	1
0001	000011	2
0001	000100	3
0010	000001	0
0010	000010	1
0011	000001	6
0011	000010	7
0011	000011	9
0100	000001	4
0100	000010	5
0100	000011	9
0101	000001	0
0110	000001	0
0111	000001	0
0111	000010	1
0111	000011	2
0111	000100	3
0111	000101	4
0111	000110	5
1010	000001	16