Getting Started with Digital VLSI SoC Design and Planning (Simplified)

Step 1: Compile the Application

- Write a program in C language.
- Compile it using GCC.
- The output of this step is called O0.

Step 2: Specification Model

- Write the same logic again in C format (as a model of the required functionality).
- Run it and get the output O1.

Step 3: Compare Outputs

- Check if O0 = O1.
- If they are the same → the specification is correct.

Step 4: Hardware Modeling

- Describe the hardware version of the design using high-level hardware languages like Bluespec or Chisel.

Step 5: RTL Simulation

- Convert the hardware description into an RTL model.
- Run the program on RTL → get output O2.
- Make sure O2 = O1.

Step 6: Split RTL Code

- Divide the RTL code into:
- 1. Processor – synthesizable (can be converted to hardware).
- 2. Peripherals/IPs – extra blocks like Macros and Analog IPs (ADC, PLL, Clock Multiplier).

Step 7: SoC Integration

- Combine processor + peripherals + GPIOs → complete SoC (System on Chip).
- Run the program on this SoC → get output O3.

Step 8: Physical Design Flow

- Convert RTL → GDSII file (layout file).
- Run checks: DRC (Design Rule Check) and LVS (Layout vs Schematic).
- Send to foundry for tapeout (manufacturing).

- Receive the manufactured chip (tapein).

Step 9: Board Integration

- Place the chip on a board along with memory, USB controller, voltage regulator, crystal oscillator, etc.

Step 10: Final Application Run

- Load the application into the chip through USB.
- Run it → get output O4.
- Final check: O1 = O2 = O3 = O4.

Timeline

Total duration: 12–14 months. Foundry (chip manufacturing) takes around 4–6 months.

Chip Specifications

Frequency: 100–130 MHz

Real-world Applications

- Smartwatches (e.g., iWatch)
- Arduino boards
- TV panels
- Air conditioners
- And many more…