32-bit RISC Processor in Verilog HDL

iiitb toy processor

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The 32-bit RISC processor designed in this project uses a pipelined architecture consisting of 3 stages.

The architecture is organized so that it can solve the following issues:

1) Addressing the problem in the following instructions (read instruction synchronous in block RAM).

Ld r1 ,#addr
Add r2, r1, r0

We are implementing the *Load instruction in the second stage* itself instead of going for NOP so as to speed up pipelining.
The load enable to data memory is coming from decoder without going through flipflops. The address to the data memory is also given directly by the IROM output.

2) Write-first mode.
The store and load instructions if in the following order:

St r0, #addr
Ld r1, #addr

The r1 register gets the updated value because we have implemented the data memory in *write-first mode.*

3) Sending the write address to the 3rd stage and back again to second stage to be written in register file.

Add r2, r1, r0
Add r3, r4, r5

In above the first add instruction writes its write data value to r3 instead of r2, if we take the write address from the IROM.
In order to solve this problem, we give the write address to the 3rd stage through the flipflops and then back again to the registers.