1.8V CMOS Low Drop-Out Voltage Regulator

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***Abstract*— This paper discusses the design and simulation of a smart 1.8V Low Dropout Voltage Regulator using 130nm CMOS technology. The operating voltage is from 1.8V to 2.2V, Vref = 1.2V, Vout = 1.8V; VDD = 2V; Iquisent = 100uA; Iref = 10uA; CL = 25pF; IL = 10uA to 15mA. The design is verified with the specifications along with the loop stability analysis and other crucial specifications mentioned in the paper.**

***Keywords*— CMOS, LDO Regulator, skywater 130nm.**

I. Introduction

Low-dropout linear regulator is a dominant type of power management chips. There are other types such as DC-DC switching regulator and charge pump regulator. LDO has the advantages of small static current, small area and low cost, which can be widely used in all kinds of portable consumer electronics products [1]. A basic LDO voltage regulator topology usually consists of a voltage reference, an error amplifier, a pass device, an external load capacitor with small value of internal resistance (ESR) and a feedback network. An error amplifier in negative feedback condition detects an error signal when there is a difference between the feedback voltage and reference voltage. The error signal will control the gate of the pass transistor for maintaining constant output voltage to supply a variable current to the load circuit. OTA is suitable for error amplifier since the output of error amplifier is used to drive the gate of the pass transistor [2].

II. Principle of Generation

The workflow of the whole structure can be seen from Figure 1 that the bandgap reference module generates a reference voltage, which is a stable reference voltage independent of temperature. In addition, the bandgap reference can provide a stable reference current for other modules of LDO as well. With the change of the output load, the sampling voltage returned by the feedback network can be compared with the reference voltage to generate an error voltage. After the amplification of the error amplifier, the grid voltage of the power regulator can be changed. In this situation, the error voltage plays the role of feedback regulation to adjust the current of the power transistor and keep the output voltage stable [3].

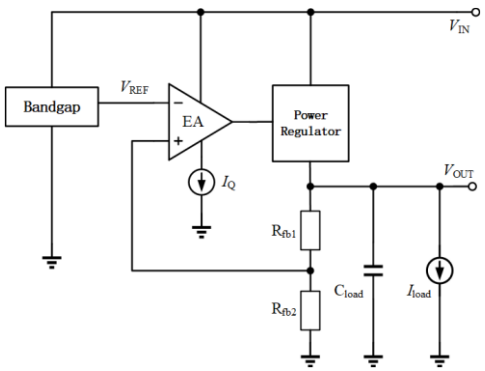

Figure. 1 Typical structure of an LDO

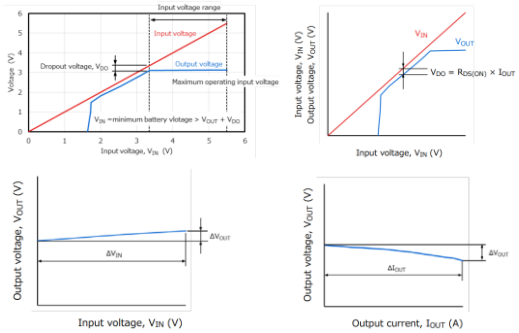

Figure. 2 Waveforms of the proposed design

III. Implementation

The proposed design can be implemented and simulated by following the steps given below:

A. Design of Error Amplifier

B. Design of Power Regulator

C. Design of Feedback Resistor Network

D. Stability Simulation

E. Line Regulation Simulation

F. Load Regulation Simulation

G. PSRR Simulation

IV. Issues and Improvements

Key issues in LDO design include high dropout voltage, reduced power efficiency, challenging load and line regulation, slow transient response, high quiescent current, stability across capacitive loads, heat management, and difficulty achieving high PSRR at high frequencies. Improvements focus on using advanced topologies to reduce dropout, adaptive biasing for efficiency, enhanced compensation for better transient response, and dynamic quiescent current reduction for battery life.

V. Conclusion and Future Scope

The design and simulation of a 1.8V Low Dropout Voltage Regulator using 130nm CMOS technology. The outputs were calculated and the design was verified with the specifications along with the loop stability analysis and other crucial specifications mentioned in the paper.

References

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