

Analog System Design

Report submitted in the partial fulfillment

Of

Bachelor of Technology

In

Electronics and Telecommunications Engineering

By

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**MUKESH PATEL SCHOOL OF TECHNOLOGY
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2023-24

CERTIFICATE



This is to certify that the project entitled “Analog System Design”, has been done by Mr. Nirvan Tamhane under my guidance and supervision for Technical Internship Program as part of curriculum of Bachelor of Technology in Electronics and Telecommunications engineering of MPSTME, SVKM’s NMIMS (Deemed-to-be University), Mumbai, India.

A handwritten signature in black ink, which appears to read "Naveen M. Kumar".

Naveen M. Kumar

Priyanka Verma

Examiner

Date: 15/11/2023

Place: Mumbai

Dr. Avinash D. More

(H.O.D EXTC)

Acknowledgement

I would like to express my heartfelt appreciation to my Internal Faculty mentor, Professor Priyanka Verma, and my Industry mentor, Naveen M. Kumar, for their unwavering guidance and support during my technical internship program. Their mentorship has provided me with invaluable insights into the practical application of academic knowledge and technology in an industrial setting, laying a strong foundation for my future projects and equipping me with essential technical expertise and invaluable industry exposure.

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ABSTRACT

The project titled "Analog System Design" is based on a comprehensive exploration and design of analog blocks and networks, that include current mirrors, operational amplifiers, LDO regulators and Bandgap references. These are designed using R-L-C circuits, P-N diodes, BJTs, MOSFETs, and a few other components. This report delves into the intricate details for their designs and the associated semiconductor physics, industry-standard design methodologies, and analytical techniques.

The designs for this project were implemented on a Linux environment and Cadence Virtuoso Design tool was used for the development and analyses. The Analog VLSI Design flow and Linux file system commands are thoroughly examined, complemented by in-depth training in schematic design and simulation procedures within the Cadence Virtuoso design suite.

Progressing through the project timeline, the initial focus was mainly on single-stage and cascode amplifier design, with a particular emphasis on the construction and significance of current mirrors in analog designs. This knowledge sets the stage for the impending design of operational amplifiers.

Once the single-stage amplifier designs were through, the project went forward with the design and operation of differential amplifiers, alongside to that, a comprehensive study of noise parameters in 5T-OTA and 9T-OTA designs, including their impact on accuracy and mitigation strategies.

Following the OTA design and simulations, the second phase of the project included the exploration of 2-stage amplifier designs featuring miller compensation and the initiation of the Low-Dropout (LDO) regulator designs.

Following the OTA design and simulations, the second phase of the project included the exploration of Bandgap reference (BGR) designs featuring CTAT and PTAT calculations along with different design architectures.

My project "Analog System Design" encapsulates a progressive journey of acquiring knowledge, building skills, and applying them in a practical context, ultimately equipping me with a robust foundation in analog system design.

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Chapter 1

Introduction

1.1 Introduction of the Industry

Takshila Institute of VLSI Technologies operates within the dynamic and cutting-edge industry of Very Large-Scale Integration (VLSI) technology. This industry represents a pivotal sector in the world of electronics and semiconductor manufacturing, driving innovation, efficiency, and miniaturization in an increasingly interconnected world.

This industry is mainly divided into three sectors: digital, analog, and mixed signal design of Integrated Circuits or more commonly known as chips. The design of these chips is further bifurcated into several blocks out of which Takshila VLSI is mainly into the digital domain, but it consists of analog and mixed signal design teams as well.

VLSI technology involves the integration of millions and billions of transistors onto a single semiconductor chip, enabling the creation of highly complex and powerful electronic systems. These chips serve as the foundational building blocks for a wide range of electronic devices, from smartphones and laptops to automotive systems and IoT devices.

1.2 Problem Addressed

The project undertaken by Takshila Institute of VLSI Technologies is centered around addressing critical problems and challenges within the field of Very Large-Scale Integration (VLSI). In the context of the pressing need for innovation in VLSI, several key issues are being tackled to drive progress in this vital industry:

1. Faster Processing: The relentless pursuit of faster processing speeds is a hallmark of the VLSI industry. The project aims to enhance the performance of integrated circuits to meet the growing computational demands of applications such as artificial intelligence, machine learning, and data-intensive tasks.

2. Higher Efficiency: Energy efficiency is a paramount concern as electronic devices become more ubiquitous. Innovations in Analog VLSI design aim to reduce power consumption while maintaining or even enhancing performance, thereby extending battery life, and minimizing environmental impact.
3. Lower Costs: The project recognizes the need for cost-effective solutions in semiconductor chip production. By optimizing processes, utilizing advanced materials, and implementing efficient design methodologies, the goal is to reduce the overall production costs of VLSI chips.
4. Miniaturization and Integration: This project seeks to advance miniaturization techniques, allowing for more functionality on smaller chips and enabling the creation of smaller, lighter, and more portable devices. In this project, a minimum transistor size of 45nm is considered for the design of the analog blocks.
5. Reliability and Robustness: As electronic systems become increasingly complex, ensuring the reliability and robustness of VLSI chips is vital. The project addresses techniques for fault tolerance, error correction, and robust design to enhance the dependability of electronic devices.
6. Analog and Mixed-Signal Chposeges: Meeting the requirements of analog and mixed-signal applications poses unique challenges. The project delves into optimizing analog designs, reducing noise, and improving signal integrity.

By addressing these multifaceted challenges, the project conducted by Takshila Institute of VLSI Technologies contributes to the ongoing innovation and advancement of VLSI technology. These solutions not only enhance the performance and capabilities of electronic devices but also contribute to a more sustainable, connected, and technologically advanced future.

1.3 Background of the project topic and related literature.

Project Background

The project titled "Analog System Design" is the result of an extensive exploration and design endeavor focused on analog blocks and networks. Within this project, key components including current mirrors, operational amplifiers, low dropout regulators,

oscillators and bandgap references were meticulously designed and constructed. These intricate designs drew upon a rich palette of electronic components such as R-C circuits, P-N diodes, BJTs, MOSFETs, and others, crafting a foundation rooted in semiconductor physics, industry-standard design methodologies, and sophisticated analytical techniques.

The purpose of this project is mainly based on the optimization of operational amplifiers, Low-Dropout (LDO) regulators, and Bandgap references (BGRs) that includes tailoring these crucial analog components to meet specific performance requirements and application needs. Custom design allows for fine-tuning parameters such as gain, bandwidth, power consumption, and noise characteristics to precisely match the demands of a particular system. This approach ensures optimal performance, efficiency, and reliability in applications where off-the-shelf components may not provide an ideal fit.

Moreover, custom designs enable the integration of innovative features, enhancing the overall functionality and competitiveness of electronic systems. By crafting these essential analog blocks to precise specifications, engineers can unlock the full potential of their designs, enabling advancements in various fields, from consumer electronics to aerospace and beyond.

Related Literature

1. Folded Cascode Current Mirror Design using Cadence.

The research paper titled "Folded Cascode Current Mirror Design using Cadence" discusses the growing demand for analog integrated devices and the increased use of current mirror circuits. These circuits provide constant current and serve as active loads due to their high output impedances. The paper focuses on a specific type of current mirror known as the folded cascode configuration, which employs a dual pnp-npn network for current feedback. This configuration offers superior output impedance, a wide impedance-bandwidth, and improved current tracking.

The study utilizes simulation tools like Multisim and Cadence for verification. It provides a theoretical framework for understanding current mirror devices and delves into the properties of the folded cascode current mirror. The simulation results obtained through Cadence are compared with those from Multisim, showing general agreement in terms of output resistance and bandwidth, with minor differences in saturation behaviors.

The conclusion emphasizes the potential for further research using Cadence 180nm MOSFET devices, which could advance the field of low-power integration, including applications like operational amplifiers and digital circuits. Overall, the paper underscores the importance of folded cascode current mirrors and their potential contributions to analog integrated circuit design.

2. Experimental Design and Implementation of two stage CMOS Operational amplifier using 90nm technology.

The research paper titled "Design and Implementation of two stage CMOS Operational amplifier using 90nm technology" focuses on the design and analysis of a two-stage CMOS operational amplifier (Opamp) with an emphasis on optimizing the Opamp gain. The study explores various parameters affecting Opamp characteristics, including gain, phase margin, slew rate, and power dissipation. The research was conducted using Cadence Virtuoso with 90nm technology.

The obtained results indicate that the designed Opamp achieves a gain of 84 dB, a phase margin of 560, and a power dissipation of $38.02\mu\text{W}$. These improvements in gain were achieved through parameter optimization, specifically adjusting the (W/L) values and carefully sizing the circuit structure. The findings demonstrate the successful implementation of a high-performance Opamp with promising specifications, making it a valuable contribution to the field of electronic device design and CMOS technology.

3. A Wide-Load-Range Mixed-Mode LDO Regulator with Single-Transistor-Assisted Buffer

The research paper introduces a novel low-dropout (LDO) regulator featuring a single-transistor-assisted buffer and mixed-mode control for a wide range of load conditions.

The single-transistor-assisted PMOS-input unity-gain buffer extends the operational range of the analog power transistor, ensuring the LDO regulator functions effectively even at very light load currents. To enhance its ability to handle heavy loads, the regulator employs mixed-mode control to detect heavy loads and activate or deactivate a digital power transistor, which efficiently supplies larger currents to the load. With digital assistance, this LDO regulator demonstrates improved load regulation and enhanced performance under heavy loads. A prototype was fabricated in a standard 0.18- μm CMOS process, occupying a small active area of 0.01 mm². The experimental results show that the LDO regulator, with digital assistance and single-transistor-assisted buffer, achieves a significant reduction in droop voltage and maintains a load regulation of 0.21 mV/mA. In conclusion, this paper introduces an innovative LDO regulator design that effectively handles a wide range of load conditions and demonstrates improved performance with experimental verification.

4. Design of an improved Bandgap Reference in 180nm CMOS Process Technology

The research paper titled "Design of an improved Bandgap Reference in 180nm CMOS Process Technology" focuses on the development of a Bandgap reference circuit with exceptional performance characteristics. In the abstract, the authors describe their achievement of a low temperature coefficient of 0.2ppm/ $^{\circ}\text{C}$ within a 180nm CMOS process. The designed circuit produces a stable output voltage reference of 1.12V at room temperature (27°C) and maintains this precision across a wide temperature range from -40°C to +125°C while operating at a supply voltage of 1.8V. The circuit exhibits low power consumption of 52.37 μW at room temperature and occupies an active area of 81.4 $\mu\text{m} * 63.43\mu\text{m}$. The design and simulations were carried out using Cadence Virtuoso and Spectre ADE, respectively.

In conclusion, the authors highlight the significant advantages of their first-order CMOS Bandgap reference (CM_BGR) design in 180nm CMOS technology. They emphasize the precise output voltage reference achieved at room temperature and the impressive low temperature coefficient of 0.2ppm/ $^{\circ}\text{C}$ across a wide temperature range. They compare their design favorably with existing circuits in more advanced CMOS technologies, demonstrating its superior temperature coefficient performance and

suitability for various CMOS process technologies. The proposed CM_BGR design is praised for its simplicity and low power consumption, making it a versatile choice for practical implementation in a wide range of applications.

5. Design of Voltage Amplifiers with Optimization of Multiple Design Parameters

The research paper titled "Design of Voltage Amplifiers with Optimization of Multiple Design Parameters" addresses the need for circuit designs that maximize the performance of sophisticated appliances with minimal modifications. The study focuses on improving two-stage operational amplifier designs, specifically comparing three variations: a simple two-stage operational amplifier, a two-stage operational amplifier with cascoding in the inner stage and lead compensation, and a two-stage operational amplifier with cascoding in the inner stage, lead compensation, and gain boosting.

The experiments were conducted using the GPDK045 and Analog Library in the Cadence Virtuoso Design Environment with specific parameters. The results indicate that the two-stage operational amplifier with cascoding in the inner stage and lead compensation achieved the highest unity gain bandwidth of 1.1436 GHz, while the method with gain boosting achieved the highest DC Gain of 117.1087 dB. Additionally, phase margin and power dissipation were evaluated, with the former being 57.8963 degrees and 57.3776 degrees for the two methods and the latter being 0.69 mW and 0.235 mW, respectively.

In conclusion, the simple two-stage operational amplifier demonstrated a lower unity-gain bandwidth and higher power consumption compared to the two-stage operational amplifier with cascoding in the inner stage, lead compensation, and gain boosting. The latter design proved to be the most effective, offering the best results across various parameters, including high unity gain bandwidth, low power dissipation, high DC Gain, CMRR, PSRR+, and PSRR-. Therefore, the research concludes that the two-stage operational amplifier with cascoding in the inner stage, lead compensation, and gain boosting is the most optimized choice among the three designs.

1.4 Motivation and scope of the report

Motivation

The motivation for this project report is to document and communicate innovative solutions to critical VLSI challenges. It captures the strategies for enhancing processing speeds, optimizing designs, and increasing energy efficiency. The report serves as a knowledge-sharing platform, transferring insights and best practices within the analog VLSI field. Additionally, it evaluates the effectiveness of proposed solutions and informs future decision-making. Ultimately, the report showcases the project's commitment to advancing VLSI technology, sharing knowledge, and providing a roadmap for further exploration and improvement.

Scope of the report

This report provides a comprehensive overview of the "Analog System Design" project, covering the design of essential analog components, the use of specific semiconductor elements, and the tools employed. It extends to the broader context of addressing critical VLSI challenges, including enhanced processing speeds, improved energy efficiency, advanced miniaturization, and optimized analog designs. The report serves as a valuable resource for those interested in analog VLSI and contributes insights into broader technological advancements in the field.

1.5 Organization of report

Chapter 2 of this report states the challenges faced due to design constraints, noise, and other degrading parameters in analog block designs.

Chapter 3 describes the planning, procedures, components, and methods used while designing to go about the project.

Chapter 4 gives information about the various tests and simulations performed and their analysis which helped me to improve the performance of the blocks.

Chapter 5 describes the advantages, limitations, and applications of these analog blocks in real world applications for consumer use.

Chapter 6 discusses the conclusion of the results and the analyzed data after which future work for the mentioned designs was discussed and stated.

Chapter 2

Problem Statement

The field of Very Large-Scale Integration (VLSI) confronts an array of pressing challenges in the era of rapid technological advancement. The need for faster processing speeds, heightened energy efficiency, cost-effective semiconductor chip production, advanced miniaturization techniques, increased reliability, and optimized analog and mixed-signal designs underscores the critical issues facing the industry. In response, the project undertaken by Takshila Institute of VLSI Technologies endeavors to tackle these multifaceted challenges head-on. By fostering innovation and driving progress in VLSI, the project seeks to elevate the performance and capabilities of electronic devices while propelling us toward a more sustainable, interconnected, and technologically advanced future.

Chapter 3

Methodology

3.1 Planning

The foundation of any successful analog system design lies in meticulous planning and specification. For our project, which revolves around current mirrors, operational transconductance amplifiers (OTAs), and Low-Dropout (LDOs) regulators, Bandgap Voltage References (BGRs) the planning phase is of paramount importance.

In the initial stages of planning, we define the precise specifications for these essential analog components. This involves determining critical parameters such as gain, bandwidth, input and output voltage ranges, power consumption, and noise constraints. These specifications serve as the guiding principles for subsequent design and development.

Simultaneously, we meticulously outline the specific design methodologies, circuit configurations, and semiconductor components to be utilized. This includes the selection of appropriate transistors, resistors, and capacitors, taking into account the desired performance characteristics and the target transistor size, such as the minimum size of 45nm for analog blocks.

Planning also encompasses the consideration of trade-offs, where we carefully weigh factors like power efficiency versus performance and speed versus accuracy. These trade-offs ensure that the final designs align closely with project goals.

Additionally, we establish comprehensive testing and validation procedures during the planning phase. These protocols will be instrumental in verifying that the actual performance of the analog blocks aligns with the planned specifications.

Specifications:

Design a single-stage common source amplifier for a gain of 5 where the input signal is a sine wave of 100KHz having 2mV pp amplitude with a DC voltage of 0.8V. The supply voltage provided is 1.8V and the drain current must be less than 20uA. Design the schematic and simulate using transient, DC, and sweep analysis.

Fig 3.1.1 Specifications for a single stage CS amplifier.

Changes: Add source degeneration to increase the gain if the gain is less than 5 and change the W/L ratio keeping ID less than 20uA.

Fig 3.1.2 Specifications changes that are to be made in the design.

Specifications:

Design a current mirror that has an Iref of 10uA with a supply of 1.8V DC through which the mirrored output current Iout must be 10uA with no load connected to it. Consider equalizing both the MOSFET's VDS voltages to get the same current at the output.

Fig 3.1.3 Specifications for a basic current mirror design.

Specifications:

Design a 5T-OTA for a 2-stage opamp to get an output voltage of 0.9V when the input voltage is 0.9V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD and a load capacitor of 1pF is connected at the output. AC gain must be >100 with an Iss = 1uA (slew rate > 10V/us).

Fig 3.1.4 Specifications for a 0.9V 5T-OTA (Differential amplifier with active load) design.

Specifications:

Design a 5T-OTA for a 2-Stage opamp to get an output voltage of 1.2V when the input voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD and Iref = 10uA. A minimum slew rate of 10V/us must be achieved at Iss = 4uA. AC gain must be >50.

Fig 3.1.5 Specifications for a 1.2V 5T-OTA (Differential amplifier with active load) design.

Specifications:

Design a 5T-OTA for an LDO to get an output voltage of 1.2V when the input voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 2V is provided at the VDD and $I_{ref} = 10\mu A$. A minimum slew rate of 10V/us must be achieved at $I_{ss} = 4\mu A$. AC gain must be >50 .

Fig 3.1.6 Specifications for a 1.2V 5T-OTA
(Differential amplifier with active load) design.

Specifications:

Design a 2-stage opamp to get an output voltage of 0.9V when the input voltage is 0.9V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD and $I_{ref} = 10\mu A$. A minimum slew rate of 10V/us must be achieved at $I_{ss} = 25\mu A$. UGB must be around 5MHz and CLoad of 10pF at the output.

Fig 3.1.7 Specifications for a 0.9V 2-Stage Opamp
design.

Specifications:

Design a 2-stage opamp to get an output voltage of 1.2V when the input voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD and $I_{ref} = 10\mu A$. A minimum slew rate of 10V/us must be achieved at $I_{ss} = 4\mu A$. UGB must be around 5MHz and CLoad of 10pF at the output.

Fig 3.1.8 Specifications for a 1.2V 2-Stage Opamp
design.

Specifications:

Design an LDO regulator to get an output voltage of 1.5V when the input reference voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD. A load capacitor of 1uF (with 20% tolerance) is connected in parallel with a load current of 10uA to 1mA at the output. Iquiscent current must not be $>10\mu A$ and slew rate $>10V/us$.

Fig 3.1.9 Specifications for a 1.5V LDO Regulator
design.

Specifications:

Design an LDO regulator to get an output voltage of 1.8V when the input reference voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 2V is provided at the VDD. A load capacitor of 25pF (with 20% tolerance) is connected in parallel with a load current of 10uA to 15mA at the output. Iquiscent current must not be >100uA and slew rate >10V/us.

Fig 3.1.10 Specifications for a 1.8V LDO Regulator design.

Specifications:

Design a Bandgap Reference circuit to get an output voltage of 1.2V when the input voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 1.8V is provided at the VDD. Iquiscent current must not be >10uA and slew rate > 10V/us.

Fig 3.1.11 Specifications for a 1.2V BGR Banba design.

Specifications:

Design a Bandgap Reference circuit to get an output voltage of 1.2V when the input voltage is 1.2V DC, with an AC sine wave of 1mV amplitude, and frequency of 1KHz. A supply voltage of 2V is provided at the VDD. Iquiscent current must not be >10uA and slew rate > 10V/us.

Fig 3.1.11 Specifications for a 1.2V BGR General design.

3.2 Calculation of Design parameters

After the planning phase, the design specifications serve as a guiding framework, providing a comprehensive overview of the desired output objectives. These parameters encompass intricate calculations such as UnCox, W/L ratio, Overdrive voltage, and a suite of other critical factors.

These calculations represent the cornerstone of the design process, constituting the basis upon which the analog blocks are designed. More specifically, they establish a nexus between gain, transconductance (G_m) of the MOSFETs, and R_{out} , intricately interweaving these elements to create the final design. These calculations aren't mere

technicalities; they are the underpinning factors that ultimately determine the performance, efficiency, and gain of the analog components.

Procedure for calculating the design parameters in analog blocks:

Note: This procedure is for the design of a single stage amplifier, but the initial steps are the same for almost all designs.

1. Calculate the overdrive voltage ($V_{GS}-V_{TH}$) for the MOSFETs.
2. Calculate the $UnCox$ and $UpCox$ for the MOSFETs using the drain current ID (Channel length modulation equation).
3. Calculate the resistor values by finding out the voltage at the drain terminal.
4. Calculate the approximate value of the transconductance (G_m) and R_{out} of the MOSFET to estimate the gain.
5. Calculate the W/L ratio for the MOSFETs and size the transistor as per the requirements or depending upon the drain current constraint.

Calculating the $UnCox$ for NMOS 2V Native V_T device:

$$\begin{aligned} I_D &= 10\mu A \\ V_{GS} &= 271.1mV \\ V_{TH} &= 39mV \end{aligned}$$

Assuming $W/L = 1$ (Taking 1um/1um)

Using the Channel Length Modulation Equation

$$I_D = 1/2 * UnCox * W/L * (V_{GS} - V_{TH})^2$$

$$UnCox = (I_D * 2) / \{W/L * (V_{GS} - V_{TH})^2\}$$

$$UnCox = (10u * 2) / \{1u/1u * (0.2711 - 0.039)^2\}$$

$$UnCox = 371.26 \mu S/V^2$$

Fig 3.2.1 Calculation of $UnCox$ for NMOS 2V Native V_T Device.

Calculating the UnCox for NMOS 2V device:

$$\begin{aligned}I_D &= 10\text{uA} \\V_{GS} &= 0.645\text{V} \\V_{TH} &= 0.484\text{V}\end{aligned}$$

Assuming W/L = 1 (Taking 1um/1um)

Using the Channel Length Modulation Equation

$$I_D = 1/2 * \text{UnCox} * W/L * (V_{GS} - V_{TH})^2$$

$$\text{UnCox} = (I_D * 2) / \{W/L * (V_{GS} - V_{TH})^2\}$$

$$\text{UnCox} = (10\text{u} * 2) / \{1\text{u}/1\text{u} * (0.645 - 0.484)^2\}$$

$$\text{UnCox} = 382.45 \text{ uS/V}^2$$

Fig 3.2.2 Calculation of UnCox for NMOS 2V Device.

Calculating the UpCox for PMOS 2V device:

$$\begin{aligned}I_D &= 10\text{uA} \\V_{GS} &= 0.6707\text{V} \\V_{TH} &= 0.434\text{V}\end{aligned}$$

Assuming W/L = 1 (Taking 1um/1um)

Using the Channel Length Modulation Equation

$$I_D = 1/2 * \text{UpCox} * W/L * (V_{GS} - V_{TH})^2$$

$$\text{UpCox} = (I_D * 2) / \{W/L * (V_{GS} - V_{TH})^2\}$$

$$\text{UpCox} = (10\text{u} * 2) / \{1\text{u}/1\text{u} * (0.6707 - 0.434)^2\}$$

$$\text{UpCox} = 178.49 \text{ uS/V}^2$$

Fig 3.2.3 Calculation of UpCox for PMOS 2V Device.

Calculating the value of R_D in the case of a CS amplifier

$$R_D = V_D / I_D \quad \text{----- (Here } V_D = I_D * R_D\text{)}$$

$$V_D = \{A_v * (V_{GS} - V_{TH})\} / 2$$

Calculating the value of G_m in the case of a CS amplifier

$$g_m = (2 * I_D) / V_{DS}$$

Calculating the voltage for maintaining the MOSFET in saturation in the case of a CS amplifier

$$V_{DS} > V_{GS} - V_{TH}$$

Calculating the output voltage in the case of a CS amplifier

$$V_{out} = V_{DD} - (I_D * R_D)$$

Fig 3.2.4 Calculations for getting the G_m and R_{out} values.

Calculating the W/L in the case of a CS amplifier

$$I_D = 1/2 * UpCox * W/L * (V_{GS} - V_{TH})^2$$

$$W/L = (I_D * 2) / \{UpCox * (V_{GS} - V_{TH})^2\}$$

Fig 3.2.5 Calculations for getting the W/L values.

Note: All the calculations are not added to this report as several calculations have been done on paper which have multiple iterations to optimize the design as per the required specifications.

3.3 Schematic Design

The schematic is designed using the Cadence Virtuoso design tool which runs on a Linux environment. This software tool is used to design the schematic, simulate, design the physical layout, post layout simulations and checks.

The schematic is made first on paper and all the calculations are done by hand (but this tool supports a highly advanced calculator specially created for analog block

design). As per the calculations, the parameters for the design components are set and the stimuli is set for whatever inputs are required or given in the design specifications.

PMOS Characterization schematic:

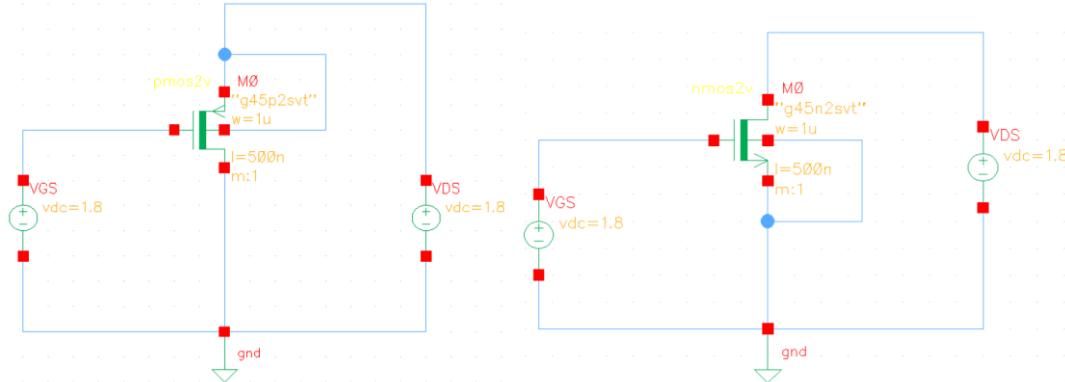


Fig 3.3.1 Schematic designed to calculate the PMOS device parameters.

Fig 3.3.2 Schematic designed to calculate the NMOS device parameters.

CMOS Inverter schematic:

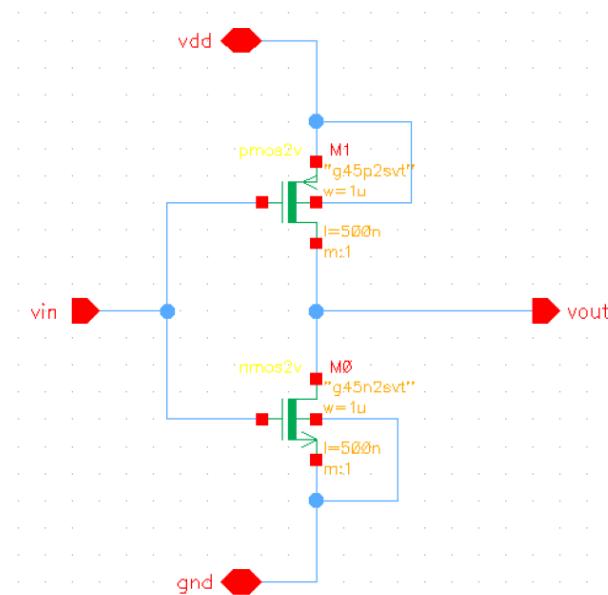


Fig 3.3.3 Schematic of a CMOS inverter.

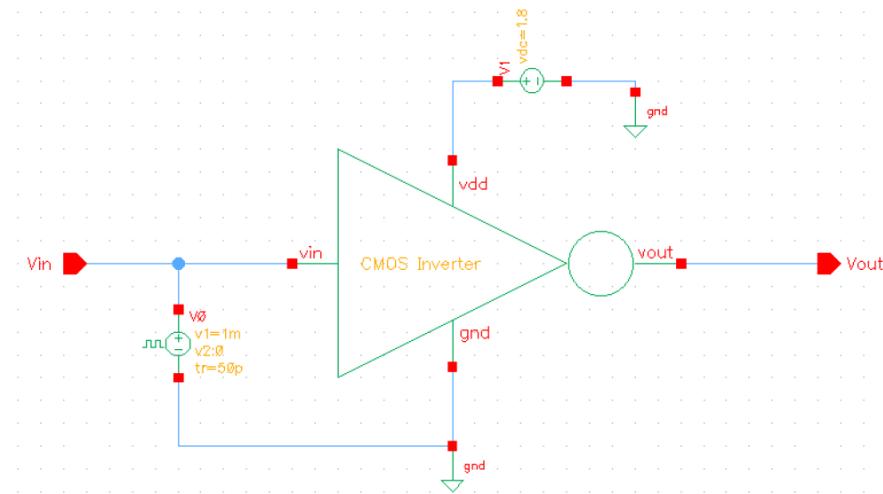


Fig 3.3.4 Schematic of a CMOS inverter testbench with symbol.

CMOS Inverter symbol:

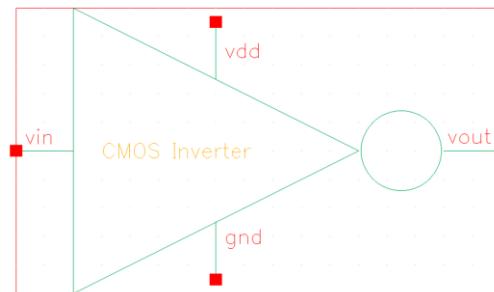


Fig 3.3.5 Symbol designed for the CMOS inverter.

Single-stage NMOS Common Source w/Source Degeneration & Common Source Amplifier schematic:

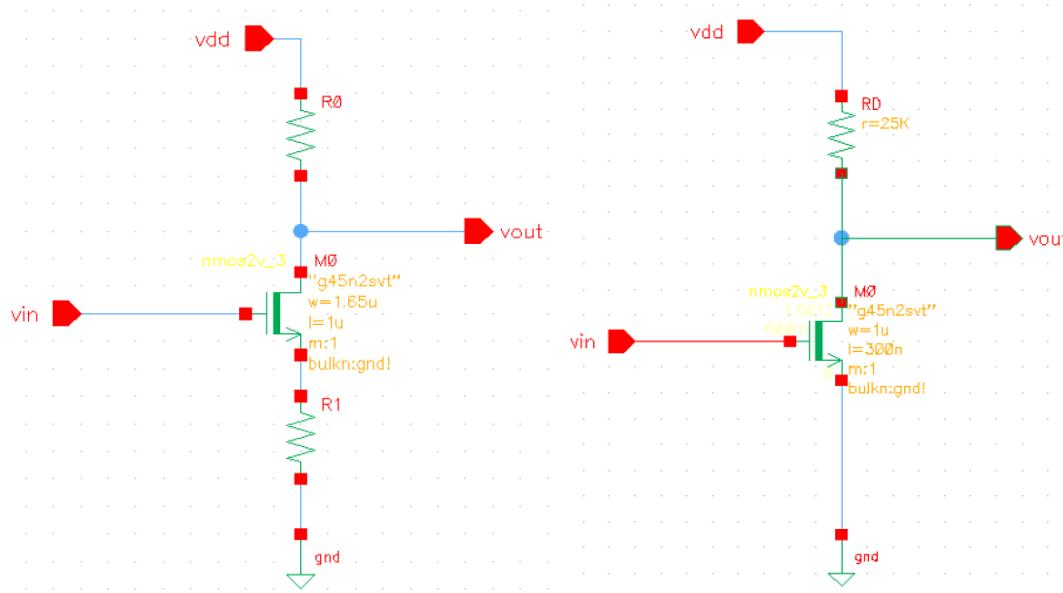


Fig 3.3.6 Schematic of a single-stage NMOS CSSD amplifier for a gain of 5.

Fig 3.3.7 Schematic of a single-stage NMOS CS amplifier for a gain of 3.

Cascode Common Source Amplifier schematic:

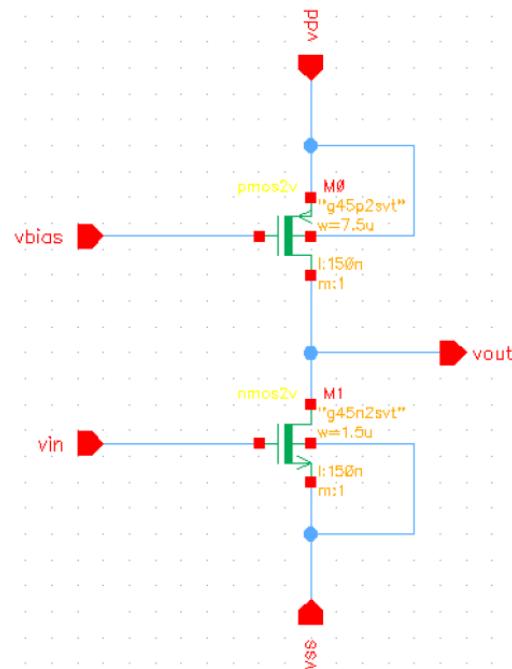


Fig 3.3.8 Schematic of a single stage cascode CS amplifier.

Current Mirror schematic:

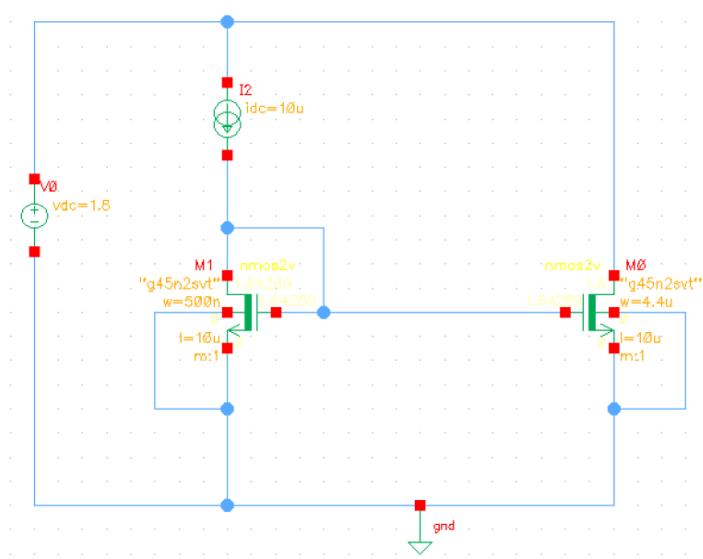


Fig 3.3.9 Schematic for a basic 1:10 current mirror design.

5-Transistor Operational Transconductance Amplifier schematic: [VDD = 1.8V; Vin = 0.7V; Vout = 1.2V; Iss = 10uA]

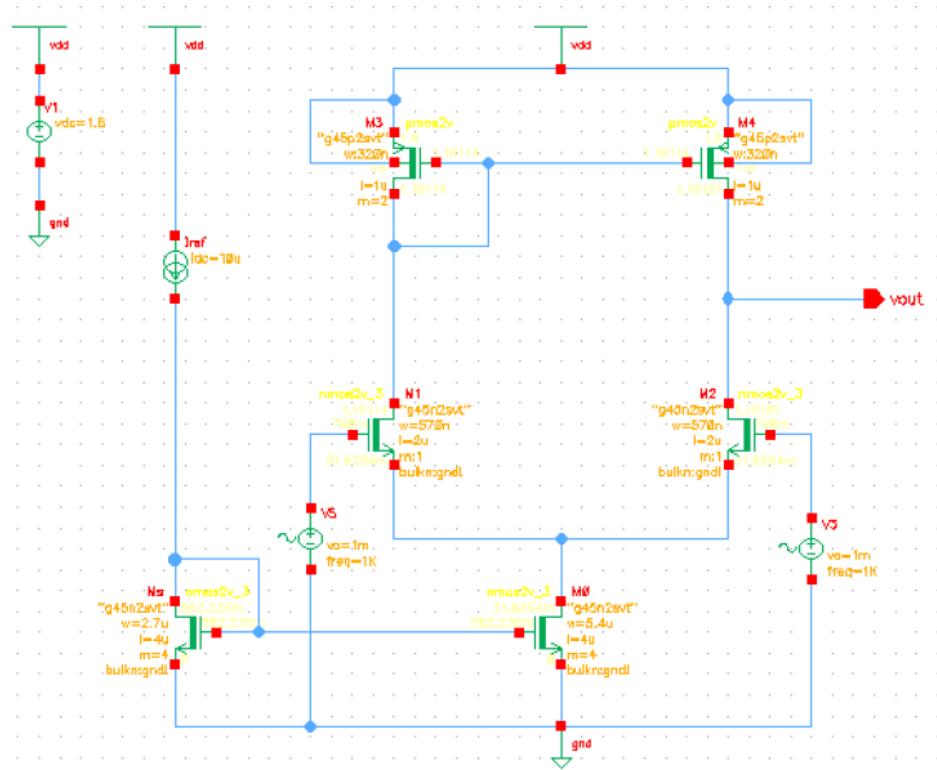


Fig 3.3.10 Schematic for a 5T – OTA (Differential amplifier).

5-Transistor Operational Transconductance Amplifier schematic: [VDD = 1.8V; Vin = 0.9V; Vout = 0.9; Iss = 1uA; Vout = 1.2V]

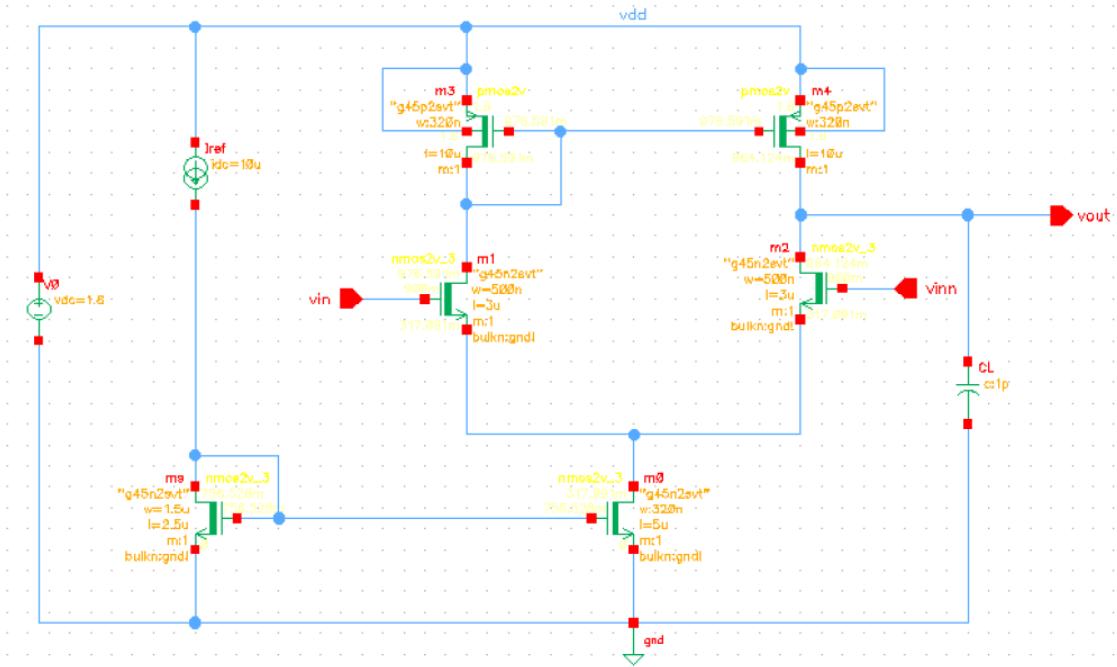


Fig 3.3.11 Schematic for a 5T – OTA with capacitive load (Differential amplifier).

5-Transistor Operational Transconductance Amplifier schematic: [VDD = 1.8V; Vin = 1.2V; Iss = 1uA; Vout = 1.2V]

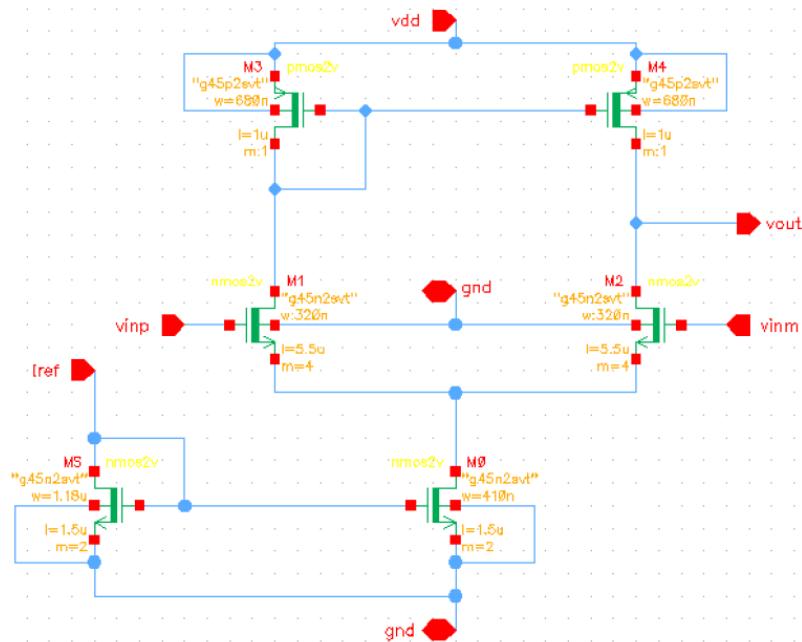


Fig 3.3.12 Schematic for a 5T – OTA for a 1.5V LDO regulator.

5-Transistor Operational Transconductance Amplifier Test Bench schematic:

[VDD = 1.8V; Vin = 1.2V; Iss = 4uA; Vout = 1.2V]

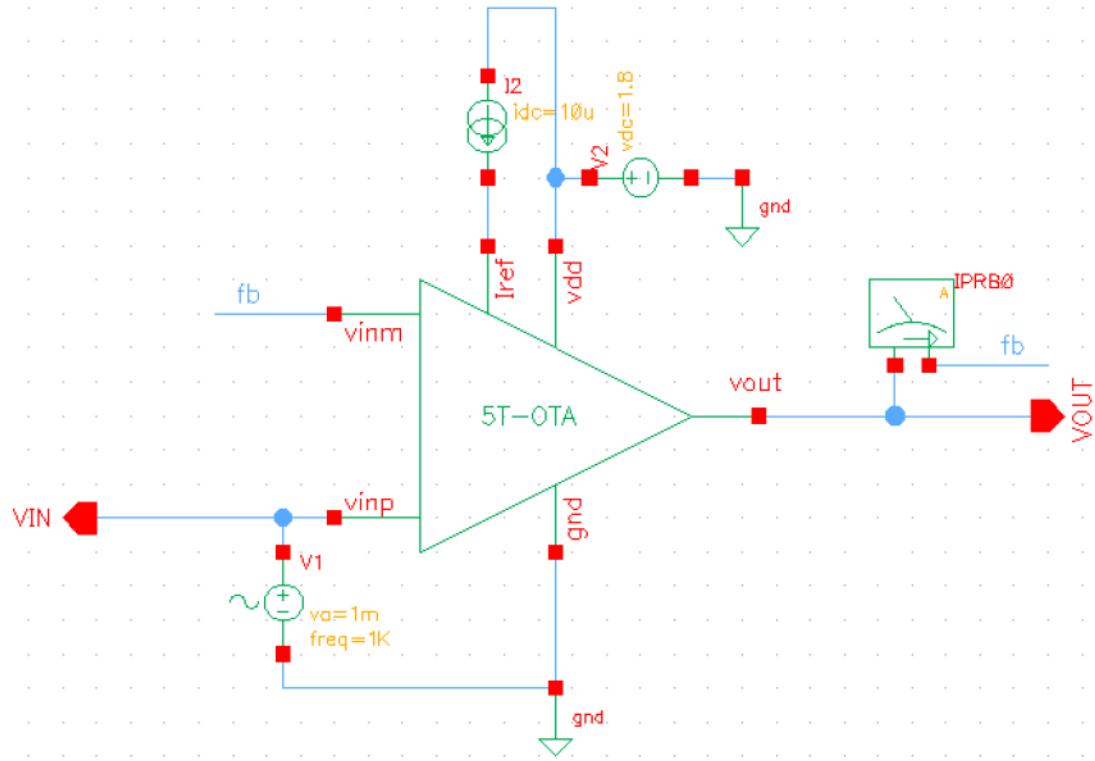


Fig 3.3.13 Schematic with symbol for a 5T – OTA Testbench for a 1.5V LDO regulator.

5-Transistor Operational Transconductance Amplifier schematic: [VDD = 1.8V; Vin = 1.2V; Iss = 4uA; Vout = 1.5V]

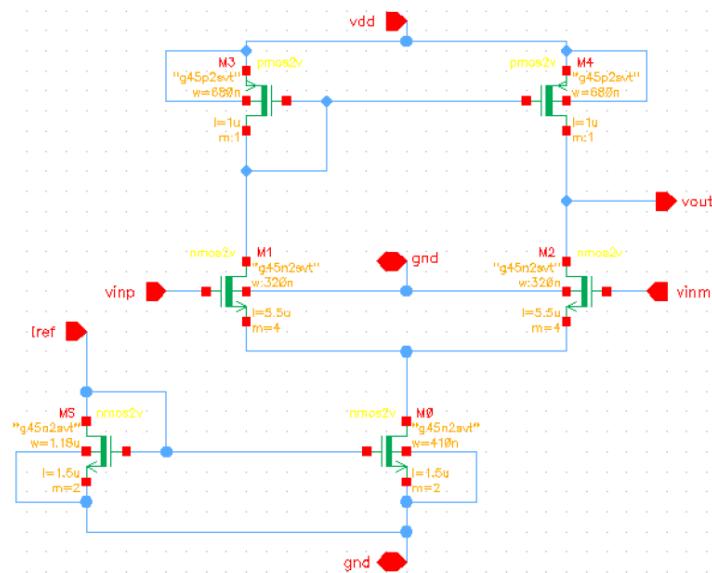


Fig 3.3.14 Schematic for a 5T – OTA for a 1.8V LDO regulator.

5-Transistor Operational Transconductance Amplifier schematic: [VDD = 2V; Vin = 1.2V; Iss = 4uA; Vout = 1.5V]

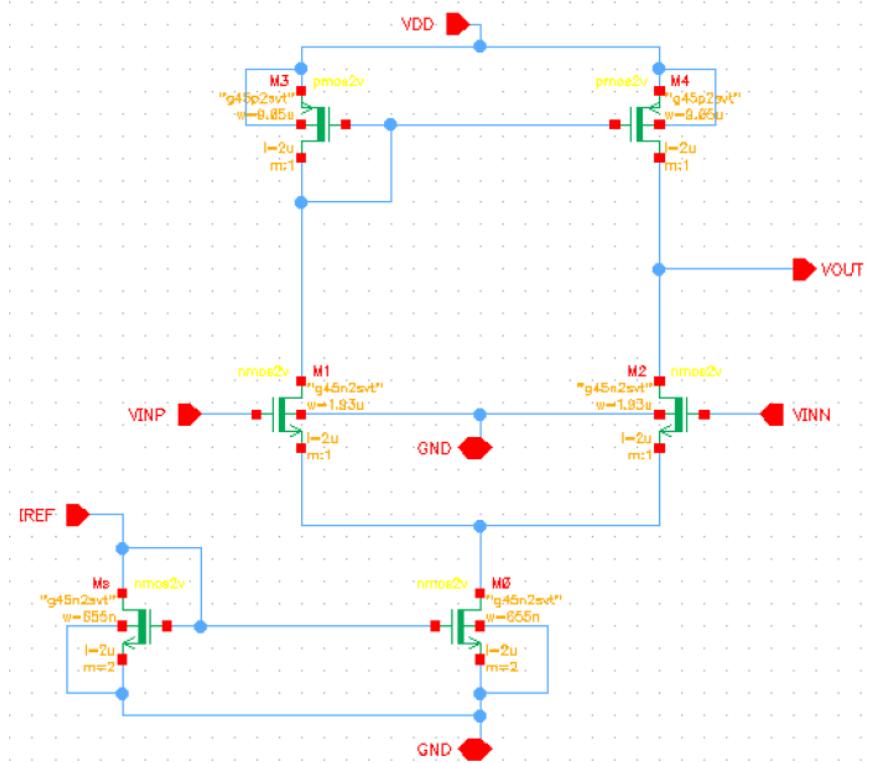


Fig 3.3.15 Schematic for a 5T – OTA for a 1.8V LDO regulator.

I] 2 -Stage Operational Amplifier (Opamp) schematic (Vin = 0.9V; Vout = 0.9V; VDD = 1.8V; Iss = 25uA; Iref = 10uA; CL = 10pF; UGB at 5MHz):

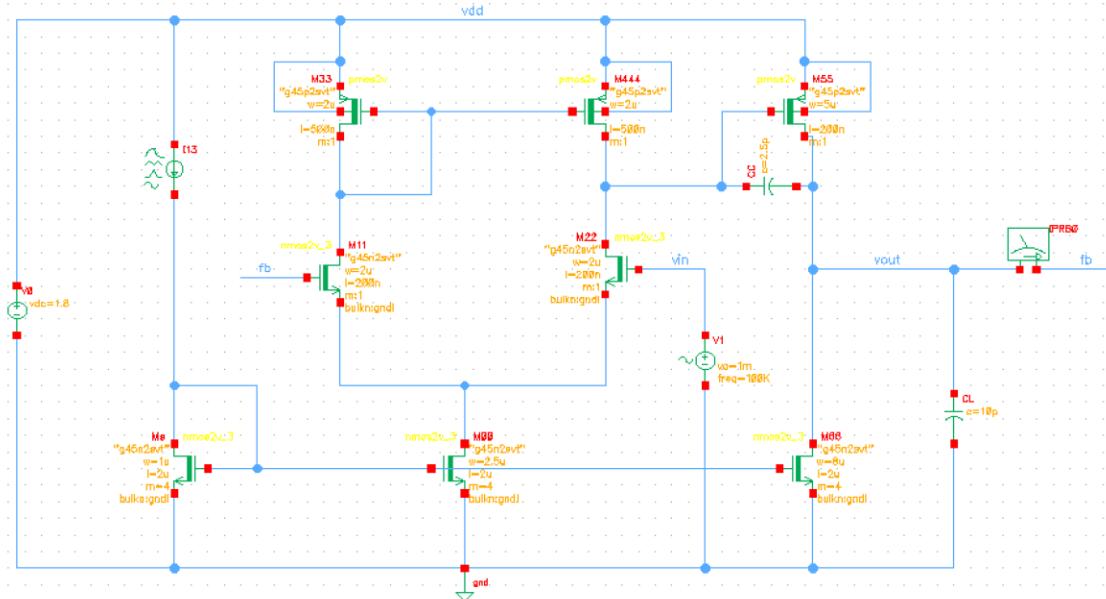


Fig 3.3.16 Schematic for a 0.9V 2-stage opamp with Miller capacitor compensation and load.

**II] 2 -Stage Operational Amplifier (Opamp) schematic (Vin = 0.9V; Vout = 0.9V;
VDD = 1.8V; Iss = 25uA; Iref = 10uA; CL = 10pF; UGB at 5MHz):**

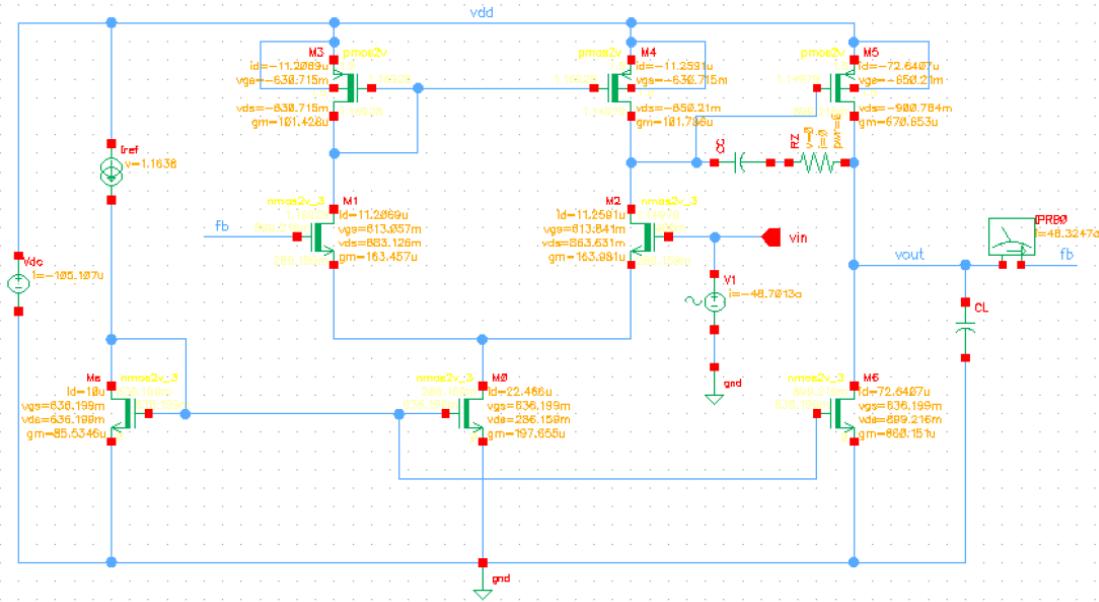


Fig 3.3.17 Schematic for a 0.9V 2-stage opamp with Miller capacitor, Nulling resistor, and load.

**III] 2 -Stage Operational Amplifier (Opamp) (for an LDO) schematic (Vin = 1.2V;
Vout = V; VDD = 1.8V; Iss = 4uA; Iref = 10uA; UGB at 5MHz):**

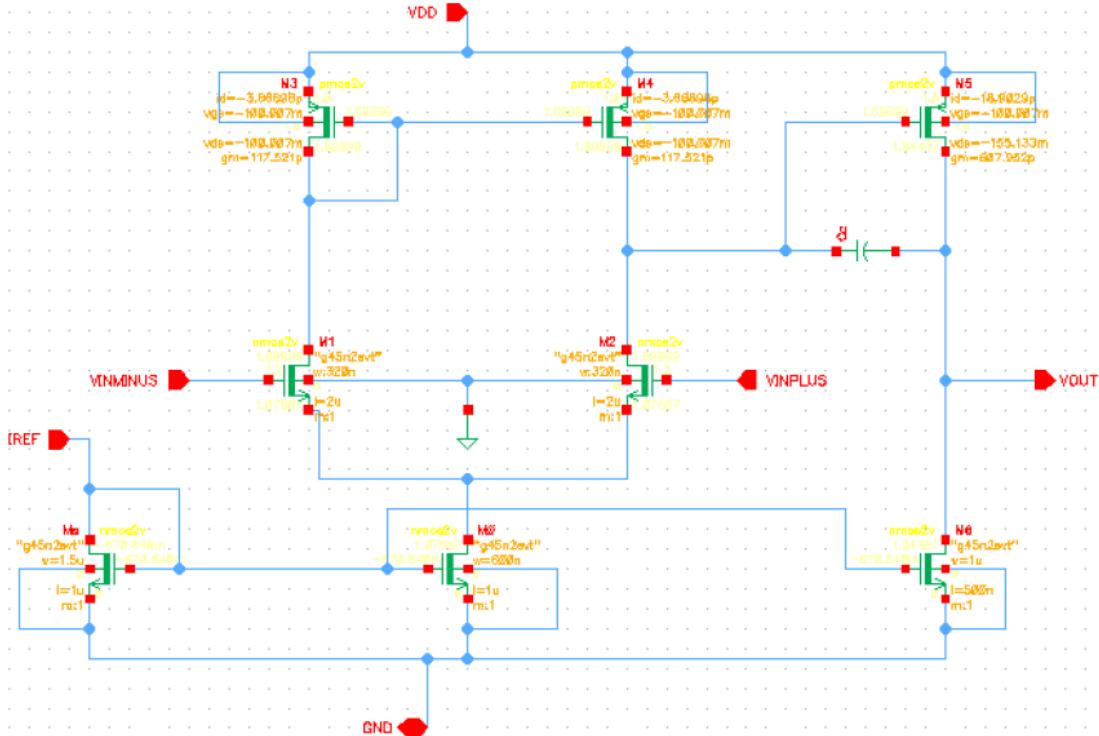


Fig 3.3.18 Schematic for a 1.2V 2-stage opamp with Miller capacitor.

2 -Stage Operational Amplifier (Opamp) Testbench (for an LDO) schematic ($V_{in} = 1.2V$; $V_{out} = 1.2V$; $V_{DD} = 1.8V$; $I_{ss} = 4\mu A$; $I_{ref} = 10\mu A$; UGB at 5MHz):

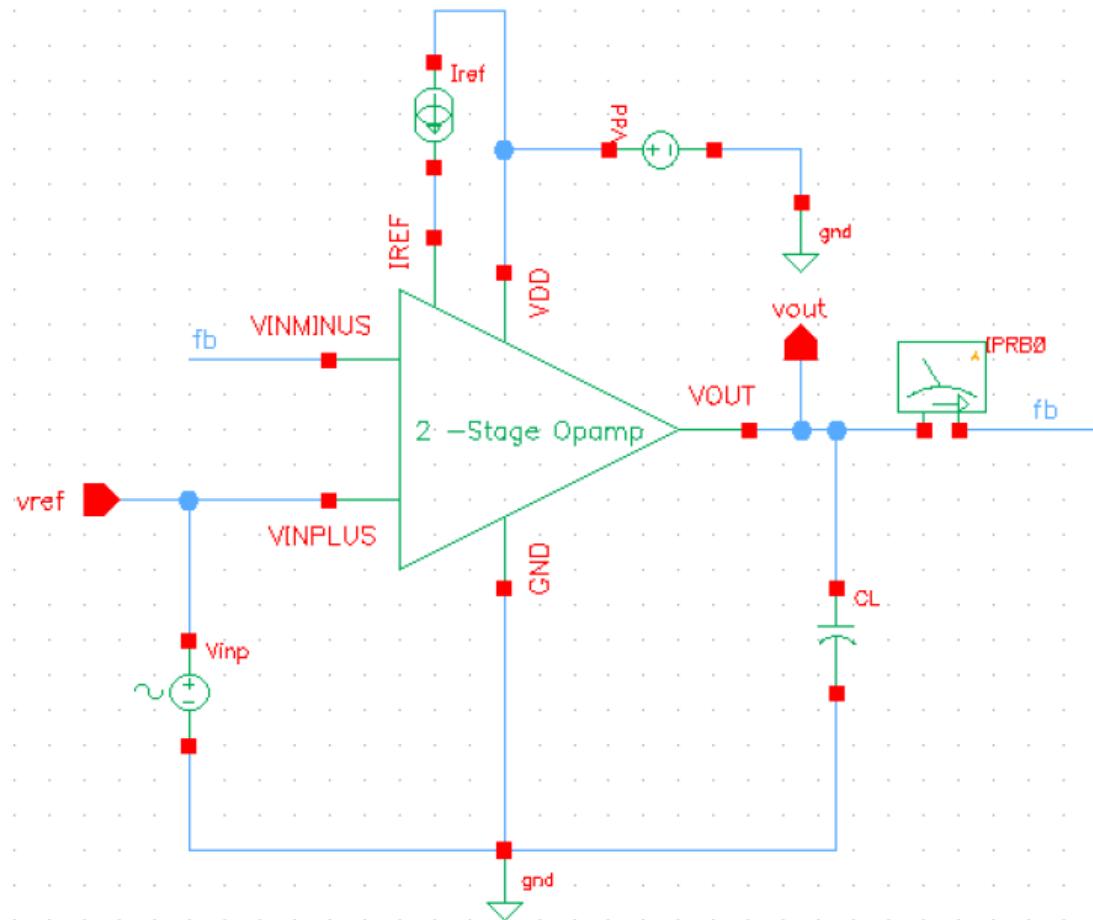


Fig 3.3.19 Schematic for a 2-stage opamp testbench
with a load capacitor.

Low Dropout Regulator (LDO) schematic (Vref = 1.2V; Vout = 1.5V; VDD = 1.8V; Iquisent = 10uA; Iref = 10uA; CL = 0.8uF to 1.2uF; IL = 10uA to 1mA):

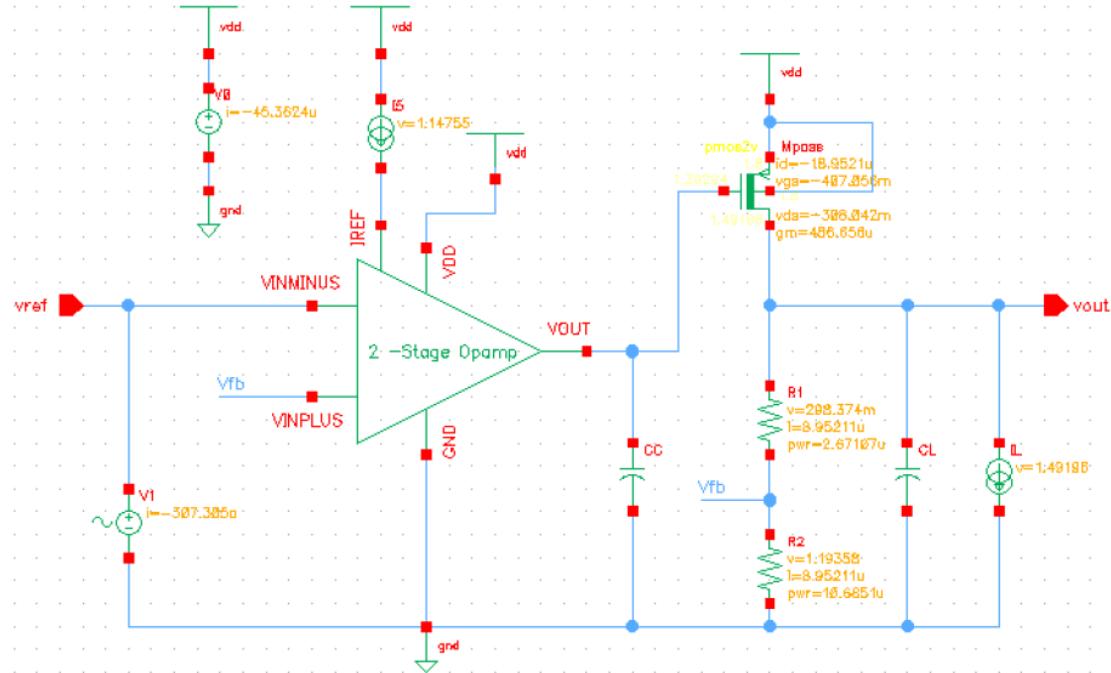


Fig 3.3.20 Schematic for a 1.5V PMOS Driver LDO with a load capacitor and current.

II] Low Dropout Regulator (LDO) schematic (Vref = 1.2V; Vout = 1.5V; VDD = 1.8V; Iquisent = 10uA; Iref = 10uA; CL = 0.8uF to 1.2uF; IL = 9uA to 1.1mA):

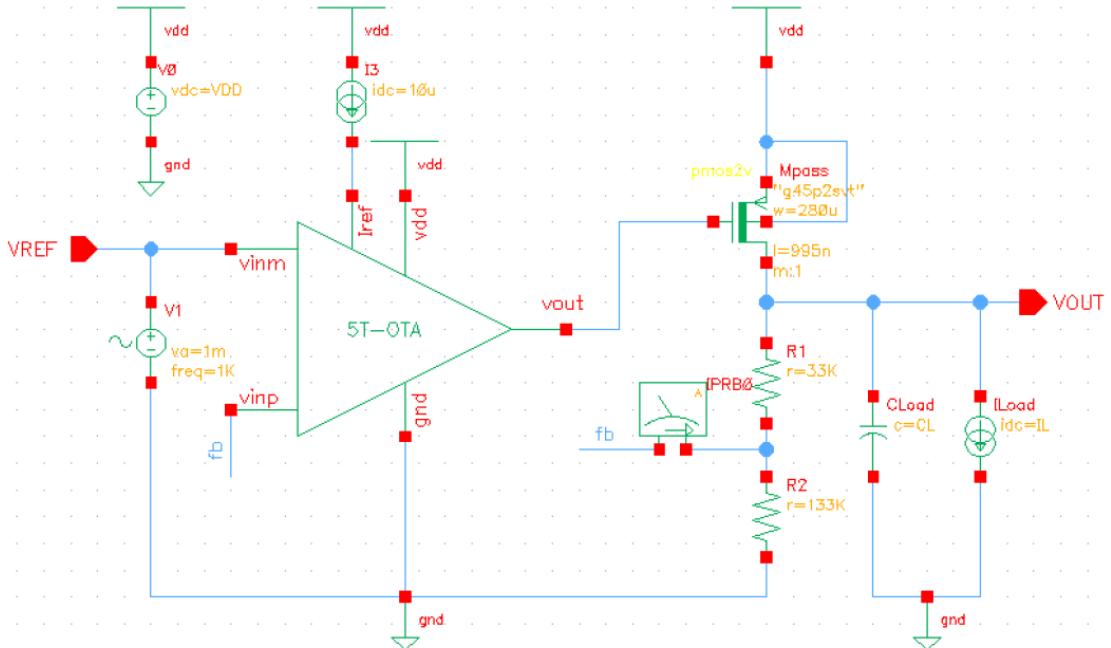


Fig 3.3.21 Schematic for a 1.5V PMOS Driver LDO with a load capacitor and current.

III] Low Dropout Regulator (LDO) schematic ($V_{ref} = 1.2V$; $V_{out} = 1.8V$; $V_{DD} = 2V$; $I_{quiescent} = 100\mu A$; $I_{ref} = 10\mu A$; $C_L = 25\text{pF}$; $I_L = 10\mu A$ to 15mA):

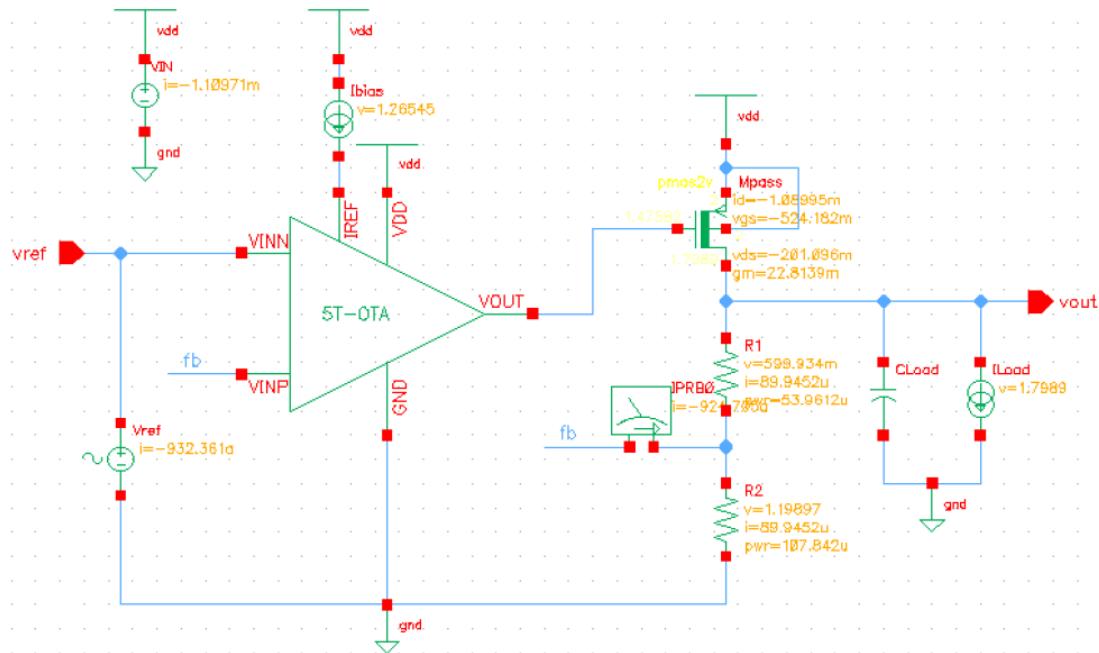


Fig 3.3.22 Schematic for a 1.8V PMOS Driver LDO
with a load capacitor and current.

**I] Bandgap Reference (BGR or Voltage reference) [Banba 1999 Sub-1V design
schematic ($V_{in} = 1.2V$; $V_{out} = 1.2V$; $V_{DD} = 2V$):**

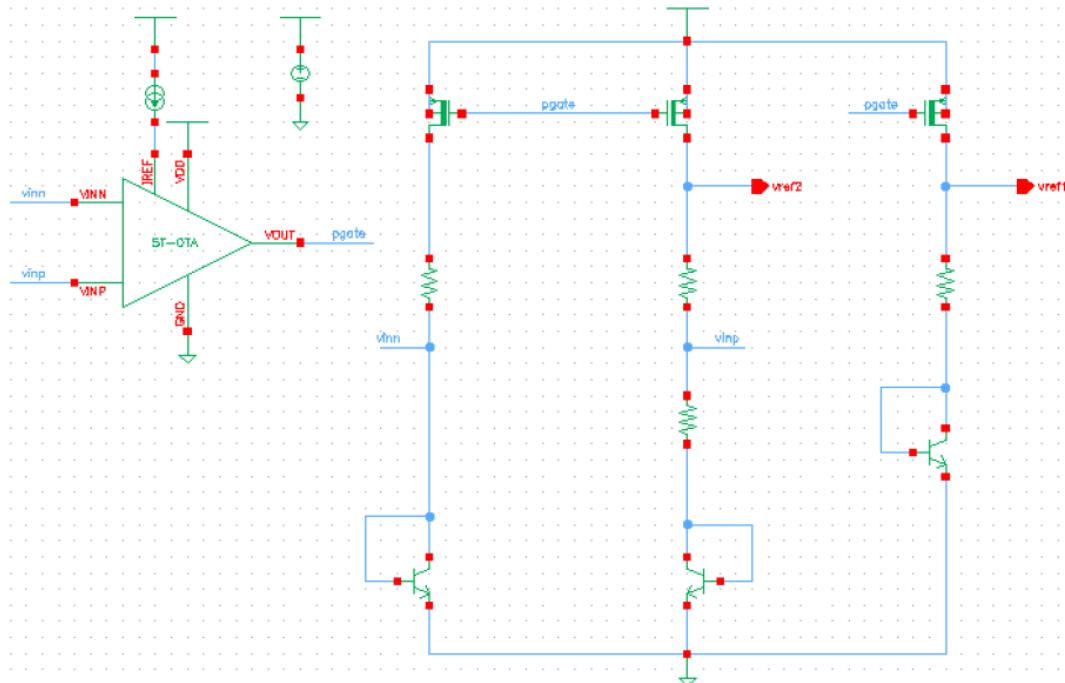


Fig 3.3.23 Schematic for a 1.2V Banba Bandgap
reference circuit design.

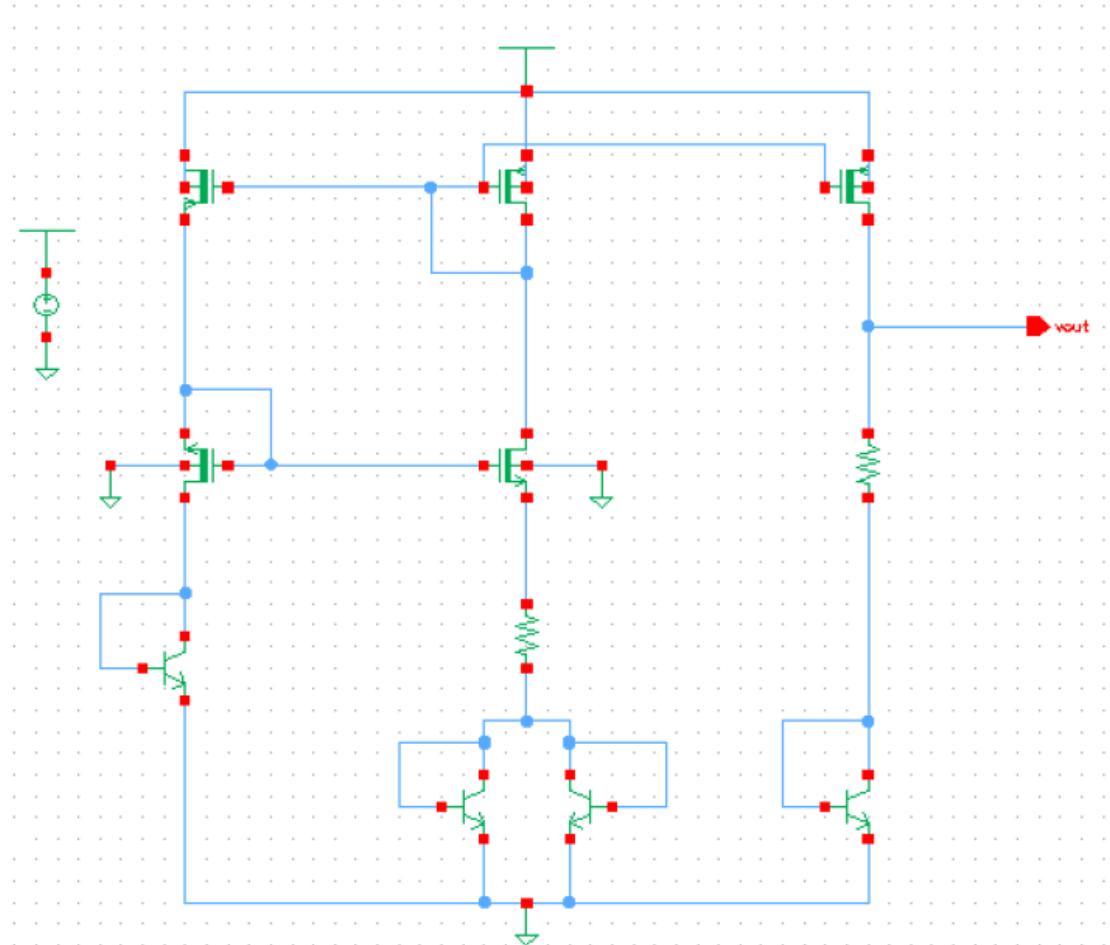
II] Bandgap Reference (BGR or Voltage reference) [general design] schematic**(Vin = 1.2V; Vout = 1.2V; VDD = 2V:**

Fig 3.3.24 Schematic for a 1.2V General Bandgap reference circuit design.

Chapter 4

Results and Discussion

4.1 Simulation results and analysis for the Analog blocks

The simulations were performed on the Analog Design Environment L & XL tool included in the Cadence Virtuoso design suite. The simulator chosen for all the simulations is spectre which is a very powerful simulator specially designed for these types of simulations.

A wide range of simulations are present in the ADE L & XL spectre, which include:

- DC simulation
- AC simulation
- Transient simulation
- Pole-zero simulation
- Noise simulation
- Stability analysis simulation
- DC matching simulation, and many more.

For most of the designs, DC, AC, Transient, stability and noise simulations are more than enough to analyze all the designs.

These are a few simulations for example:

PMOS I_D vs V_{GS} DC simulation & PMOS I_D vs V_{DS} DC simulation:

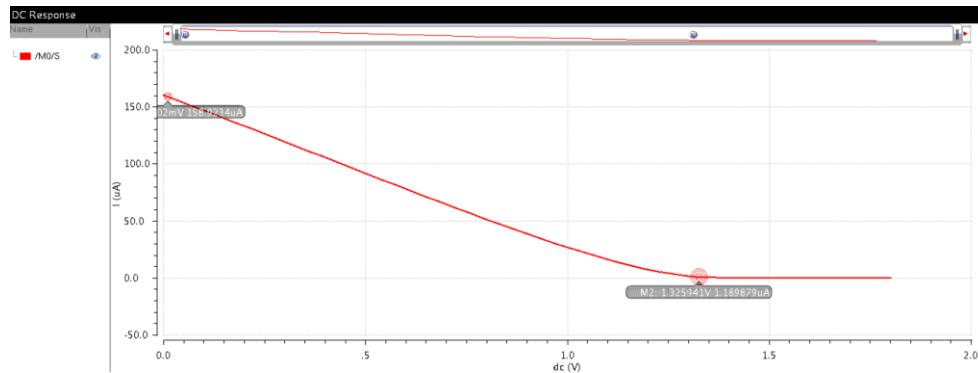


Fig 4.1.1 Graph for the I_D vs V_{GS} characteristics for a PMOS.

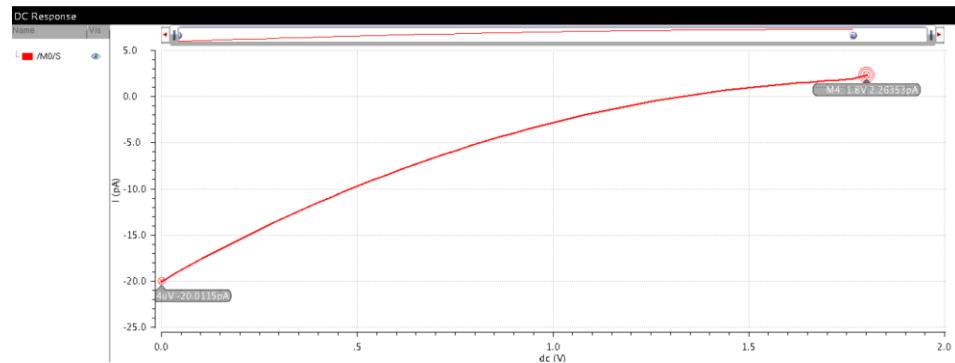


Fig 4.1.2 Graph for the I_D vs V_{DS} characteristics for a PMOS.

NMOS I_D vs V_{GS} DC simulation & NMOS I_D vs V_{DS} DC simulation:

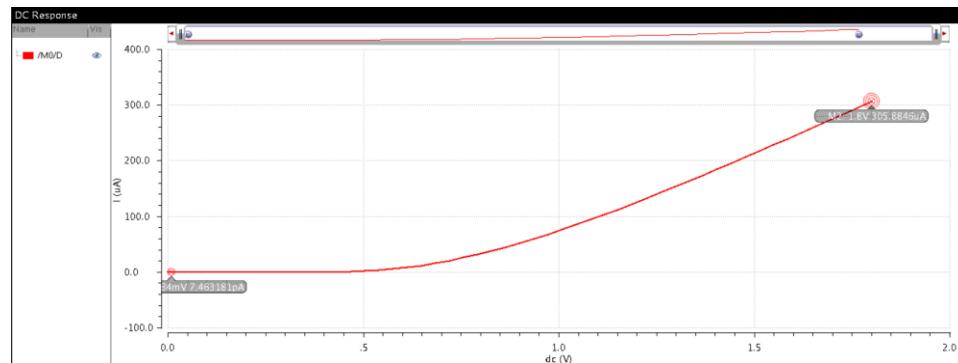


Fig 4.1.3 Graph for the I_D vs V_{GS} characteristics for a NMOS.

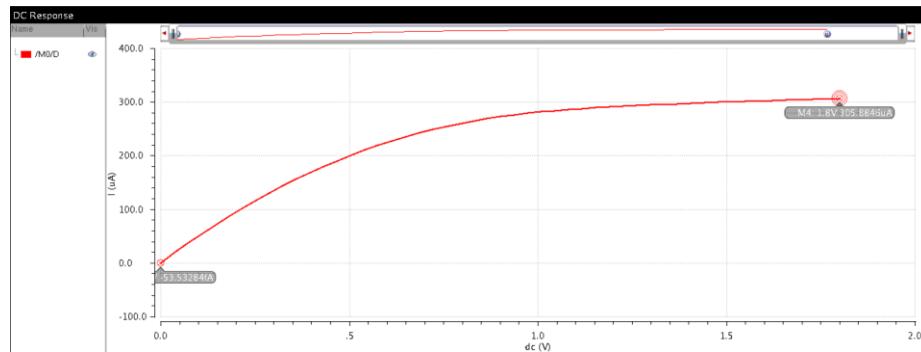


Fig 4.1.4 Graph for the I_d vs V_{GS} characteristics for a NMOS.

CMOS Inverter Transient simulation [0-100ns] ($V_{inDC} = 1.8V$, Pulse input Period = 20ns, Rise/Fall time = 50ps; Amplitude = 1V):

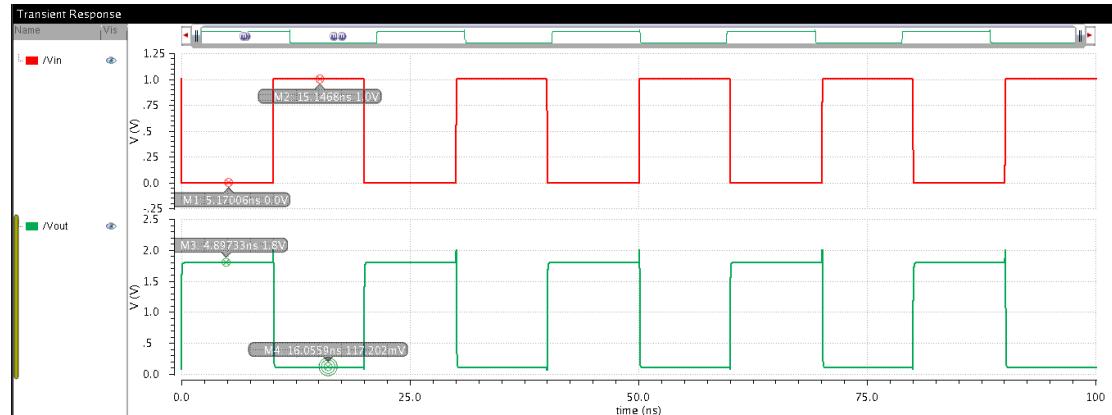


Fig 4.1.5 Graph for the CMOS Inverter.

Single-stage CSSD Amplifier Transient simulation [0-100us] ($V_{inDC} = 800mV$, $V_{inAC} = 100KHz$ Sine wave w/2mVpp amplitude; Gain = 2.16):

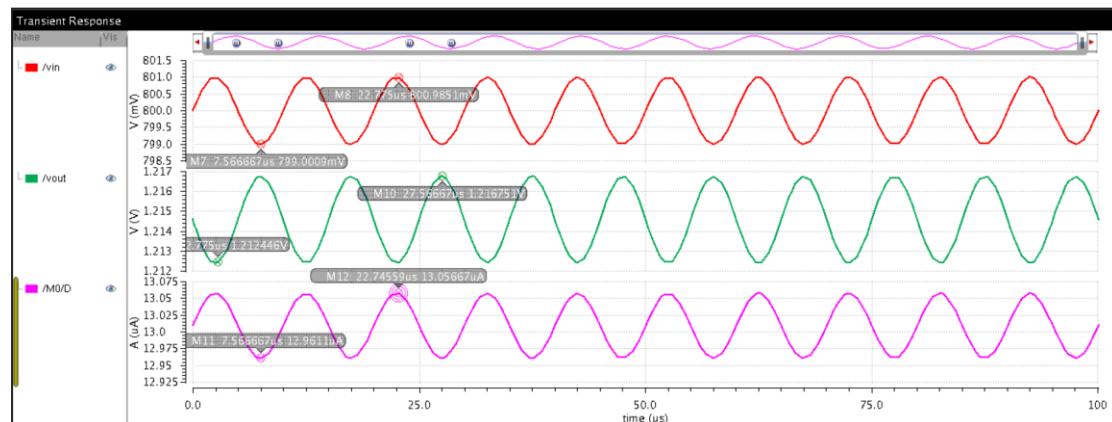


Fig 4.1.6 Resultant waveforms for the V_{in} vs V_{out} and I_d of a CSSD amplifier.

Single-stage CSSD Amplifier DC simulation (Annotated results):

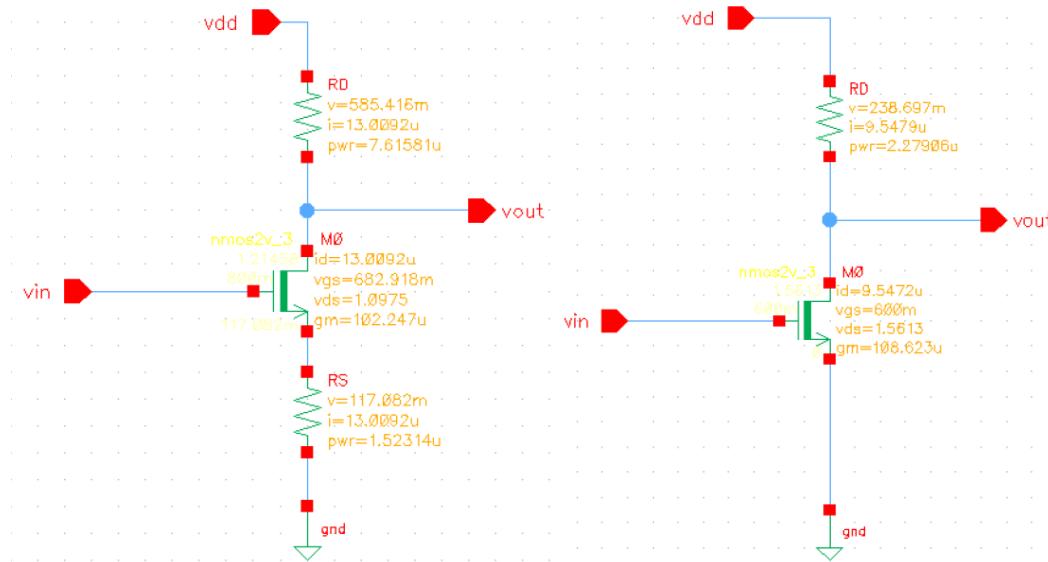


Fig 4.1.7 Resultant DC operating points for a CSSD amplifier.

Fig 4.1.8 Resultant DC operating points for a CS amplifier.

Single-stage CSSD Amplifier ADE XL ($\mathbf{R_D}$) Transient Corner simulation [0-100us] ($V_{inDC} = 800\text{mV}$, $V_{inAC} = 100\text{KHz}$ Sine wave w/2mVpp amplitude):

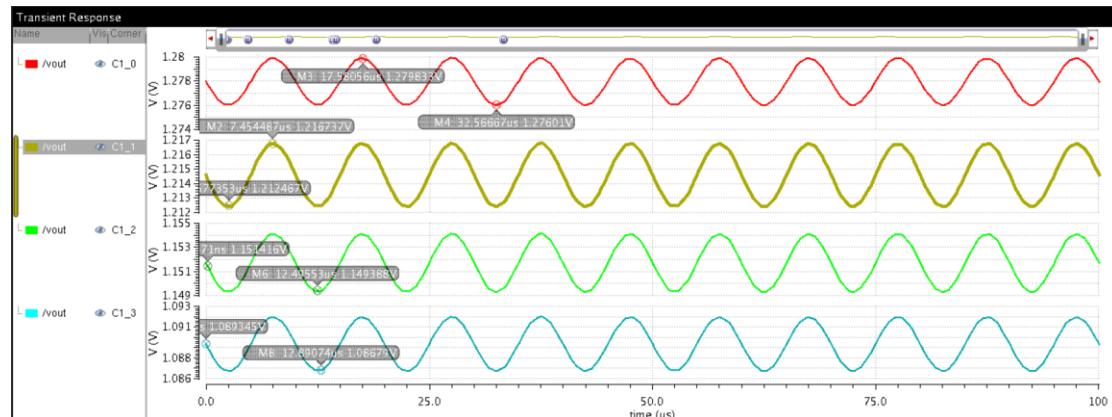


Fig 4.1.9 Resultant waveforms for the V_{out} at multiple corners of R_D for CSSD Amplifier.

Single-stage CS Amplifier ADE XL (R_D) Transient Corner simulation [0-10ms]

($V_{inDC} = 800mV$, $V_{inAC} = 1KHz$ Sine wave w/2mVpp amplitude):

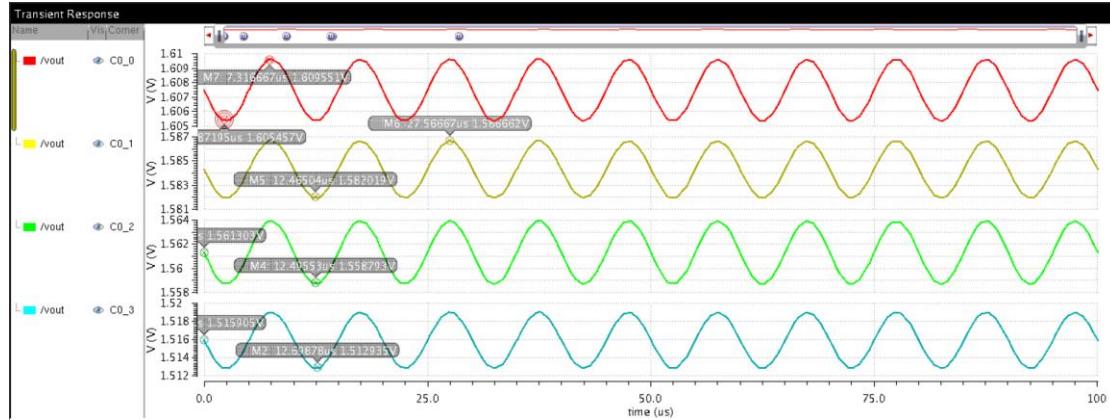


Fig 4.1.10 Resultant waveforms for the Vout at multiple corners of RD for CS Amplifier.

1:10 Current Mirror DC simulation (Annotated results):

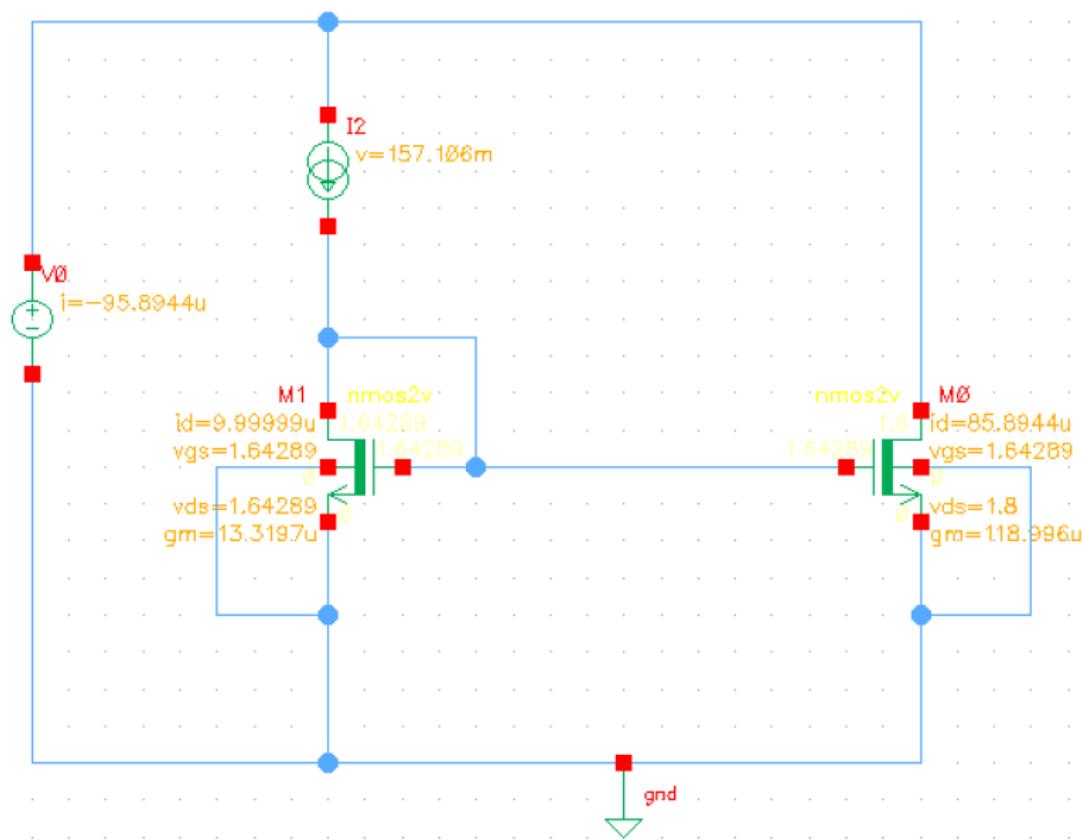


Fig 4.1.11 Resultant DC operating points for a basic 1:10 current mirror.

1:10 Current Mirror Transient simulation:

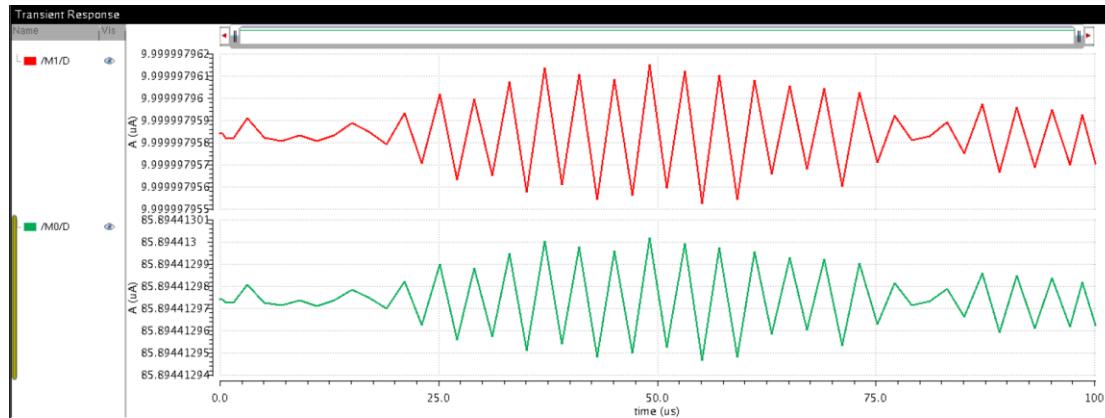


Fig 4.1.12 Resultant Transient simulation for a basic 1:10 current mirror.

I] 5-T OTA ($V_{out} = 0.7V$; $V_{inDC} = 1.2V$, $V_{inAC} = 1\text{KHz}$ Sine wave w/2mVpp amplitude):

5-T OTA DC simulation (Annotated results):

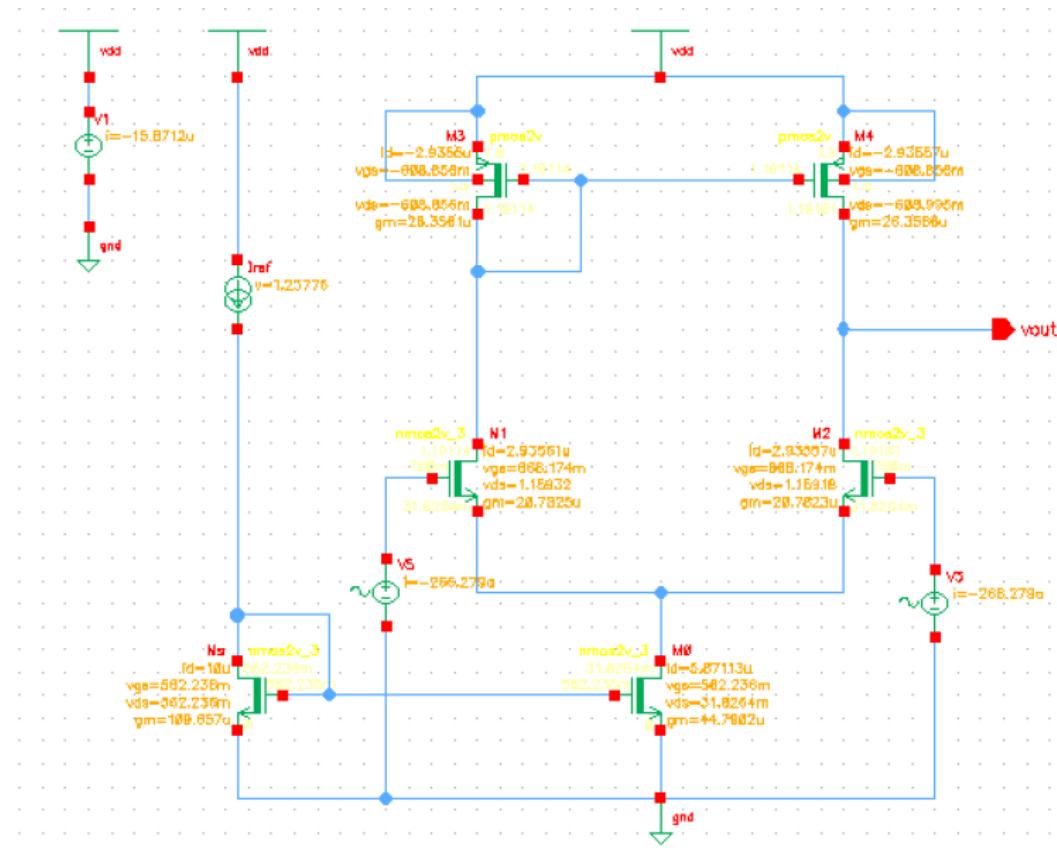


Fig 4.1.13 Resultant DC operating points of a 5T-OTA.

5-T OTA Transient simulation [0-10ms] (Vin_{DC} = 700mV, Vin_{AC} = 1KHz Sine wave w/2mVpp amplitude): [Gain = 52.6]

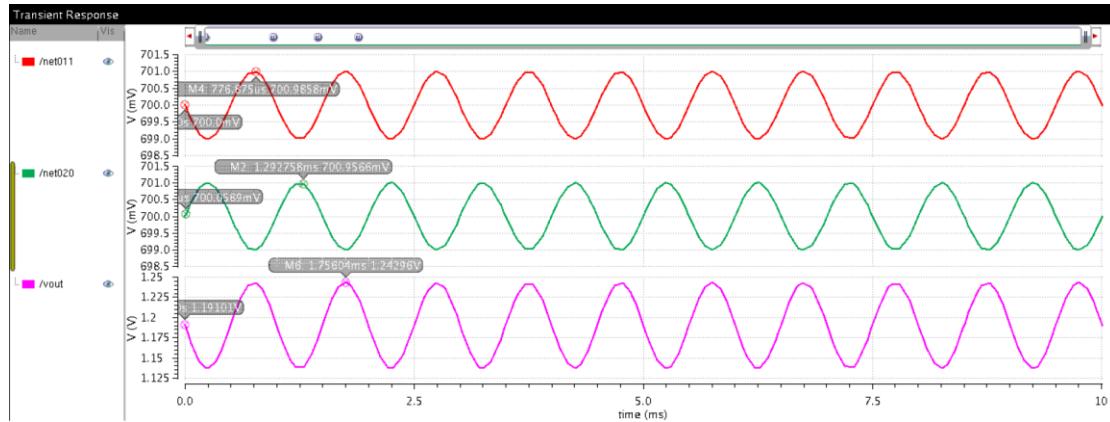


Fig 4.1.14 Resultant waveforms for the Vin+, Vin- & V_{out} of a 5T-OTA.

AC Response simulation [1-10GHz]: [Gain = 52.73]

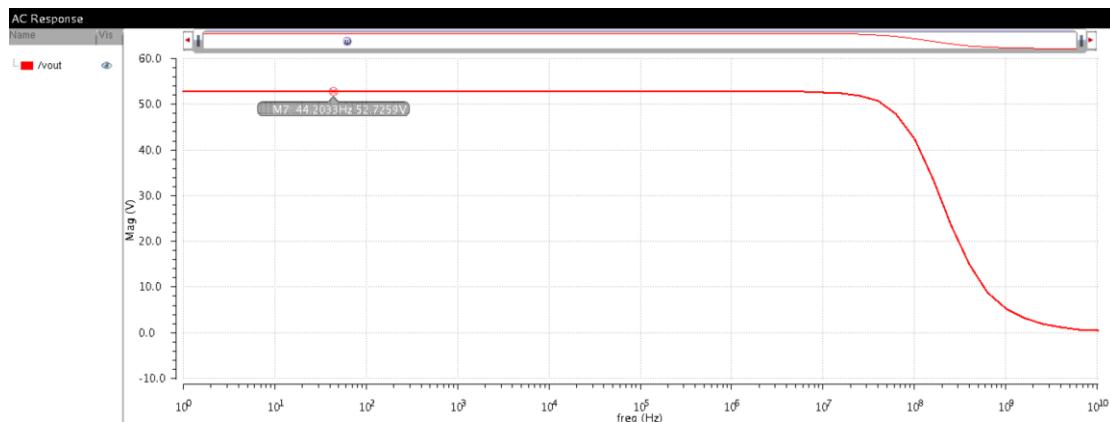


Fig 4.1.15 Resultant waveforms for the AC Response of a 5T-OTA.

Stability response (1 to 100GHz) - Magnitude and Phase plots: (LG = 28.31dB; PM = 90.91°; UGB at 412.78MHz):

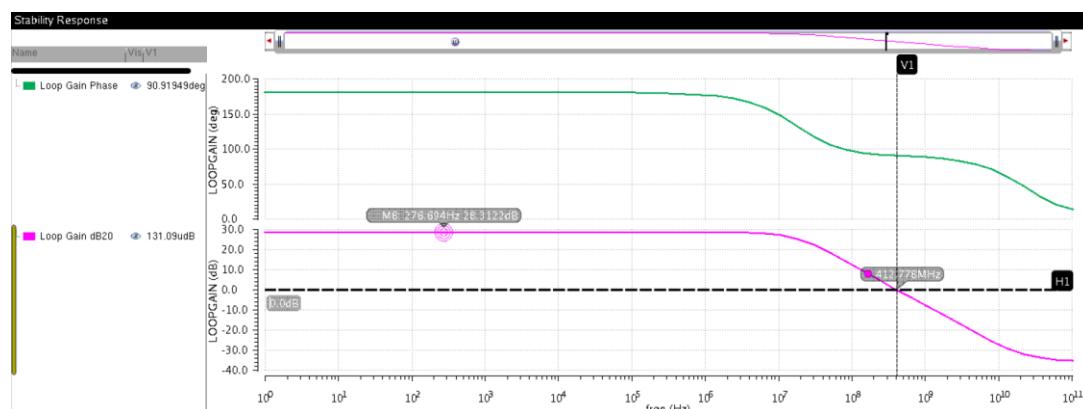


Fig 4.1.16 Resultant waveforms for the Stability Response of a 5T-OTA.

II] 5-T OTA ($V_{out} = 1.2V$; $V_{inDC} = 1.2V$, $V_{inAC} = 1\text{KHz Sine wave w/2mVpp amplitude}$):

5-T OTA DC simulation (Annotated results):

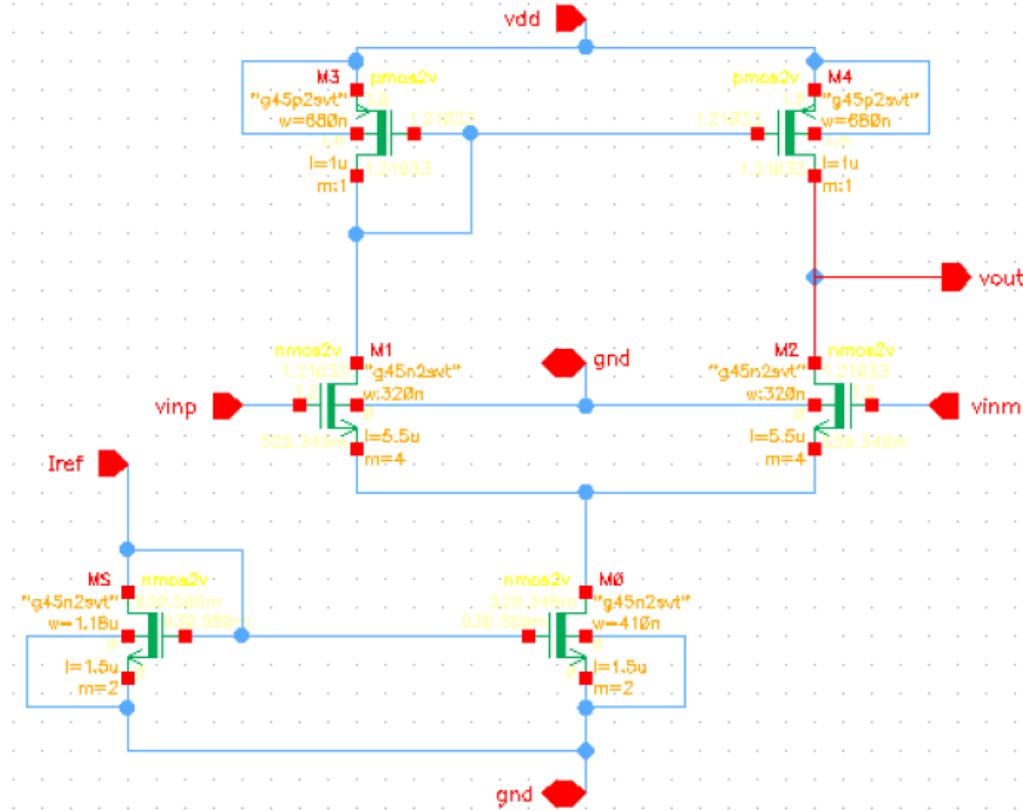


Fig 4.1.17 Resultant DC operating points of a 5T-OTA.

5-T OTA Transient simulation [0-10ms] ($V_{inDC} = 1.2V$, $V_{inAC} = 1\text{KHz Sine wave w/2mVpp amplitude}$): [Gain = 58.25]

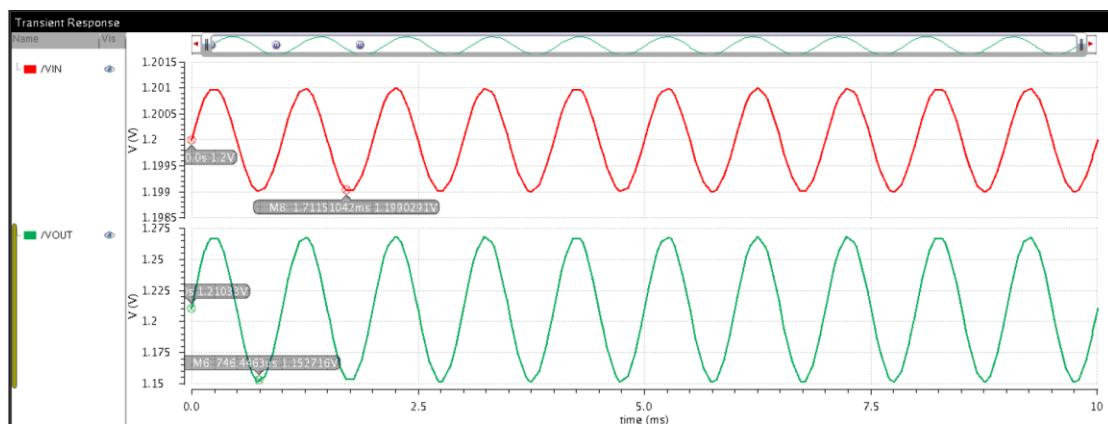


Fig 4.1.18 Resultant waveforms for the V_{in} and V_{out} of a 5T-OTA.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

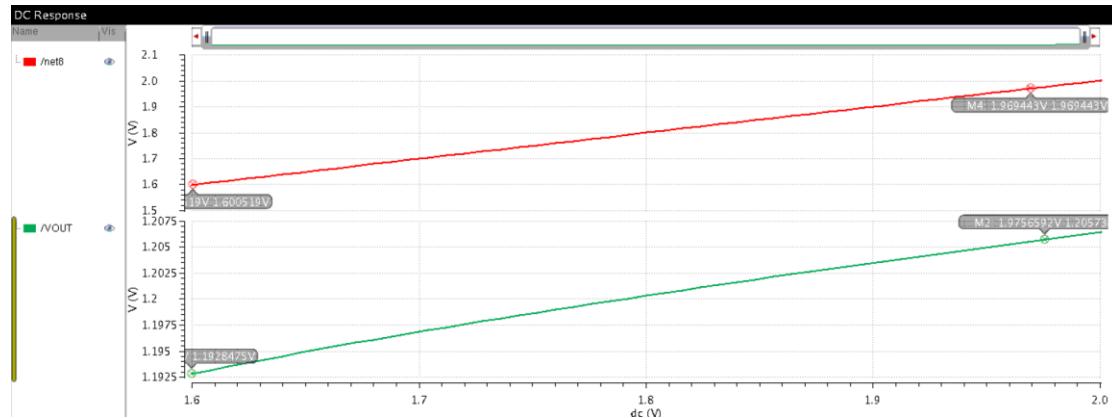


Fig 4.1.19 Resultant waveforms for the VDD v/s Vout sweep of a 5T-OTA.

AC Response simulation [1-10GHz]: [Gain = 58.43]

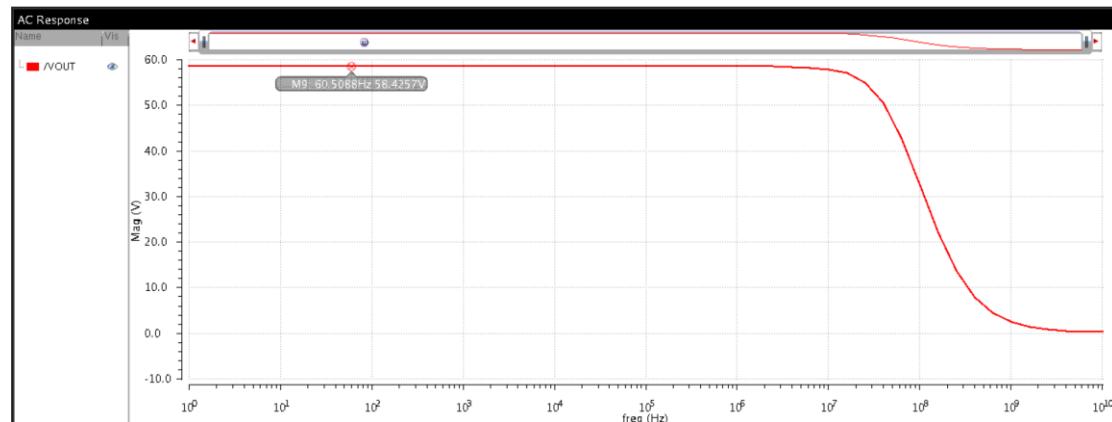


Fig 4.1.20 Resultant waveforms for the AC Response of a 5T-OTA.

Stability response (1 to 10GHz) - Magnitude and Phase plots: (LG = 29.34dB; PM = 83.51°; UGB at 93.95MHz):

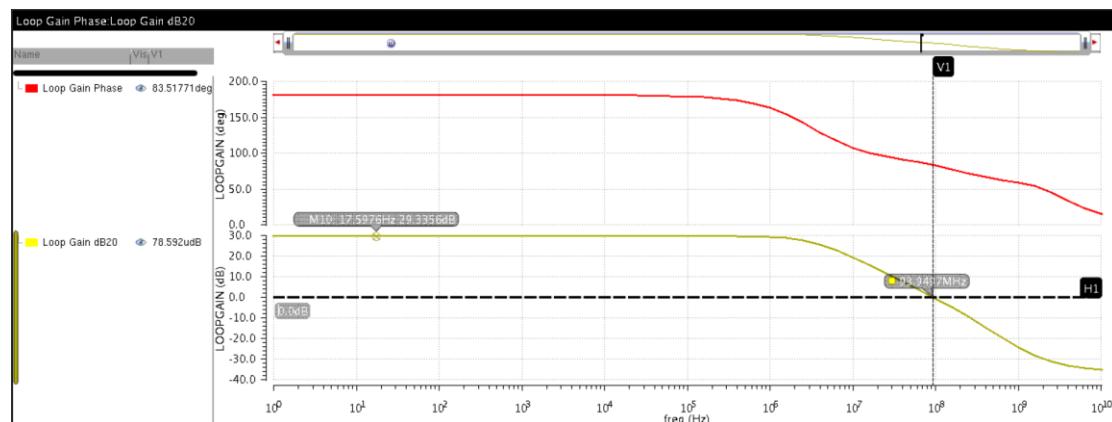


Fig 4.1.21 Resultant waveforms for the Stability Response of a 5T-OTA.

IV] 5-T OTA (Vout = 1.5V; VinDC = 0.7V, VinAC = 1KHz Sine wave w/2mVpp amplitude):

5T-OTA DC simulation (Annotated results):

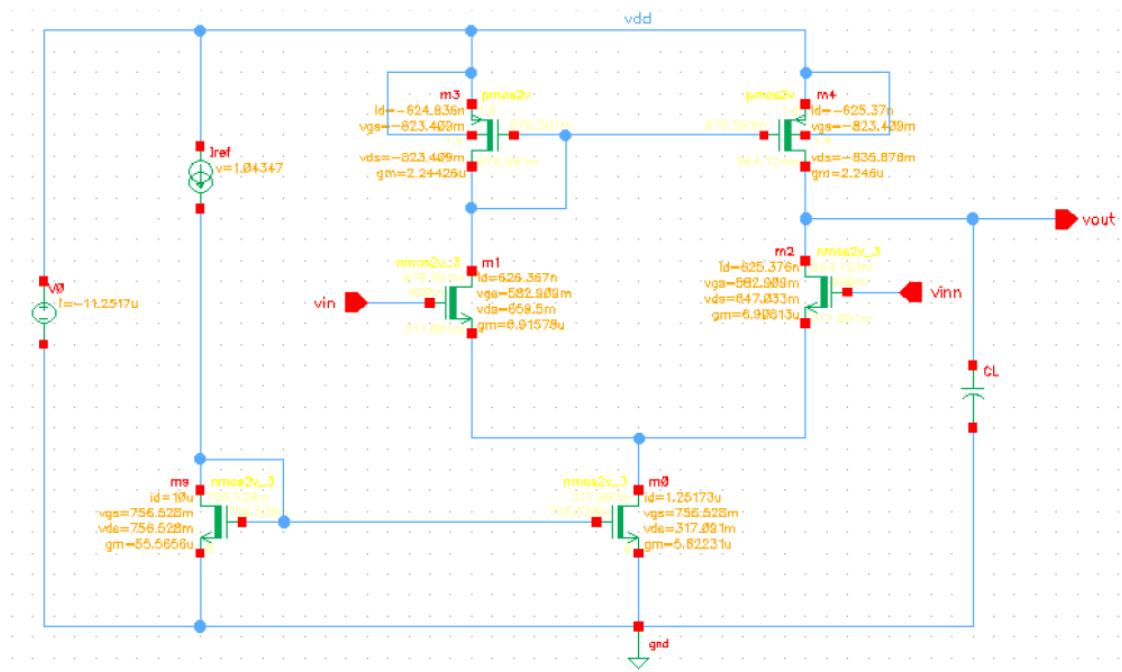


Fig 4.1.22 Resultant DC operating points of a 5T-OTA.

5-T OTA Transient simulation [0-10ms] (VinDC = 900mV, VinAC = 1KHz Sine wave w/2mVpp amplitude): [Gain = 109.5]

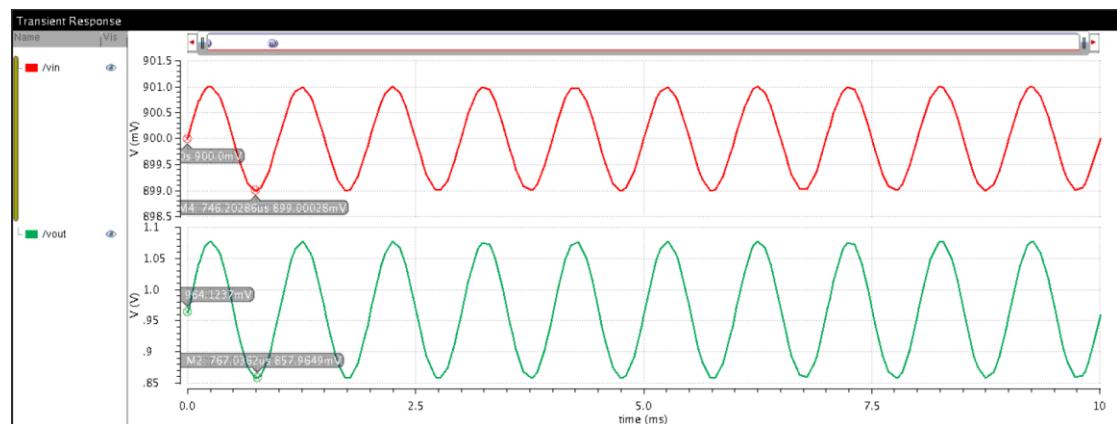


Fig 4.1.23 Resultant waveforms for the V_{in} and V_{out} of a 5T-OTA.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

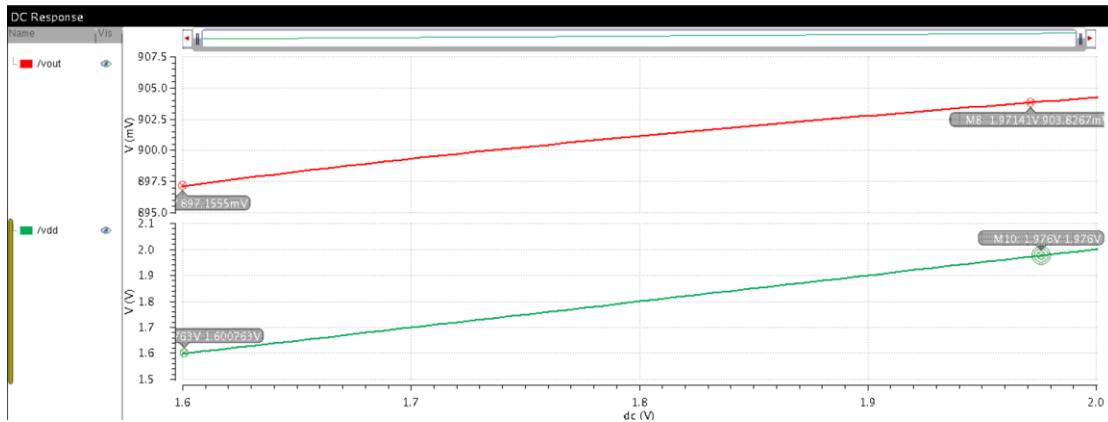


Fig 4.1.24 Resultant waveforms for the VDD v/s Vout sweep of a 5T-OTA.

AC Response simulation (1Hz to 10GHz w/o Feedback): [Gain = 111.28]

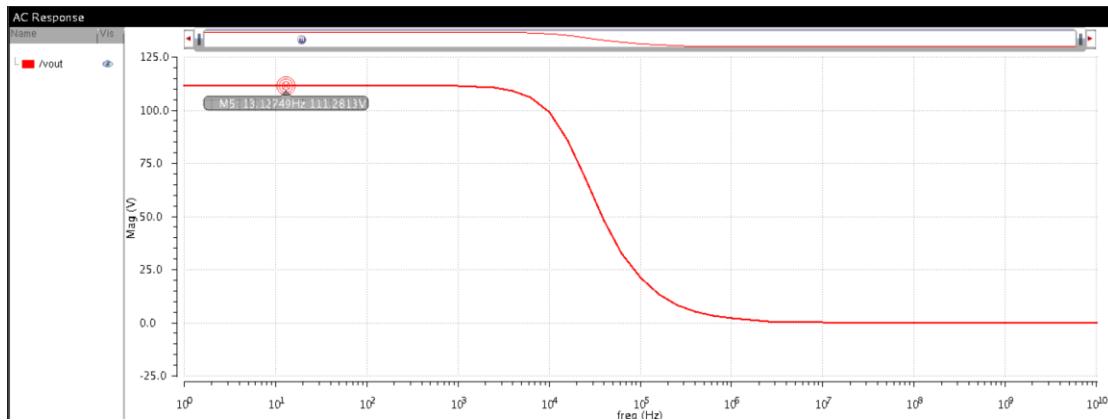


Fig 4.1.25 Resultant waveforms for the AC Response of a 5T-OTA.

Stability response Magnitude and Phase plots, (LG = 34.47dB; PM = 86.68°; UGB at 1.069MHz):

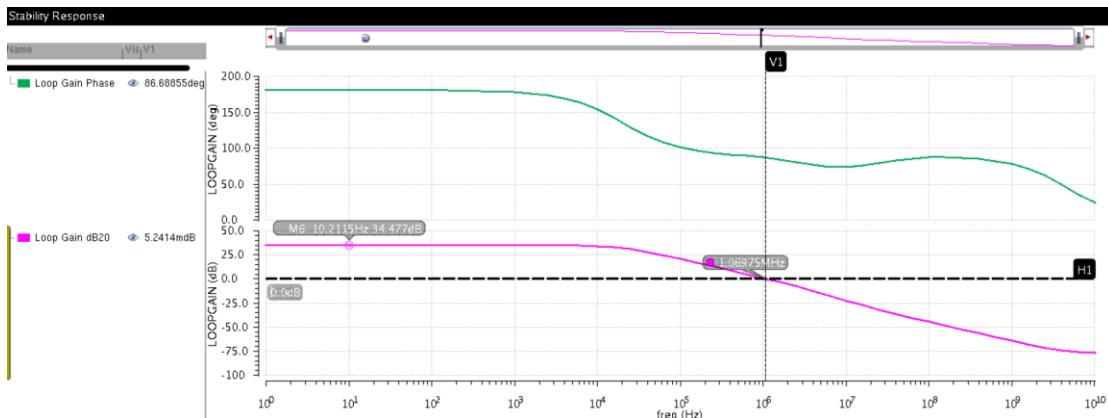


Fig 4.1.26 Resultant waveforms for the Stability Response of a 5T-OTA.

I] 2-Stage Opamp DC Operating point simulation (Results Annotated)

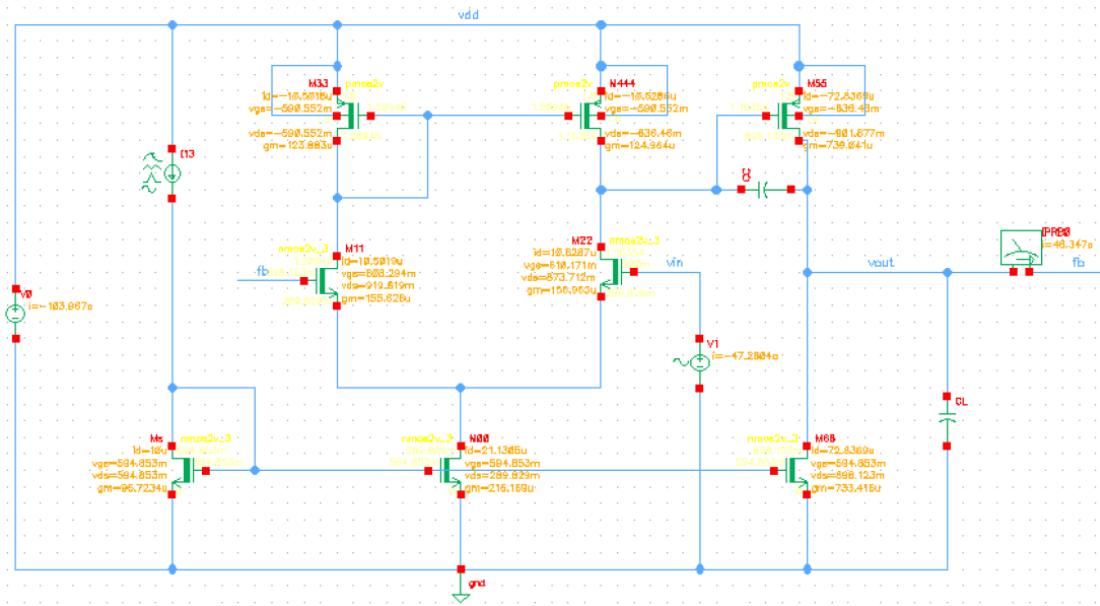


Fig 4.1.27 Resultant DC operating points of a 2-stage opamp with compensation and load.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

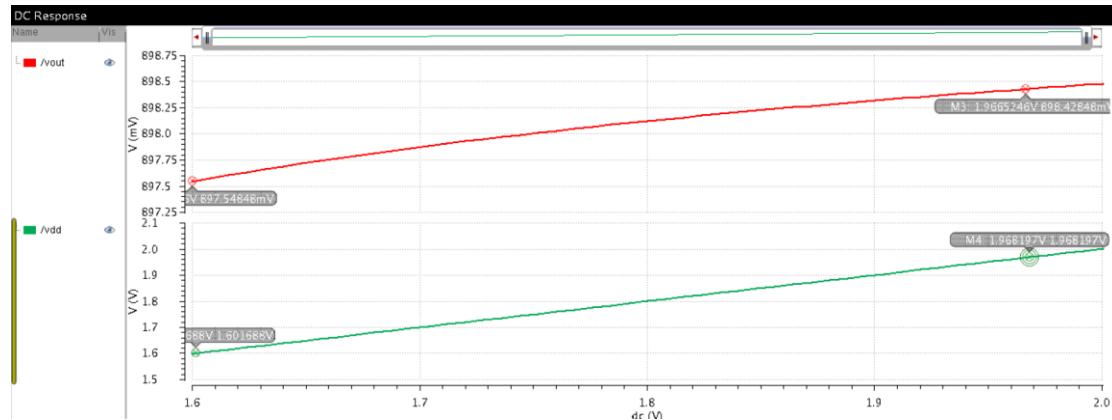


Fig 4.1.28 Resultant waveforms for the VDD v/s V_{out} sweep of a 2-stage opamp with compensation and load.

Transient simulation [0-100us] ($V_{inDC} = 900mV$, $V_{inAC} = 100KHz$ Sine wave w/2mVpp amplitude): [Gain = 0.991]

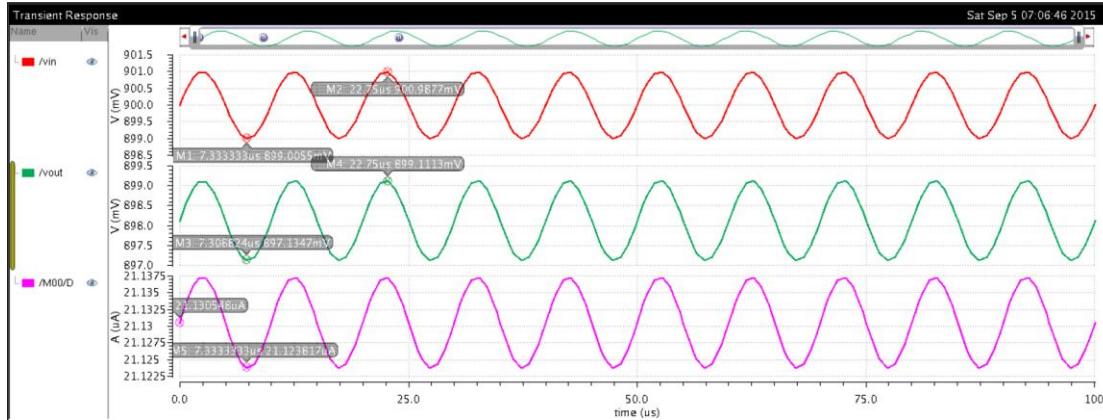


Fig 4.1.29 shows the resultant waveforms for the Vin, ID and Vout of a 2-stage opamp with compensation and load.

Stability response (1 to 100GHz) - Magnitude and Phase plots: (LG = 55.97dB; PM = 48.52°; UGB at 7.93MHz):

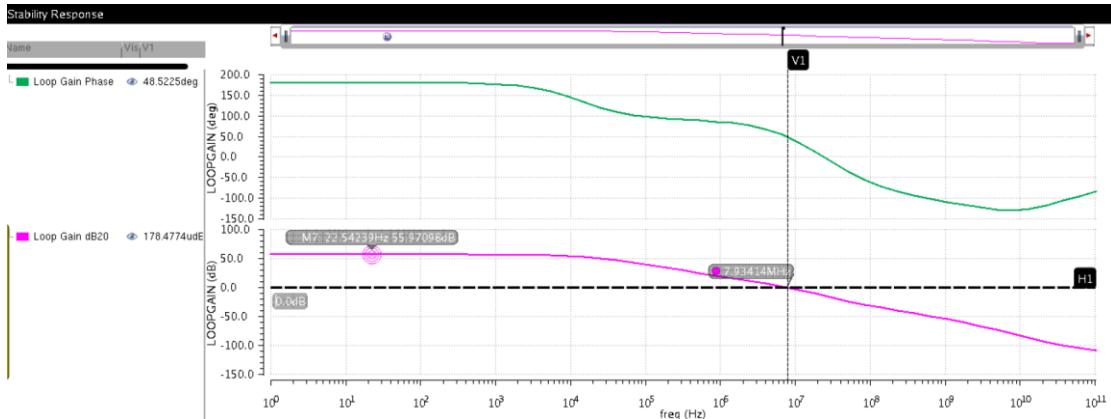


Fig 4.1.30 Resultant waveforms for the Stability Response of a 2-stage opamp with compensation and load.

II] 2-Stage Opamp DC Operating point simulation (Results Annotated)

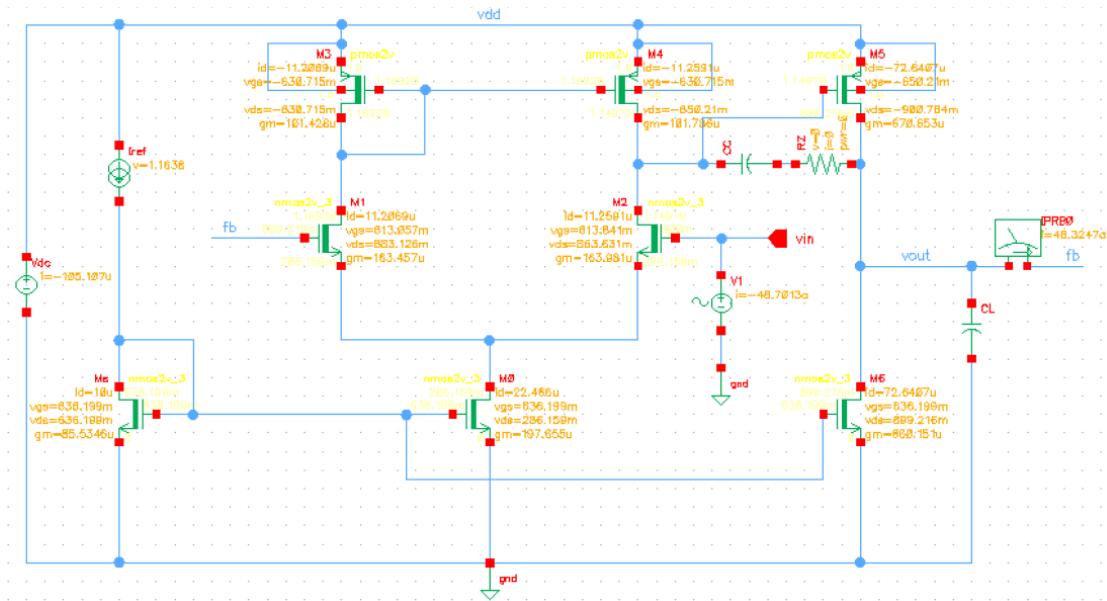


Fig 4.1.31 Resultant DC operating points of a 2-stage opamp with compensation and load.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

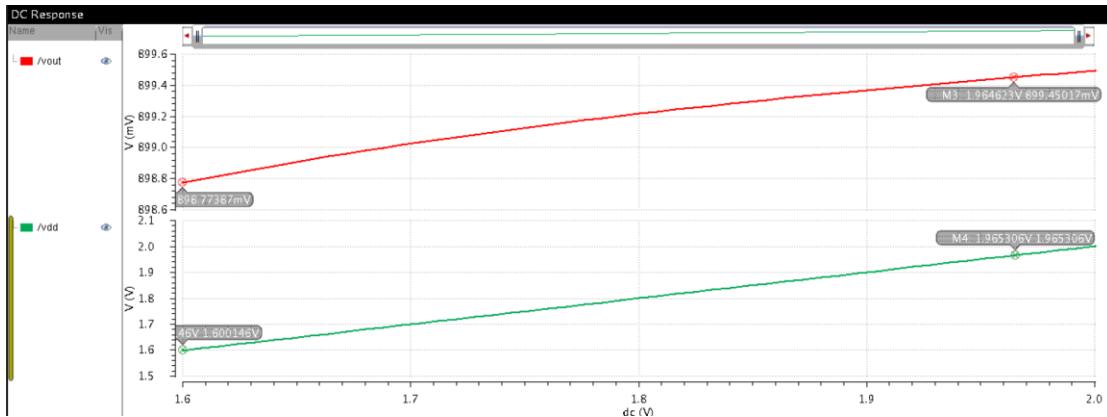


Fig 4.1.32 Resultant waveforms for the VDD v/s V_{out} sweep of a 2-stage opamp with compensation and load.

Transient simulation [0-10ms] ($V_{inDC} = 900mV$, $V_{inAC} = 1KHz$ Sine wave w/2mVpp amplitude): [Gain = 0.99]

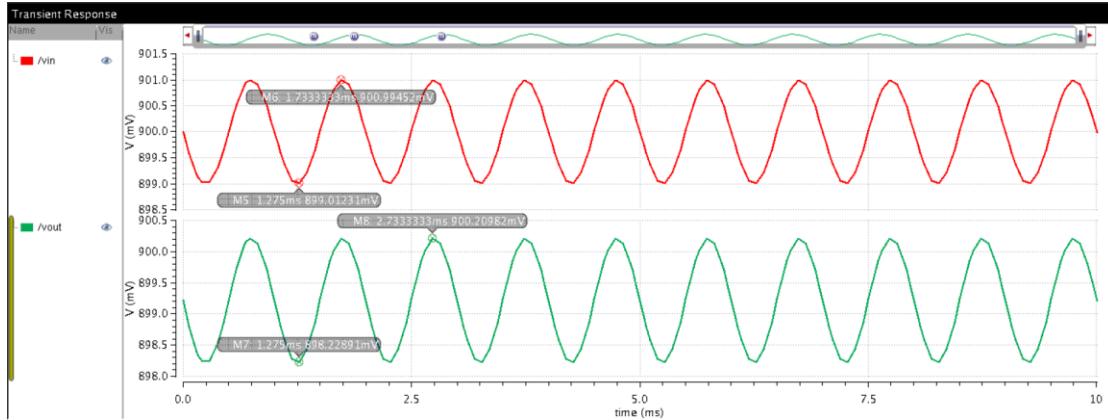


Fig 4.1.33 Resultant waveforms for the V_{in} and V_{out} of a 2-stage opamp with compensation and load.

Stability response (1 to 10GHz) - Magnitude and Phase plots: (LG = 54.94dB; PM = 59.51°; UGB at 7.83MHz):

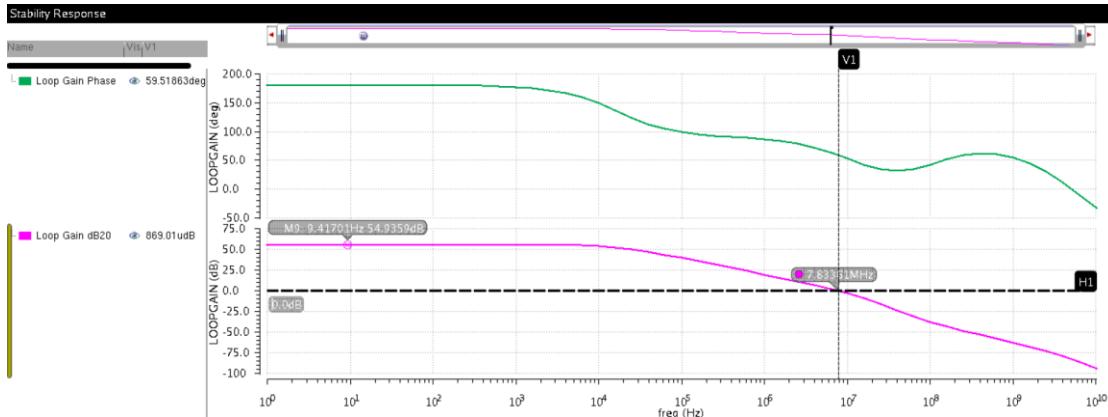


Fig 4.1.34 Resultant waveforms for the Stability Response of a 2-stage opamp with compensation and load.

III] 2-Stage Opamp DC Operating point simulation (Results Annotated)

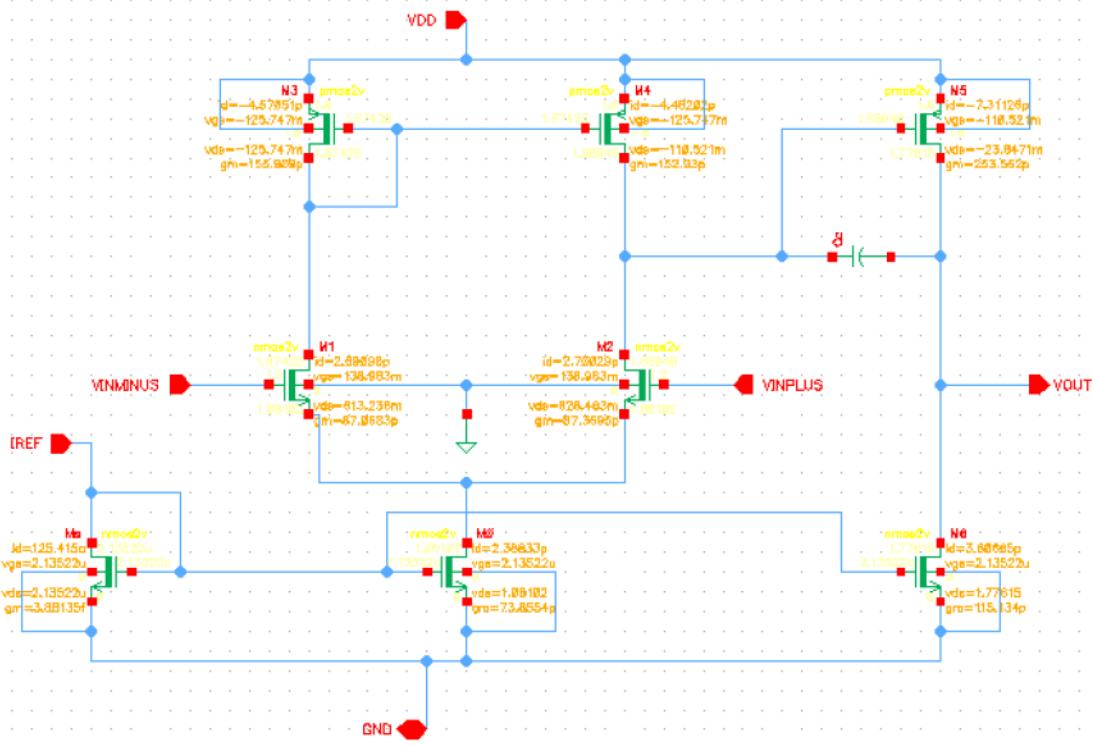


Fig 4.1.35 Resultant DC operating points of a 2-stage opamp with compensation.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

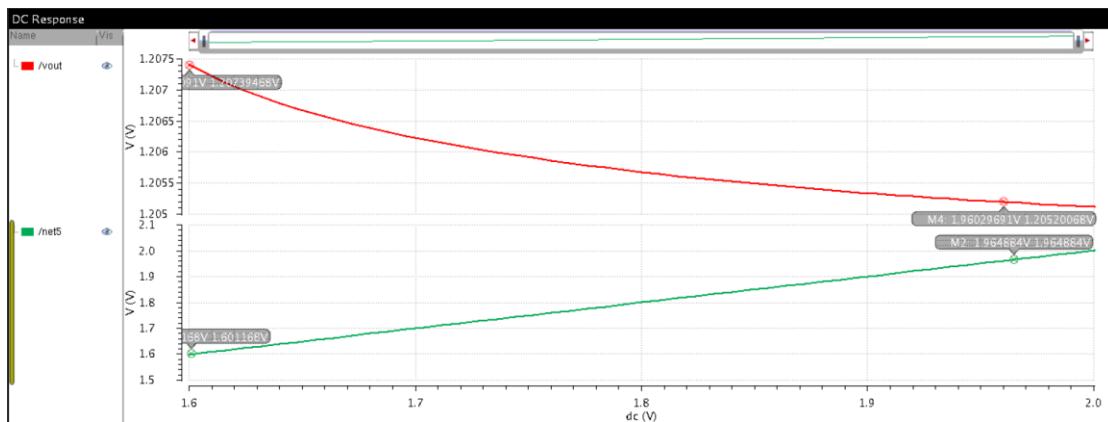


Fig 4.1.36 Resultant waveforms for the VDD v/s Vout sweep of a 2-stage opamp with compensation and load.

Transient simulation [0-10ms] ($V_{inDC} = 1.2V$, $V_{inAC} = 1KHz$ Sine wave w/2mVpp amplitude): [Gain = 1.004]

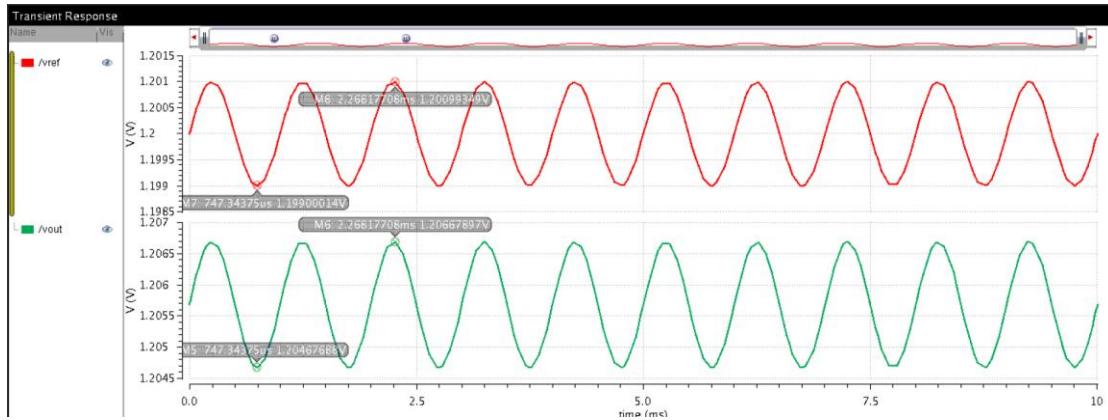


Fig 4.1.37 Resultant waveforms for the V_{in} and V_{out} of a 2-stage opamp with compensation and load.

Stability response (1 to 100GHz) - Magnitude and Phase plots: (LG = 57.57dB; PM = 60.79°; UGB at 4.594 MHz):

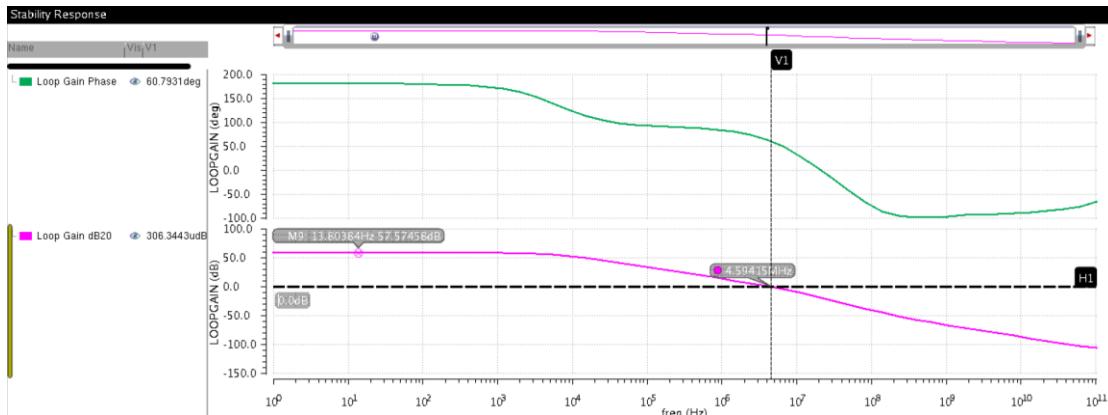


Fig 4.1.38 Resultant waveforms for the Stability Response of a 2-stage opamp with compensation and load.

I] LDO Regulator with a 2-stage opamp ($V_{out} = 1.5V$; $V_{ref} = 1.2V$, $V_{inAC} = 1KHz$ Sine wave w/2mVpp amplitude; $VDD = 1.8V$; $CL = 0.8\mu F$ to $1.2\mu F$; $IL = 10\mu A$ to $1mA$):

LDO DC simulation (Annotated results):

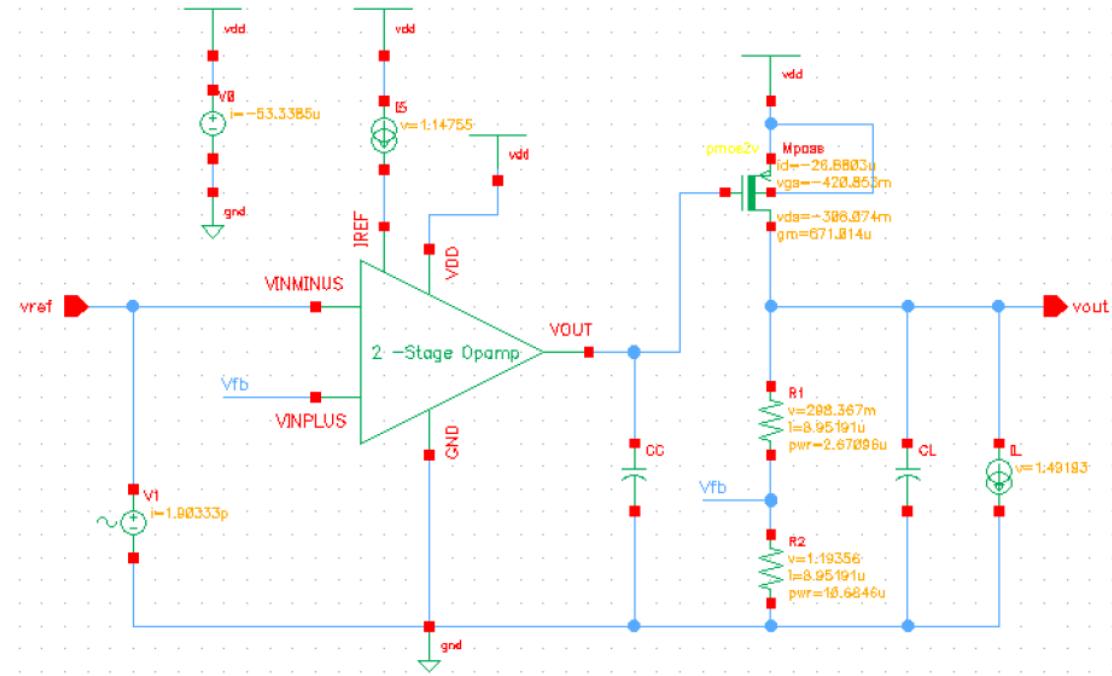


Fig 4.1.39 Resultant DC operating points of an LDO Regulator.

LDO Transient simulation [0-10ms] ($V_{inDC} = 1.2V$, $V_{inAC} = 1KHz$ Sine wave w/2mVpp amplitude): [Gain = 1.245]

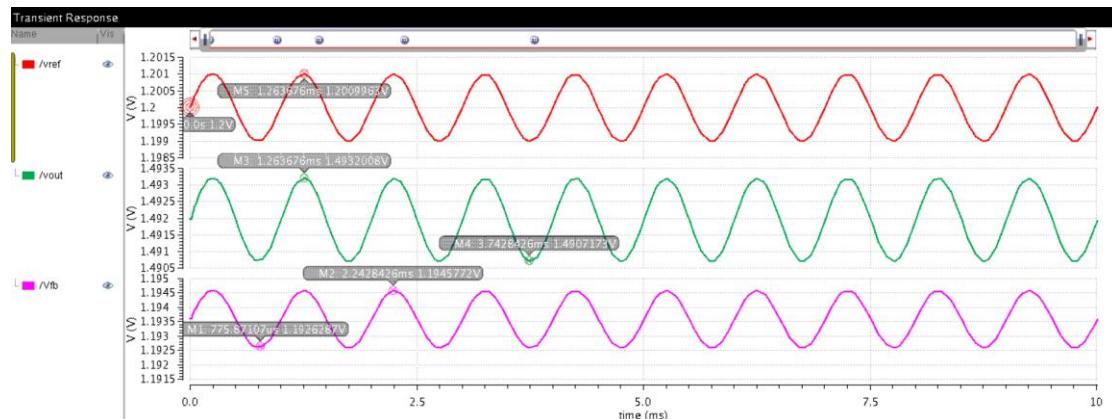


Fig 4.1.40 shows the resultant waveforms for the V_{fb} , V_{ref} and V_{out} of a $1.5V$ LDO Regulator.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

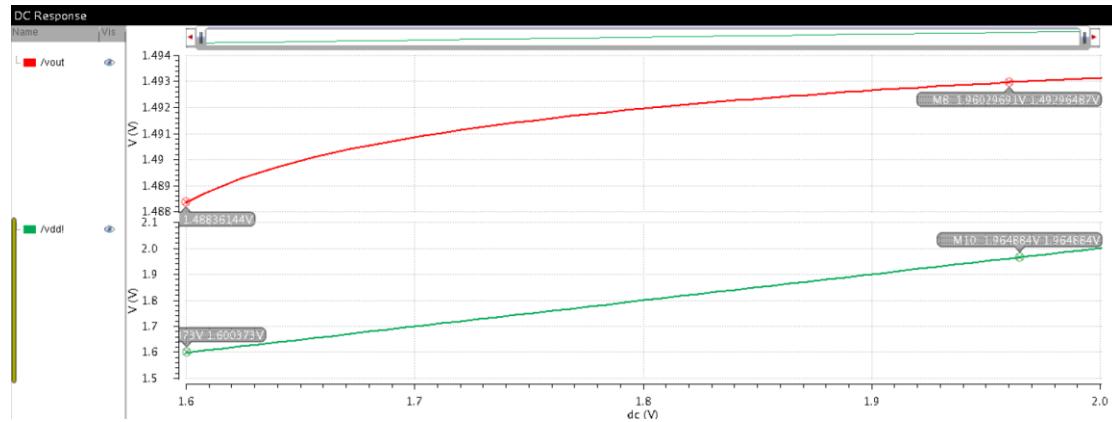


Fig 4.1.41 Resultant waveforms for the VDD v/s Vout sweep of an LDO.

Stability response Magnitude and Phase plots at CL = 1uF and IL = 10uA, (LG = 80.85dB; PM = 29.07°; UGB at 16.04KHz):

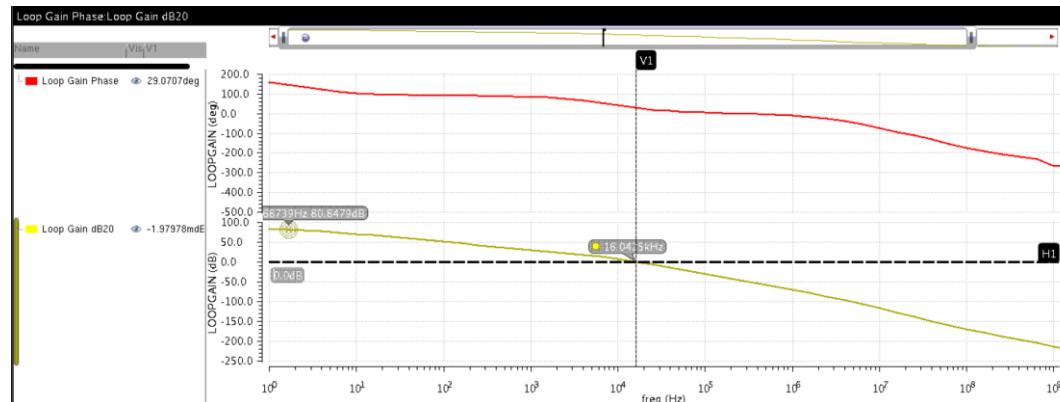


Fig 4.1.42 Resultant waveforms for the Stability Response of an LDO at minimum load.

Stability response Magnitude and Phase plots at CL = 0.8uF and IL = 1.1mA, (LG = 80.85dB; PM = 4.87°; UGB at 77.94KHz):

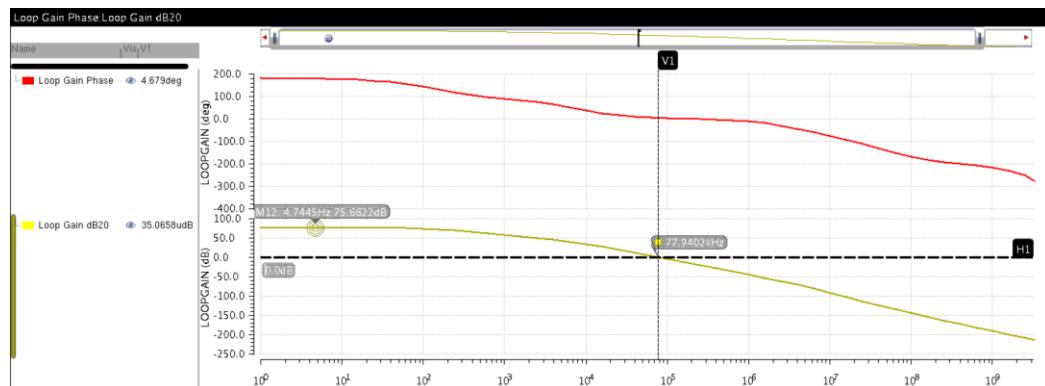


Fig 4.1.43 Resultant waveforms for the Stability Response of an LDO at maximum load.

Stability response Magnitude and Phase plots at CL = 1.2uF and IL = 10uA, (LG = 81.66dB; PM = 31.96°; UGB at 14.59KHz):

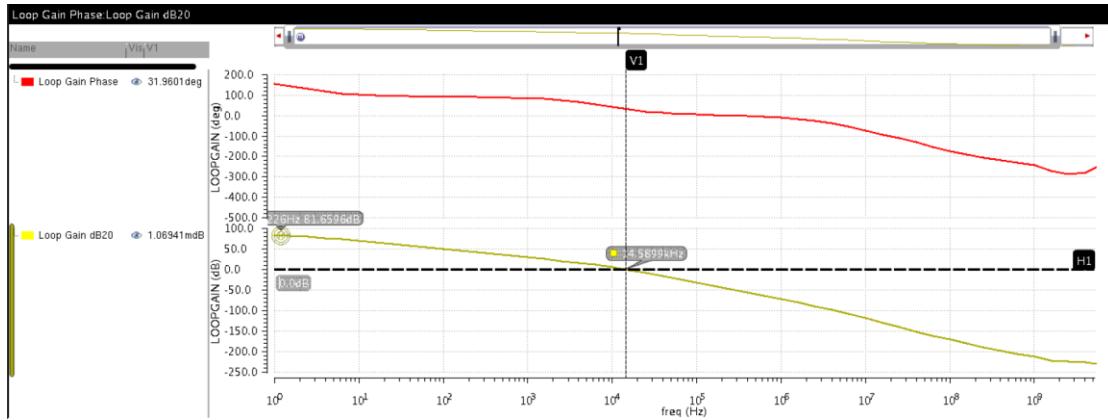


Fig 4.1.44 Resultant waveforms for the Stability Response of an LDO at Ideal load.

**II] LDO Regulator with a 5T-OTA (Vout = 1.5V; Vref = 1.2V, VinAC = 1KHz Sine wave w/2mVpp amplitude; VDD = 1.8V; CL = 0.8uF to 1.2uF; IL = 10uA to 1mA):
LDO DC simulation (Annotated results):**

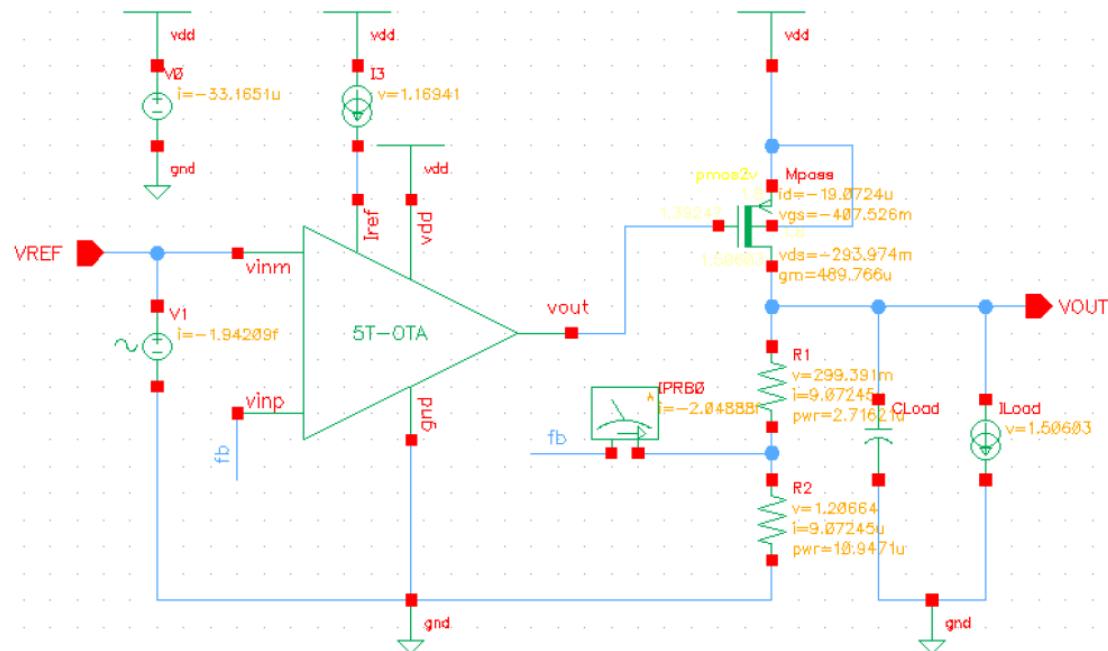


Fig 4.1.45 Resultant DC operating points of an LDO Regulator.

LDO Transient simulation [0-10ms] (VinDC = 1.2V, VinAC = 1KHz Sine wave w/2mVpp amplitude):

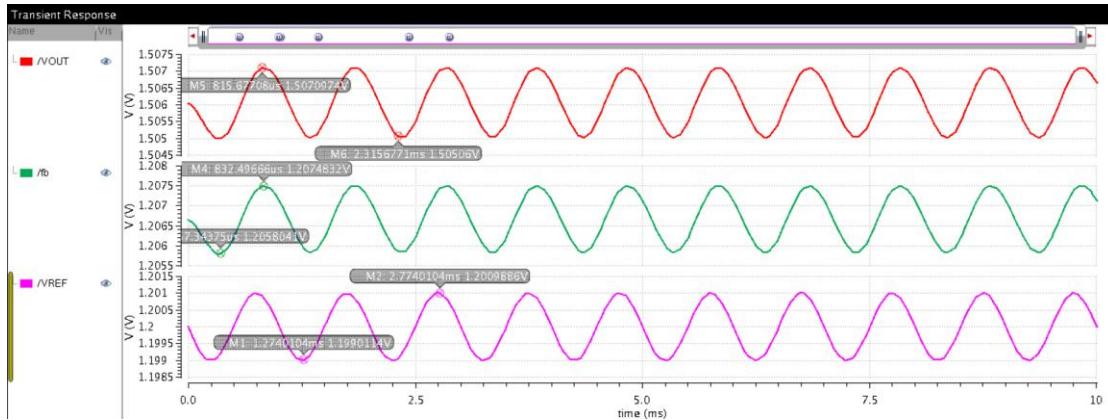


Fig 4.1.46 Resultant waveforms for the Vfb, Vref and Vout of a 1.5V LDO Regulator.

DC Simulation with a VDD sweep from 1.6V to 2V (VDD v/s VOUT):

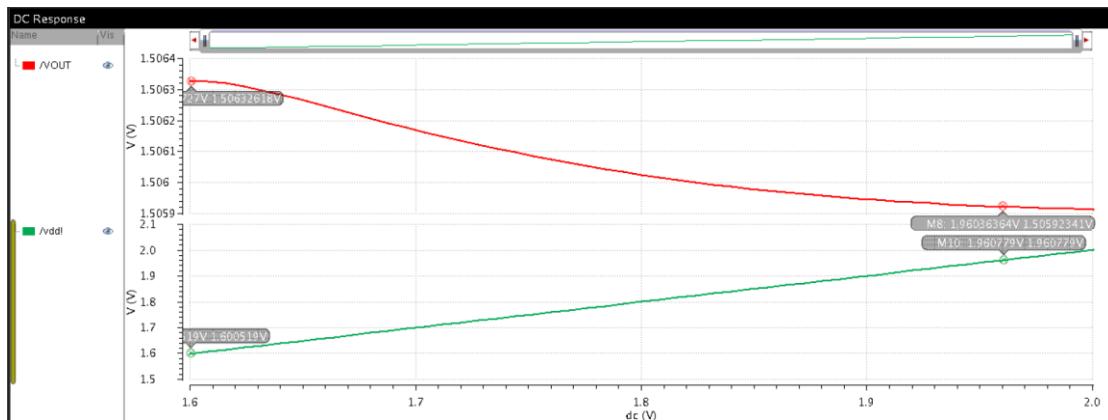


Fig 4.1.47 Resultant waveforms for the VDD v/s Vout sweep of an LDO.

DC Simulation with a temperature sweep from -50C to 125C (Temp v/s VOUT):

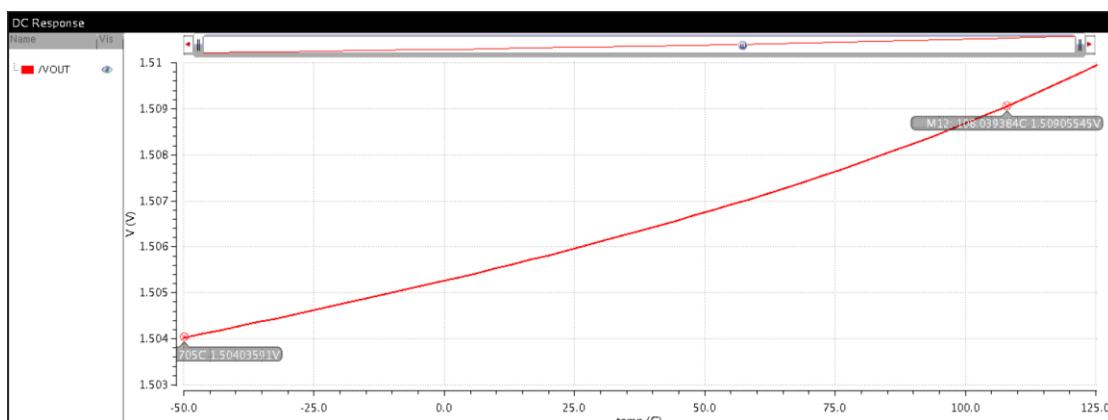


Fig 4.1.48 Resultant waveforms for the Temperature v/s Vout sweep of an LDO.

DC Simulation with a temperature sweep from -50C to 125C (Temp v/s VOUT):

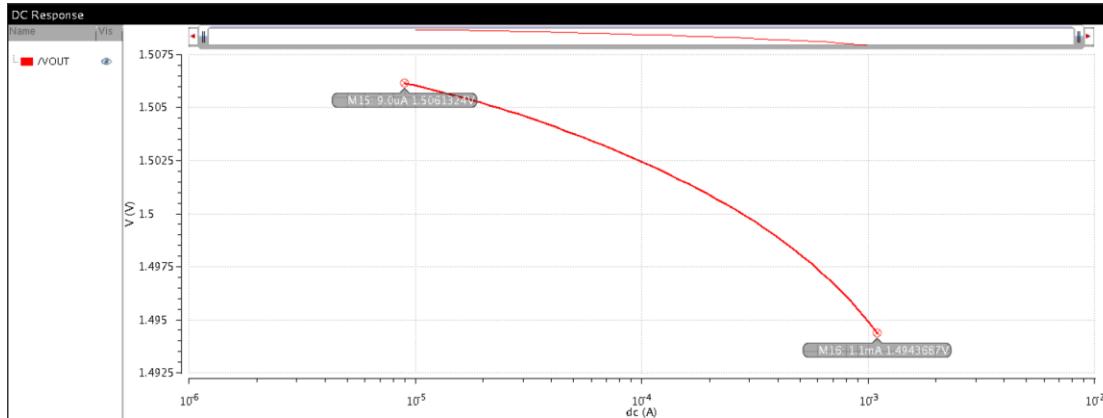


Fig 4.1.49 Resultant waveforms for the Iload v/s Vout sweep of an LDO.

Stability response Magnitude and Phase plots at CL = 1uF and IL = 10uA, (LG = 55.20dB; PM = 88.94°; UGB at 1.542KHz):

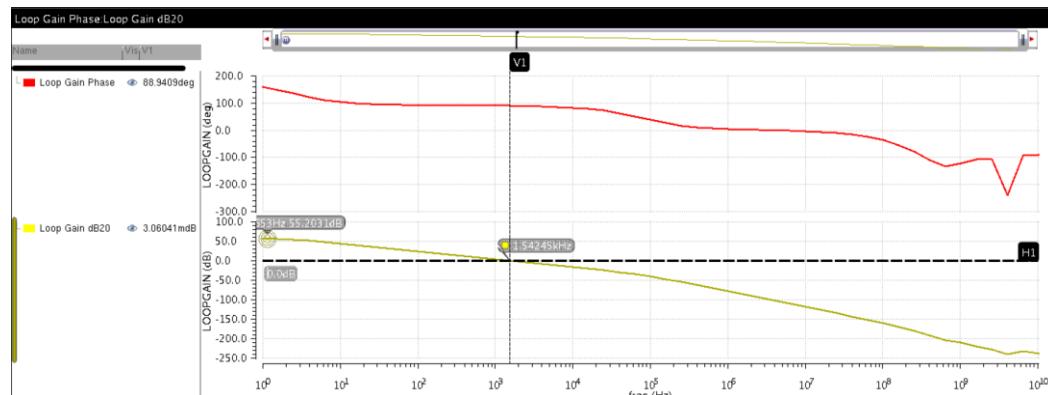


Fig 4.1.50 Resultant waveforms for the Stability Response of an LDO at minimum load.

Stability response Magnitude and Phase plots at CL = 1uF and IL = 1mA, (LG = 49.79dB; PM = 61.32°; UGB at 24.65KHz):

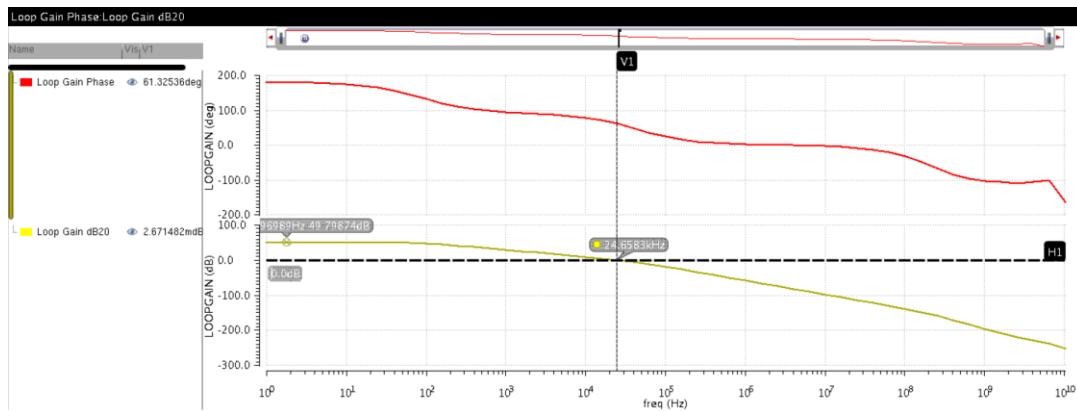


Fig 4.1.51 Resultant waveforms for the Stability Response of an LDO at Ideal load.

III] LDO Regulator with a 5T-OTA (Vout = 1.8V; Vref = 1.2V, VinAC = 1KHz Sine wave w/2mVpp amplitude; VDD = 2V; CL = 25pF; IL = 10uA to 15mA):

LDO DC simulation (Annotated results):

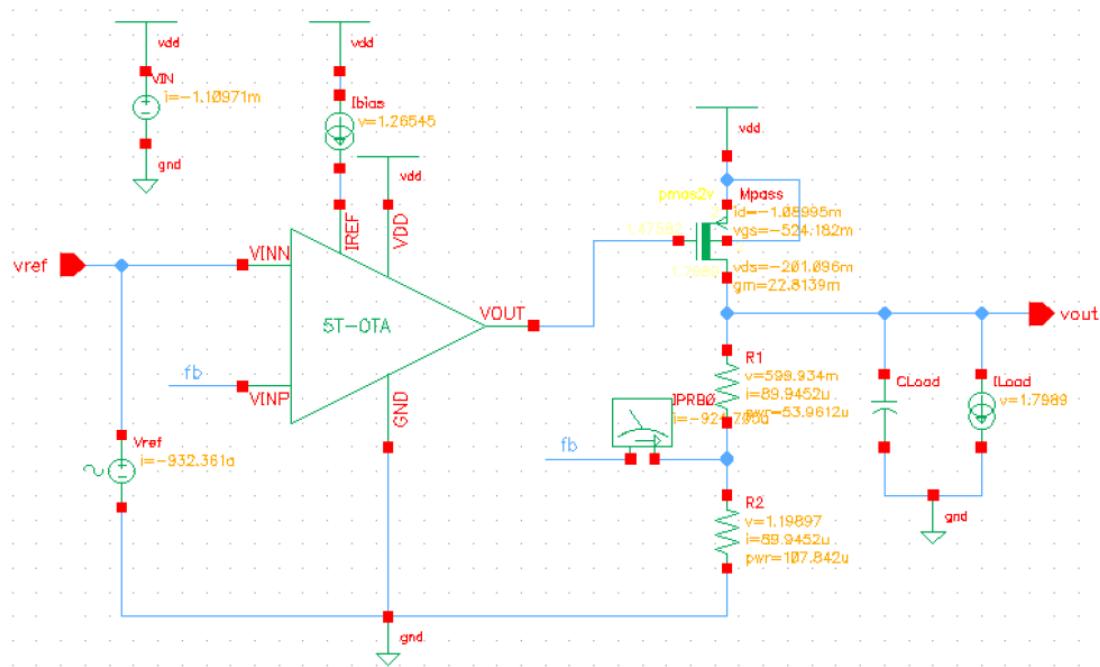


Fig 4.1.52 Resultant DC operating points of an LDO Regulator.

LDO Transient simulation [0-10ms] (VinDC = 1.2V, VinAC = 1KHz Sine wave w/2mVpp amplitude): [Gain = 1.5]

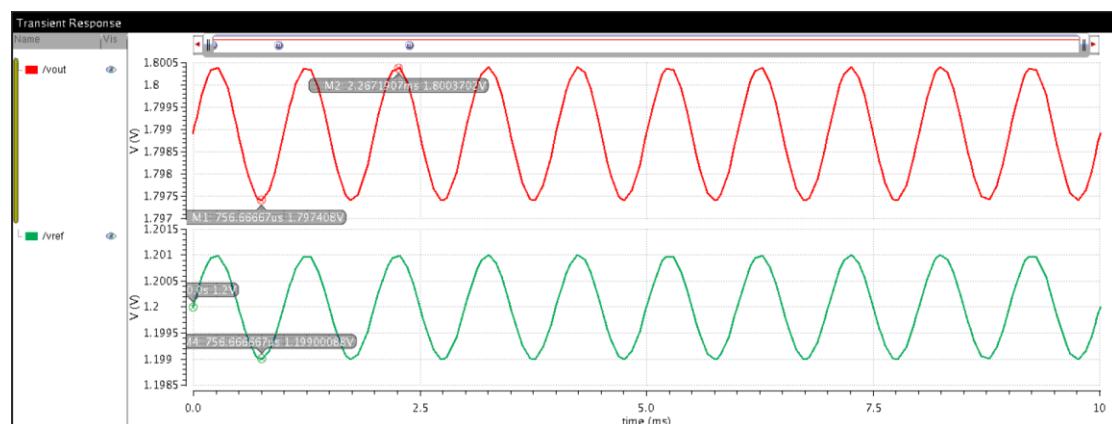


Fig 4.1.53 Resultant waveforms for the Vref and Vout of a 1.8V LDO Regulator.

DC Simulation with a VDD sweep from 1.8V to 2.2V (VDD v/s VOUT):

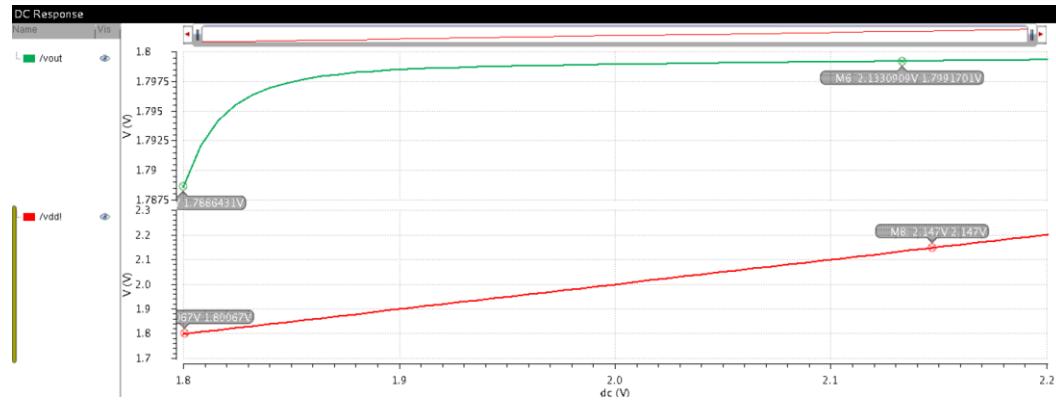


Fig 4.1.54 Resultant waveforms for the VDD v/s Vout sweep of an LDO.

DC Simulation with a temperature sweep from -50C to 125C (Temp v/s VOUT):

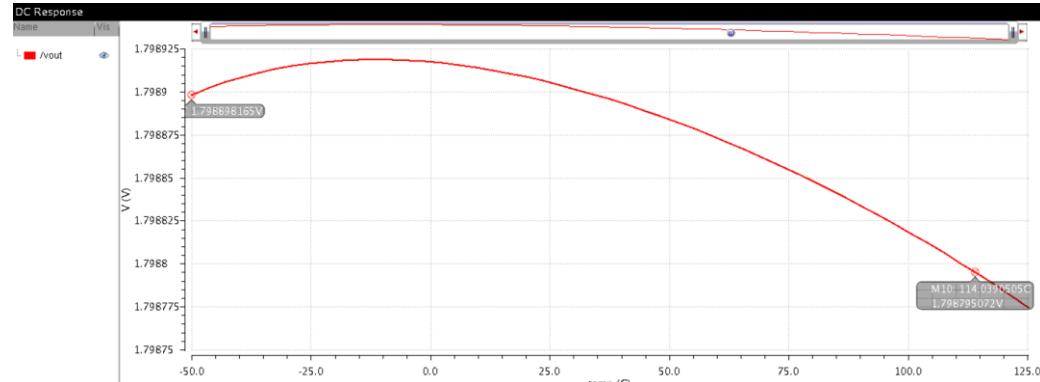


Fig 4.1.55 Resultant waveforms for the Temperature v/s Vout sweep of an LDO.

Stability response Magnitude and Phase plots at CL = 25pF and IL = 1mA, (LG = 52.36dB; PM = 46.84°; UGB at 15.14MHz):

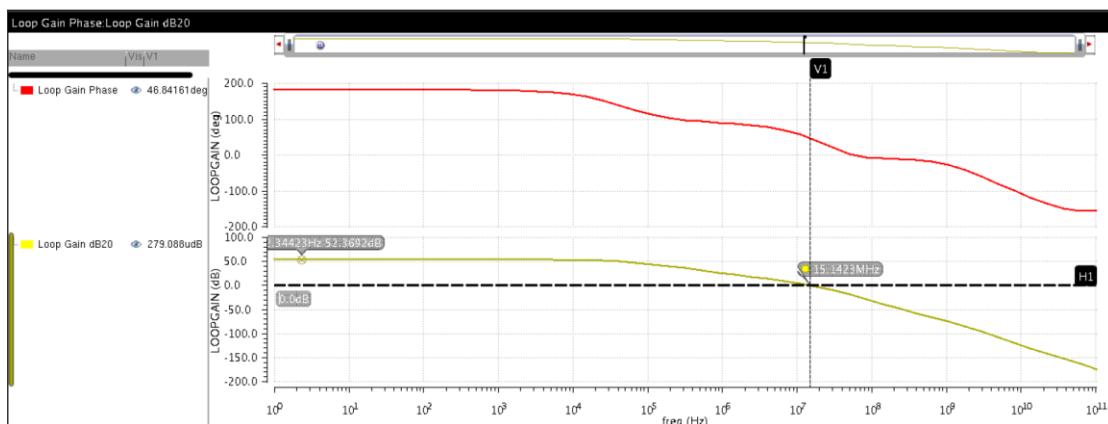


Fig 4.1.56 Resultant waveforms for the Stability Response of an LDO at Ideal load.

Stability response Magnitude and Phase plots at CL = 25pF and IL = 10uA, (LG = 50.78dB; PM = 20.87°; UGB at 8.29MHz):

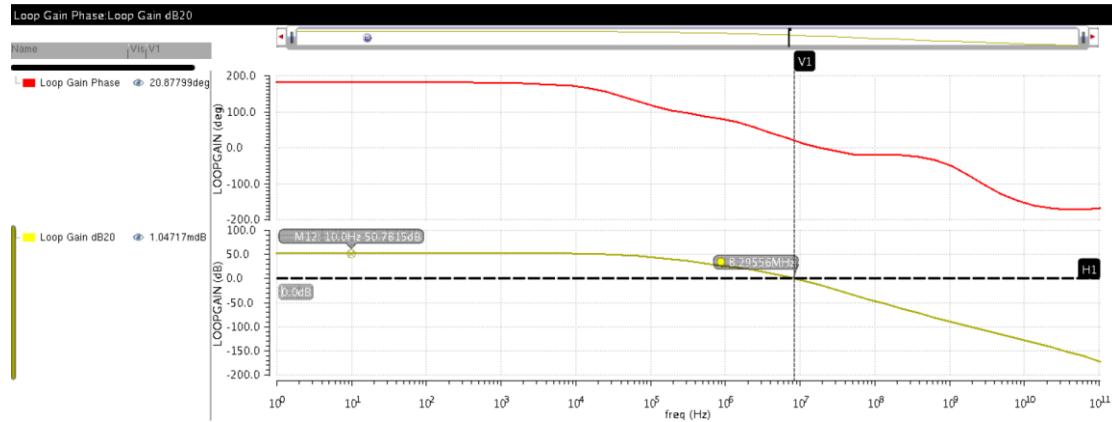


Fig 4.1.57 Resultant waveforms for the Stability Response of an LDO at minimum load.

Stability response Magnitude and Phase plots at CL = 25pF and IL = 15mA, (LG = 34dB; PM = 86.06°; UGB at 5.39MHz):

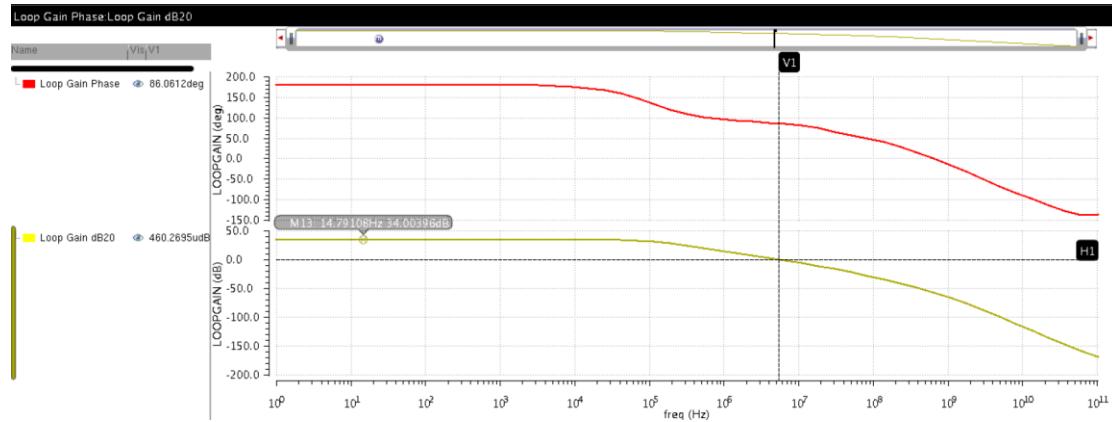


Fig 4.1.58 Resultant waveforms for the Stability Response of an LDO at maximum load.

I] Bandgap Reference (Banba 1999 Sub-1V design) with a 5T-OTA (Vout = 1.2V; Vin = 1.2V, VinAC = 1KHz Sine wave w/2mVpp amplitude; VDD = 2V:
LDO DC simulation (Annotated results):

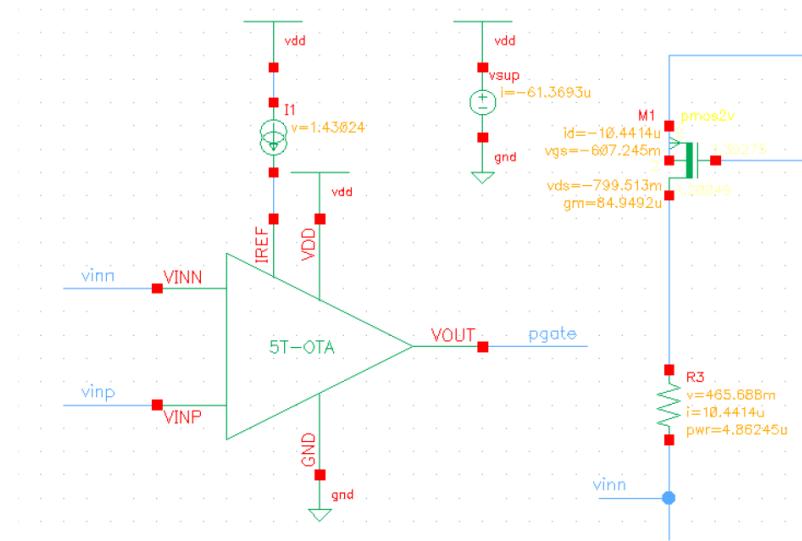


Fig 4.1.59 Resultant DC operating points of a Bandgap Reference 5T-OTA.

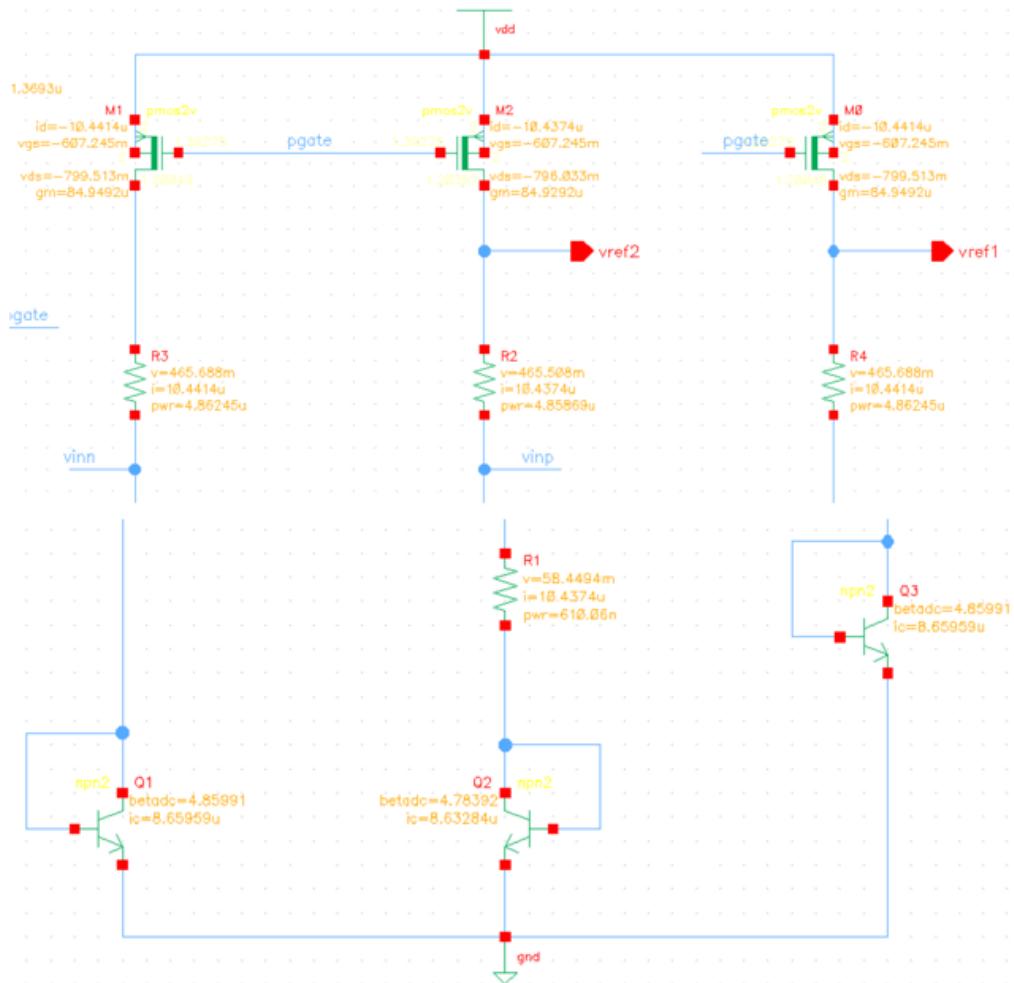


Fig 4.1.59 Resultant DC operating points of a Bandgap reference.

DC Simulation with a temperature sweep from -50C to 125C (CTAT v/s PTAT):

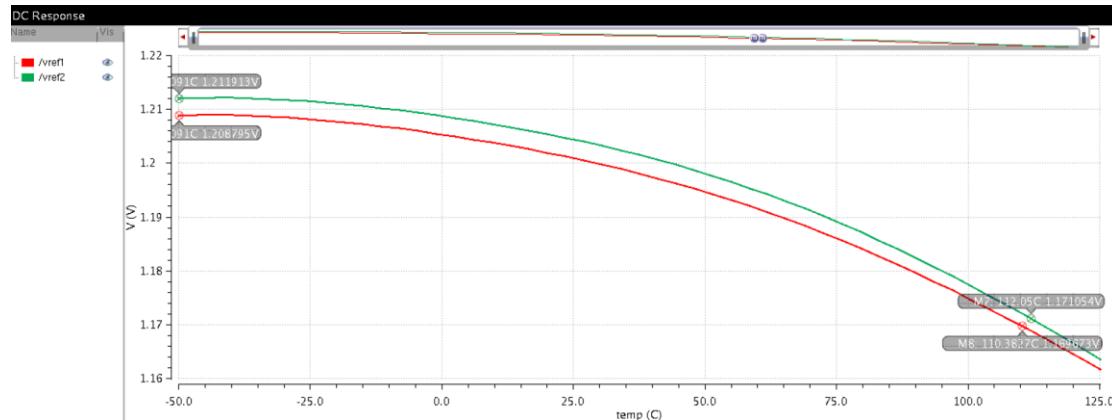


Fig 4.1.60 Resultant waveforms for the CTAT and PTAT curve of a 1.2V Bandgap Reference.

DC Simulation with a temperature sweep from 0C to 80C (Temp v/s VOUT):

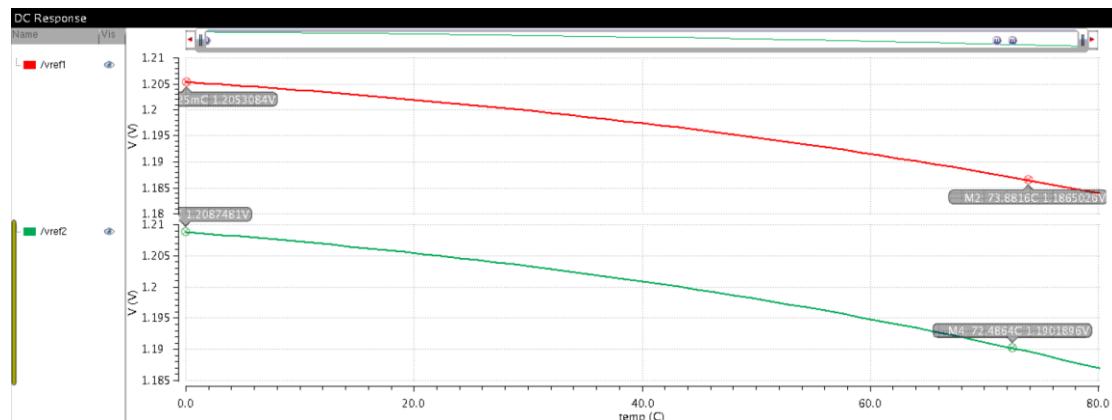


Fig 4.1.61 Resultant waveforms for the Ideal Temperature & Vout sweep of a BGR.

DC Simulation with a temperature sweep from -50C to 125C (Temp v/s VOUT):

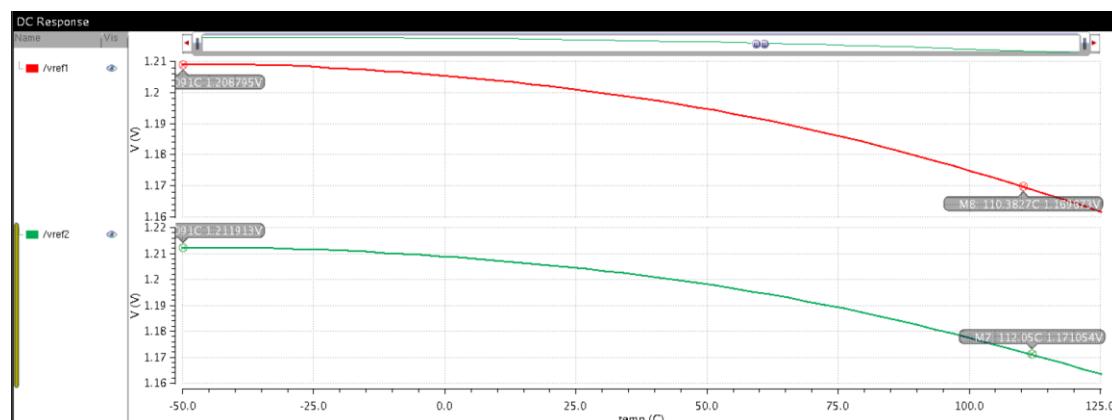


Fig 4.1.62 Resultant waveforms for the Full range Temp v/s Vout sweep of a BGR.

**II] Bandgap Reference (General design) ($V_{out} = 1.2V$; $V_{in} = 1.2V$, $V_{inAC} = 1KHz$
Sine wave w/2mVpp amplitude; VDD = 2V:
BGR DC simulation (Annotated results):**

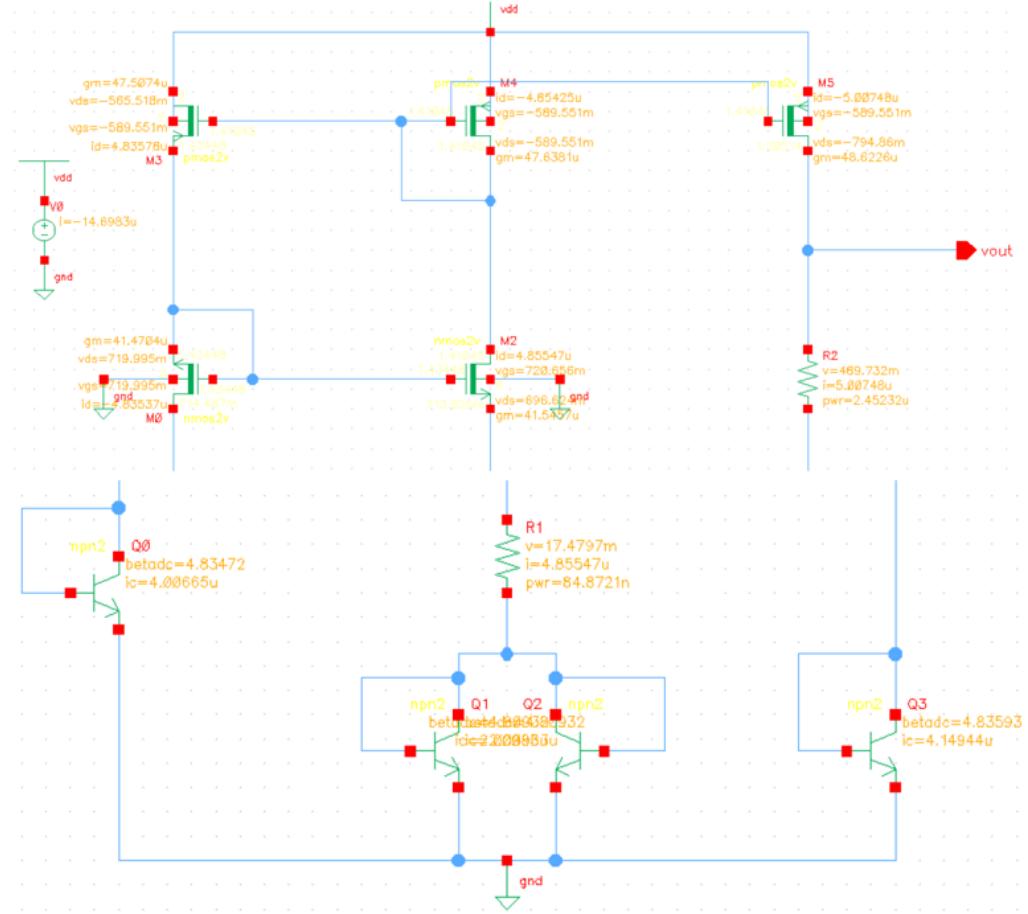


Fig 4.1.63 Resultant DC operating points of a General Bandgap reference.

DC Simulation with a temperature sweep from -50C to 125C (Temp v/s Vout):

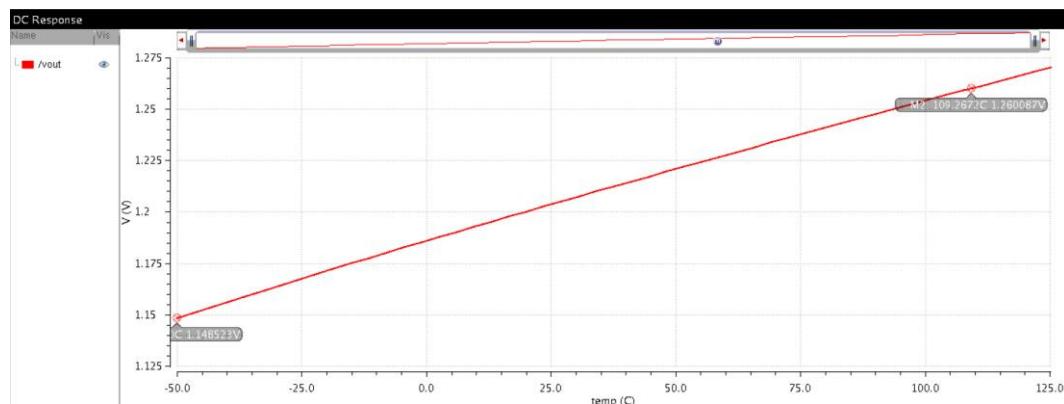


Fig 4.1.64 Resultant waveforms for the Full range Temperature v/s Vout sweep of a BGR.

DC Simulation with a temperature sweep from 0C to 80C (Temp v/s VOUT):

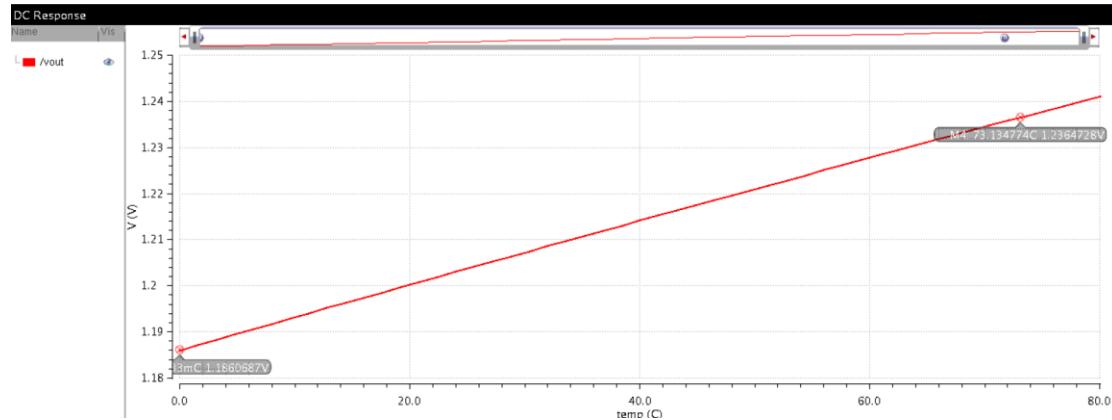


Fig 4.1.65 Resultant waveforms for the Ideal Temperature v/s Vout sweep of a BGR.

Discussion:

All the simulations were verified with the designed specifications to ensure that the design is correctly calculated and optimized as per the requirements.

The simulated results revealed that the designs were correctly calculated with all the parameters such as I_D , stability, noise, DC gain, and transient characteristics being within the permissible limits for the design rules.

This made the designs pass the design rule checks and enabled them to go to the layout stage wherein the physical layout can be created by the layout design engineer.

Chapter 5

Advantages, Limitations and Applications

5.1 Advantages

- High Gain: Differential amplifiers, operational amplifiers (Op-Amps), and cascode amplifiers offer high voltage gain.
- Versatility: Op-Amps are versatile, finding applications in filters, amplifiers, oscillators, and voltage regulators.
- Low Input/Output Resistance: Cascode amplifiers have low input and output resistance, minimizing loading effects.
- Stability: Op-Amps are designed for stability in various circuit designs.
- Simplicity: Single-stage amplifiers are straightforward in design.
- Common-Mode Rejection: Differential amplifiers excel at rejecting common-mode signals.
- Balanced Inputs: Differential amplifiers are ideal for balanced input applications.
- Limitations:

5.2 Limitations

- Limited Gain-Bandwidth Product: Single-stage amplifiers may have limited bandwidth for high-gain configurations.
- Linearity Challenges: Achieving high linearity can be challenging, particularly in single-stage amplifiers.
- Power Consumption: Op-Amps can consume significant power.
- Complexity: Cascode amplifiers can be more complex to design and analyze.

5.3 Applications:

- Audio Amplification: Single-stage amplifiers, Op-Amps, and cascode amplifiers are used in audio equipment and headphones.
- Instrumentation: Differential amplifiers are vital in instruments like oscilloscopes and data acquisition systems.
- Communication Systems: Differential amplifiers find use in balanced communication systems.
- Signal Processing: Op-Amps are used in filters, signal conditioners, and instrumentation amplifiers.
- Voltage Regulation: Op-Amps and LDO regulators are integral to voltage regulation circuits.
- Control Systems: Op-Amps are used in control systems and feedback loops.
- Mobile Devices: LDO regulators provide stable power in smartphones and tablets.
- RF Systems: LDO regulators are used in RF circuits for low-noise power supplies.
- Battery-Powered Devices: LDO regulators extend battery life in portable devices.
- Precision Voltage References: Bandgap references are used in ADCs, DACs, and precision analog circuits for accurate voltage references.

Chapter 6

Conclusion and Future Scope

Conclusion

In the pursuit of my project, "Analog System Design," I embarked on an immersive journey into the realm of analog hardware devices and networks. This endeavor provided me with a deep understanding of fundamental components, including R-L-C Circuits, P-N diodes, BJTs, MOSFETs, and more. I delved into the intricacies of semiconductor physics, industry-standard design techniques, and analytical methodologies that underpin analog VLSI design.

Throughout this project, I honed my skills, from navigating the Linux environment to utilizing the Cadence Virtuoso Design tool. I learned the intricacies of the Analog VLSI Design flow, becoming proficient in Linux file system commands. Additionally, I developed expertise in schematic design and simulation procedures within the Cadence Virtuoso design suite.

In the project, my focus was more towards designing and optimizing critical analog components, including single-stage amplifiers, differential amplifiers, 5T-OTAs, 9T-OTAs, and more. These components laid the groundwork for more intricate analog designs and applications.

Of paramount importance was the rigorous verification of our simulations against meticulously planned design specifications. This step was crucial to ensure the precision and optimization required by the project. The results of these simulations confirmed the accuracy of our calculations, with parameters such as I_D , stability, noise, DC gain, and transient characteristics all falling within the prescribed design rules.

This successful verification not only validated my designs but also paved the way for the next phase: the layout stage. Here, skilled layout design engineers will transform our virtual designs into tangible physical layouts, serving as blueprints for real-world circuit implementation.

Future work

This project has laid a solid foundation in analog system design, but the journey continues toward more intricate challenges. In the future, I aim to tackle complex analog blocks, including sub-1V voltage regulators, Low Noise Amplifiers, Sub-1V Bandgap references, oscillators, Phase Locked Loops and Data converters.

These advanced components play pivotal roles in modern electronics, requiring a deeper understanding of analog VLSI principles and nuanced optimization. Challenges will include noise reduction, temperature stability, and phase synchronization, among others.

I also plan to explore emerging technologies and innovative approaches to analog design, staying at the forefront of VLSI advancements. These future projects will expand my expertise and contribute to the ongoing evolution of high-performance electronic systems in our interconnected world.

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U. M. Iqbal, L. S. Mahmood, L. Nguyen and L. Albasha, "Folded Cascode Current Mirror Design using Cadence," 2019 International Conference on Communications, Signal Processing, and their Applications (ICCS SPA), Sharjah, United Arab Emirates, 2019, pp. 1-4, doi: 10.1109/ICCS SPA.2019.8713755.

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C. L. Kavyashree, M. Hemambika, K. Dharani, A. V. Naik and M. P. Sunil, "Design and implementation of two stage CMOS operational amplifier using 90nm technology," 2017 International Conference on Inventive Systems and Control (ICISC), Coimbatore, India, 2017, pp. 1-4, doi: 10.1109/ICISC.2017.8068601.

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Citation:

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