IP5328P REG Documentation

1 I2C interface

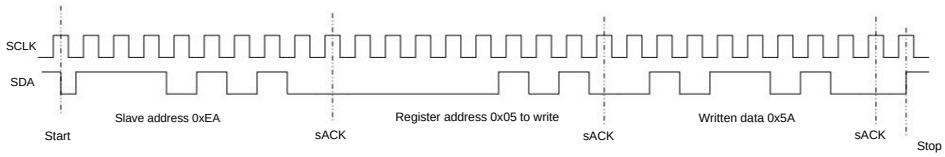
The chip can only support one I2C connection method at the same time. Connecting according to the corresponding method will turn off the Function function and automatically enter the I2C mode.

Mode. I2C speed supports 400Kbps. Supports 8-bit register address width and 8-bit data width. Send and receive MSB first, the default slave sends
The register address is 0xEA.

The I2C of IP5328P acts as a slave and is controlled by the host. The SCK signal of I2C is provided by the host, and the SDA line can be pulled up to VCC by a 3.3Kohm resistor, or Pulled low by master or slave. The typical timing for writing 8-bit data to a register is shown in the figure below. The host sends out the start signal in turn,
Slave address, register address and 8-bit data. For every 8 bits of data (register address or data) sent, IP5328P sends an ACK. all
A process stops sending by sending a stop signal from the host.

All 8-bit registers must be written before data is updated.

For example: write 8-bit data 0x5A to 0x05 register, the slave register address is 0xEA.



Note: The sACK signal is generated by the slave, the mACK is generated by the master, and the mNACK is the NACK generated by the master.

Figure1 I2C write

A typical I2C read timing is shown in the figure below. The master sends the start signal, the slave address, the register address in sequence, then the restart bit and the slave

Address 0xEB generates a read operation. The host outputs an 8-bit clock and reads 8-bit data.

For example: read data 0x5A from 0x05 register, the slave register address is 0xEA.

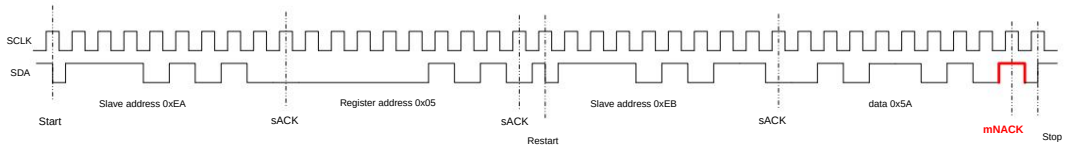
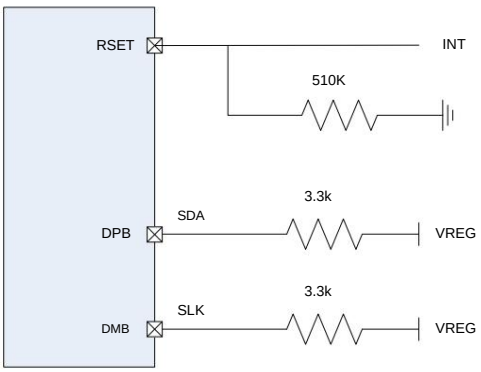


Figure 2 I2C Read

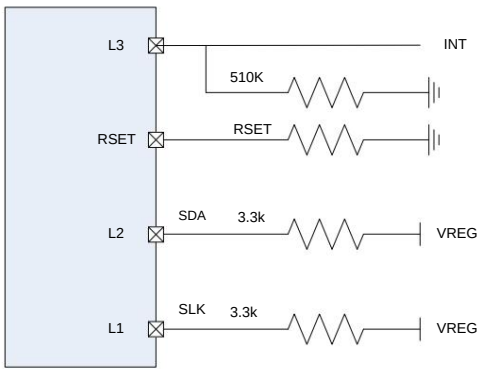
Special note: At the end of the I2C read data, when the last BYTE is read, be sure to give a NACK signal, otherwise IP5318 will think that the MCU needs to continue to read data, and the next

SCLK will output the next data, and the STOP signal cannot be received normally, which may cause the I2C bus to be pulled to death.

2. I2C application description



IIC Mode 2



IIC Mode 1

Note: The " ***IP5328P*** register has been updated here" is a reminder that the **IP5328P** register and the **IP5328** register are updated in different places.

1. The IP5328P standard product supports I2C by default, and there is no need to customize the **I2C** version separately;

2. When the IP5328P changes from the sleep state to the working state (buttons, load access, 5V charging access), the IP5328P will first detect L1,

Whether the L2 pin is pulled up to 3.1V (VREG), if L1 and L2 are pulled up to 3.1V at the same time, enter the I2C mode, and L3 outputs a 3.1V high

level; if it is not detected that L1 and L2 are pulled up at the same time, it will enter the LED light display mode, and it will be detected every time it enters the working state from sleep;

3. Since the IP5328P will perform I2C detection when it enters the working state from sleep, the MCU needs to match SDA and SCK when it is sleeping.

Set to input or high-impedance state, and start reading and writing I2C data until INT is detected to be high, otherwise it will cause the IC to enter work from sleep.

In the state, it is detected that L1 or L2 is not pulled up and cannot enter the I2C state

4. Since the IP5328P will perform I2C detection when it enters the working state from sleep and the digital level inside the IP5328P is 3.1V, the MCU supplies

The power must be powered by VREG. If the MCU is powered by an external LDO, when the BAT is out of power or less than 2V, VIN is connected to 5V to supply the IP5328P

When the VREG is powered, the system will perform I2C detection, but the MCU has no power, and the state of SDA and SCK is uncertain, which may cause L1 and L2 not to be detected.

Pull-up cannot enter I2C mode;

5. If you want to modify a certain register of IP5328P, you need to first read the value of the corresponding register and perform AND-OR operation on the BIT bits that need to be modified.

After the calculation, write the calculated value into this register to ensure that only the values of the **bits** that need to be modified and other **bits cannot be changed arbitrarily. The default value of the register**

Based on the value read, **IC** default values may vary from batch to batch.

6. When IP5328P uses **I2C , MCU** can realize IP5328P **IC** work without writing **0** to **bit7** of **0x03** and **0** to **bit6** of **0x84**

When **INT** is high when sleeping, **INT** is blocked. If you write **0** to **bit7** of **0x03** and 0 to **bit6** of **0x84** in a similar way to **IP5328 ,** it will not affect

The state of the INT is **affected ,** and it has no effect on the actual application development.

IP5328P registers are updated here

3 Register Description

*Reserved registers cannot be written to data at will, and the original value cannot be changed, otherwise unexpected results will occur. to the register

The operation must be carried out according to read-modify-write, only the used bits are modified, and the values of other unused bits cannot be modified.

*The default value of the register in this document only represents a certain specification. The default value of the register of most specifications does not correspond to this document, so in the

Special attention should be paid to bitwise operations during read and write operations.

2.1 SYS_CTL1

register address = 0x01

Bit(s)	Name	Description	R/W
7:3		Reserved	
2		Boost boost enable 1ÿenable 0ÿdisable	R/W
1		Charger charging enable 1ÿenable 0ÿdisable	R/W
0		Reserved	

2.2 SYS_CTL3

register address = 0x03

Bit(s)	Name	DescriptionPower	R/W
7		-on reset register enable 1ÿenable 0ÿdisable	R/W
6:4		Reserved	
3		Long press time setting 0ÿ2s 1 ÿ 3s	R/W
2		Long press for 10S to reset enable 1ÿenable 0ÿdisable	R/W
1:0		Button shutdown mode selection 00/10: disable 01: short press twice 11: long press	R/W

2.3 SYS_CTL4

register address = 0x04

Bit(s)	Name 7	DescriptionChip	R/W
	EN_BSTTMDN	high temperature off BOOST enable 1ÿenable 0ÿdisable	R/W
6	EN_CHGTMDN	Chip high temperature off CHARGE enable 1ÿenable 0ÿdisable	R/W
5	EN_NTCL_BST	NTC low temperature off BOOST enable 1ÿenable 0ÿdisable	R/W
4	EN_NTC_MID	NTC medium temperature charge current halved enable 1ÿenable	R/W

		0ÿdisable	
3	EN_NTC_CHG	NTC high and low temperature off Charger enable 1ÿenable 0ÿdisable	R/W
2	EN_NTCH_BST	NTC high temperature shutdown BOOST enable 1ÿenable 0ÿdisable	R/W
1	EN_NTC_SC	When NTC is grounded (NTC<0.2V), disable NTC function enable 1ÿenable 0ÿdisable	R/W
0	EN_NTC	NTC protection enable 1ÿenable 0ÿdisable	R/W

2.4 IC_TEMP

register address = 0x42

Bit(s)	Name	Description	R/W
7:3		Reserved	
2	ENTSBST	The chip temperature protection points are all increased by 15C 1ÿenable 0ÿdisable	R/W
1	HT	Chip temperature high temperature alarm and recovery temperature 1 :140CÿC 0 :130C, 80C	R/W
0	TSEN	Chip temperature detection enable 1ÿenable 0ÿdisable	R/W

2.5 SYS_CTL5

register address = 0x05

Bit(s)	Name	Description	R/W
7:4		Reserved	
3	En_wled_on_r	WLED flashlight button switch control mode 0: long press 1: short press twice	R/W
2:1		Reserved	
0	En_wled_r	WLED flashlight (multiplexed with KEY) 1ÿenable 0ÿdisable	R/W

2.6 SYS_CTL7

register address = 0x07

Bit(s)	Name	DescriptionLight	R/W
7:6	Set_ilow_bst	load off Boost time: 00: 8s 01:16s 10: 32s 11:63s	R/W

5:4			
3	En_CHG_flash_r	IC charging high temperature flashing enable (flash cycle 1s) 1ÿenable 0ÿdisable	R/W
2		NTC charging high and low temperature flashing enable (flash cycle 1s) 1ÿenable 0ÿdisable	R/W
1		Charge input overvoltage flashing light enable (flashing period 1s) 1ÿenable 0ÿdisable	R/W
0		BAT charging overvoltage flashing light enable (flashing cycle 1s) 1ÿenable 0ÿdisable	R/W

2.7 BST_LED_FLASH1

register address = 0x9B

Bit(s)	Name 7	Description	R/W
	En_BST_flash_r	IC high temperature flashing enable (flash cycle 1s) 1ÿenable 0ÿdisable	R/W
6		NTC high and low temperature flashing enable (flash cycle 1s) 1ÿenable 0ÿdisable	R/W
5:0		Reserved	

2.8 SYS_CTL10

register address = 0x0A

Bit(s)	Name	Description	R/W
7	Set_dled_r	LED Mode Register Setting Enable 1ÿenable 0ÿdisable In I2C mode, the power calculation result can be viewed through the 0xDB register	R/W
6:5	Dled_mode_r	Register setting several light modes to calculate power 00:1 lights 01:2 Lights 10:3 lights 11:4 Lights	R/W
4:0		Reserved	

2.9 LED_STATUS

register address = 0xDB

Bit(s)	Name	Description	R/W
7:5		Reserved	
4:0	LED	battery level 11111: 4 lights on 01111: 3 lights on 00111: 2 lights on 00011: 1 light on 00001: Low-power flashing light when discharging 00000: shutdown	R

2.10 SYS_CTL11

register address = 0x0B

Bit(s)	Name	Description	R/W
7		Reserved	
6:5	Set_pod_time Set the interval time of output port closing when unplugging from charging to discharging state	01:2s 10: 3s 11: 4s	R/W
4:0		Reserved	

2.11 SYS_CTL13

register address = 0x0D

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:4		VIN and VBUS charging priority selection 00: According to the order of access, the first access person will be charged first 01: Look at the input voltage, high voltage priority 1X: When the voltage is the same, VBUS takes priority here ***IP5328P*** Register updated	
2		When the same charging and discharging is enabled, the charging current of the battery cell is automatically set to a maximum of about 500mA 1ÿenable 0ÿdisable	R/W
1	En_maxvinlp_r is enabled to automatically increase the 5V charging undervoltage loop to 4.92V when charging and discharging at the same time. Priority is given to charging the load	1ÿenable 0ÿdisable	R/W
0	in_same_r	Same charge and same discharge enable 1ÿenable 0ÿdisable	R/W

2.12 SYS_CTL14

register address = 0x0E

Bit(s)	Name	Description	R/W
7		Reserved	
6	En_chg2bst_r	Whether to automatically turn on Boost when the Charge is unplugged 1: On 0: not enabled	R/W
5ÿ4		Reserved	R/W
3	En_swclk2_r	Switch I2C mode 2 Standby clock enable (I2C of DCPB) 1ÿenable 0ÿdisable When enabled, I2C can be accessed at less than 10k in standby	R/W
2	En_swclk1_r	Switch I2C mode 1 Standby clock enable (I2C for L1/L2) 1ÿenable 0ÿdisable When enabled, I2C can be accessed at less than 10k in standby	R/W
1:0		Reserved	

2.13 VBAT_LOW

register address = 0x10

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:4	BATLOWSET	BAT actual voltage low power off voltage setting 11 3.00 ÿÿ3.10 10 2.90 ÿÿ3.00 01 2.81 ÿÿ2.89 00 2.73 ÿÿ2.81	R/W

3:0		Reserved	

2.14 WINE

register address = 0x11

Bit(s)	Name	Description	R/W
7:2		Reserved	
1:0	VINOVSET	VIN charge overvoltage setting 11: 16V 10:14V 01:6.0V 00: 5.6V	R/W

2.15 VBUSOV

register address = 0x12

Bit(s)	Name	Description	R/W
7:2		Reserved	
1:0	VBUSOVSET	VBUS charge overvoltage setting 11: 16V 10:14V 01:6.0V 00: 5.6V	R/W

2.16 BOOST_LINC

register address = 0x13

Bit(s)	Name	Description	R/W
7:2		Reserved	
1	Rlineext	Analog line compensation enable 1ÿenable 0ÿdisable	R/W
0	RLINC	Line Compensation Options: 1ÿ250mV@2A 0ÿ125mV@2A	R/W

2.17 TYPE-C_CTRL0

register address = 0x1B

Bit(s)	Name	Description	R/W
7:2		Reserved	
1:0	CC_mode	CC mode sel 00: UFP 01:DFP 10:DRP	RW

Here **the IP5328P** register has been updated, and IP5328 corresponds to **0X1A**

2.18 TYPE-C_CTRL1

register address = 0x1A

Bit(s)	Name	Description	R/W
7:4		Reserved	
3:2	SRC_Rp	SRC current setting for USB TypeC when not charging	RW

		00ÿdefault 01ÿ1.5A 10 ÿ 3A	
1:0			

here ***IP5328P*** Register updated **, IP5328** corresponds to **0X1B**

2.19 TYPE-C_CTRL4

register address = 0x1E

The value of the 0X1E register corresponding to IP5328P cannot be changed. The original IP5328 corresponds to "when charging and discharging, the SRC current configuration of USB typeC has been delete"

here ***IP5328P*** Register updated

2.20 CHG_CTL

register address = 0x1F

The value of the 0X1F register corresponding to the IP5328P cannot be changed.

The settings have been combined with the 4.2V cell constant voltage boost register (0X22 bit1:0).

here ***IP5328P*** Register updated

2.21 CHG_CTL2

register address = 0x22

Bit(s)	Name	Description	R/W
7:4		Reserved	
3:2	VCHG_SET	Constant voltage setting: 11:4.5 10:4.4 01:4.35 00:4.2	RW
1:0	R_CV	4.5V/4.4V/4.35V/4.2V battery constant voltage fast charge: 11: Constant voltage increases by 42mv 10: Constant voltage increases by 28mv 01: Constant voltage increases by 14mv 00: no increase	RW

2.22 CHG_CTL3

register address = 0x23

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:3	R_VIL7	Charge input undervoltage loop threshold @7V: 111:6.7 110:6.64 101:6.59 100:6.53 011:6.47 010:6.42 001:6.36 000:6.25	RW
2:0	R_VIL5	Charge input undervoltage loop threshold @5V:	RW

		111:4.92 110: 4.88 101:4.84 100: 4.8 011: 4.76 010: 4.72 001: 4.64 000: 4.58	

2.23 CHG_CTL4

register address = 0x24

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:3	R_VIL12	Charging input undervoltage loop threshold @12V: 111:11.8 110:11.7 101:11.6 100:11.5 011:11.4 010:11.3 001:11.2 000:11	RW
2:0	R_VIL9	Charge input undervoltage loop threshold @9V: 111:8.8 110:8.73 101:8.65 100:8.58 011:8.5 010:8.43 001:8.35 000:8.2	RW

2.24 CHG_ISET_9V

register address = 0x26

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:0	Chg_iset_H9V	Charge ISET @ 9V while charging Input charging current: Ichg=ISET*0.05A (The actual charging current will be 0~300mA smaller than the theoretical value)	RW

2.25 CHG_ISET_12V

register address = 0x27

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:0	Chg_iset_H12V	Charge ISET @ 12V while charging Input charging current: Ichg=ISET*0.05A (The actual charging current will be 0~300mA smaller than the theoretical value) IP5328P temporarily does not support 12V charging	RW

here ***IP5328P*** Register updated

2.26 CHG_ISET_5V_VBUS

register address = 0x29

Bit(s)	Name	Description	R/W
7:6		Reserved	
5:0	Chg_iset_vbus	Charge ISET @ VBUS 5V while charging Input charging current: Ichg=ISET*0.05A	RW

		(The actual charging current will be 0~300mA smaller than the theoretical value)	

2.27 **CHG_ISET_5V_VIN**

register address = 0x2A

Bit(s)	Name	Description	R/W
7:6			
5:0	Chg_iset_vin	Charge ISET @ VIN 5V while charging Input charging current: Ichg=ISET*0.05A (The actual charging current will be 0~300mA smaller than the theoretical value)	RW

2.28 **CHG_ISET_7V**

register address = 0x2B

Bit(s)	Name	DescriptionCharge	R/W
7:6	Set_iset_tk	ISET battery terminal charging current during trickle: Ichg=ISET*0.05A+0.10A	RW
5:0	Chg_iset_H5V	Charge ISET @ 7V while charging Input charging current: Ichg=ISET*0.05A (The actual charging current will be 0~300mA smaller than the theoretical value)	RW

2.29 CHG_TIMER_EN

register address = 0x2C

Bit(s)	Name	Description	R/W
7	En_tktime_r Trickle timer enable	0ÿdisable 1ÿenable	RW
6	En_cvtime_r	Charge CV timing enable 0ÿdisable 1ÿenable	RW
5	En_chgtime_r	Charge total timing enable (CC+CV) 0ÿdisable 1ÿenable	RW
4	En_vset_r	VSET setting mode 0: Set by register (0x22h[3:2]) 1: Set by pin	RW
3:1		Reserved	
0	en_tk_r	Trickle enable 0ÿdisable 1ÿenable	RW

2.30 CHG_TIMER_SET

register address = 0x2D

Bit(s)	Name	Description	R/W
7:6	Set_tk_time Trickle timeout setting	00ÿ2h 01ÿ3h 10 ÿ 4h 11ÿ6h	RW
5:4	Set_pcc_time Constant voltage interruption time N setting (when it is almost fully charged, the charging current is reduced to 0 every N minutes, see the battery cell whether the voltage is full)	00ÿ2min 01ÿ4min 10ÿ8min	RW

		11 ÿ 16min	
3:2	Set_cv_time	Charge CV Timeout Settings 00ÿ2h 01 ÿ 4h 10ÿ6h 11ÿ8h	RW
1:0	Set_chg_time	Charge CC+CV timeout setting 00ÿ8h 01ÿ12h 10ÿ16 o'clock 11 ÿ 24h	RW

2.31 DCDC_FREQ

register address = 0x31

Bit(s)	Name	Description	R/W
7:5	BSTFRQ	BST frequency setting 125k+125k*code	RW
4:2	CHGFRQ	CHG frequency setting 125k+125k*code	RW
1:0		Reserved	

2.32 QC_EN

register address = 0x3E

Bit(s)	Name	Description	R/W
7ÿ4		Reserved	
3	EN_QC_VBUS	VBUS channel fast charge enable 0ÿdisable 1ÿenable	RW
2	EN_QC_VIN	VIN channel fast charge enable 0ÿdisable 1ÿenable	RW
1	EN_QC_VOUT2	VOUT2 channel fast charge enable 0ÿdisable 1ÿenable	RW
0	EN_QC_VOUT1	VOUT1 channel fast charge enable 0ÿdisable 1ÿenable	RW

here ***IP5328P*** The registers are updated, This register is newly added for IP5328P

2.33 PMOS_REG_CTL0

register address = 0x59

Bit(s)	Name	Description	R/W
7:6		The Reserved	
5	En_vout2_r	register controls the vout2 channel 0: off 1: On	R/W
4	Vout2_ctrl	Register controls the vout2 path 0: State machine automatic control 1: Register control	R/W
3	En_vout1_r	Register controls the vout1 path 0: State machine automatic control 1: Register control	R/W
2	Vout1_ctrl	Register controls the vout1 path 0: off 1: On	R/W
1	En_vin_r	Register Controls VIN Path	R/W

		0: off 1: On	
0	Vin_ctrl	Register Controls VIN Path 0: State machine automatic control 1: Register control	R/W

2.34 PMOS_REG_CTL1

register address = 0x5A

Bit(s)	Name	Description	R/W
7:6		Reserved	
5	Set_vinlp_mode register setting or state setting charging undervoltage LOOP	1: Register (0x5Ah[4:3]) 0: Status setting	RW
4:3	Svinloop_r	Register set charge undervoltage LOOP 00ÿ5V 01 ÿ 7V 10 ÿ 9V 11ÿ12V	RW
2	En_vbusi_r	Register controls VBUS input path 0: off 1: On	R/W
1	En_vbuso_r	Register controls VBUS output path 0: off 1: On	R/W
0	Vbus_ctrl	Register Control VBUS Path Control 0: State machine automatic control 1: Register control (0x5A[2:1])	R/W

2.35 FORCE_EN

register address = 0x5B

Bit(s)	Name	Description	R/W
7	Force_WLED		R/W
6	En_force_WLED first write 1 to bit6, and then write 1 to bit7 to trigger WLED internally;	After turning on, write 0 to bit7 first, and then write 0 to bit6 to turn off the WLED	R/W
5	Force_reset		R/W
4	Force_boost		R/W
3			R/W
2	En_force_ restart first write 1 to bit2, then write 1 to bit5, which can trigger the chip reset internally.		R/W
1	En_force_boost first write 1 to bit1, then write 1 to bit4, which can trigger BOOST internally.	When BOOST is turned on, write 0 to bit4 when both bit1 and bit4 are 1, which can trigger turning off BOOST and shut down immediately. Only writing 0 to 0x01 register bit2 will only turn off BOOST, but not immediately That is, shut down, shut down or need to wait for light load conditions.	R/W
0			R/W

2.36 BATVADC_DAT0

register address = 0x64

Bit(s)	Name	Description	R/W
7:0	BATVADC[7:0]	Low 8bit of BATVADC data True voltage of BATPIN	R

2.37 BATVADC_DAT1

register address = 0x65

Bit(s)	Name	Description	R/W

7:0	BATVADC[15:8]	High 8bit of BATVADC data VBAT = BATVADC * 0.26855mv + 2.6V True voltage of BATPIN	R

2.38 BATIADC_DAT0

register address = 0x66

Bit(s)	Name	Description	R/W
7:0	BATIADC [7: 0]	Low 8bit of BATIADC data	R

2.39 BATIADC_DAT1

register address = 0x67

Bit(s)	Name	Description High	R/W
7:0	BATIADC [15: 8]	8bit of BATIADC data IBAT = BATIADC * 1.27883mA LSB=1.27883mA corresponds to 10mOhm sampling resistor (Complement format, charge is positive, discharge is negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.40 SYSVADC_DAT0

register address = 0x68

Bit(s)	Name	Description	R/W
7:0	SYSVADC [7: 0]	Lower 8bits of SYSVADC data	R

2.41 SYSVADC_DAT1

register address = 0x69

Bit(s)	Name	Description	R/W
7:0	SYSVADC [15: 8]	High 8bit of SYSVADC data SYSV=SYSVADC * 1.61133mV + 15.6V (Complement format, valid values are usually negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.42 SYSIADC_DAT0

register address = 0x6A

Bit(s)	Name	Description	R/W
7:0	SYSIADC [7: 0]	Lower 8bits of SYSIADC data	R

2.43 SYSIADC_DAT1

register address = 0x6B

Bit(s)	Name	Description	R/W
7:0	SYSIADC [15: 8]	High 8bits of SYSIADC data SYSI=SYSIADC * LSB LSB=0.6394mA corresponds to 10mOhm sampling resistor (Complement format, discharge is negative, charge is positive) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.44 VINIADC_DAT0

register address = 0x6C

Bit(s)	Name	Description	R/W
7:0	VINIADC [7: 0]	Low 8bit of VINIADC data	R

2.45 VINIADC_DAT1

register address = 0x6D

Bit(s)	Name	Description	R/W
7:0	VINIADC [15: 8]	VINIADC data high 8bit VINI=VINIADC *LSB LSB=0.6394mA corresponds to 10mOhm sampling resistance, the actual situation needs to be based on the PCB The trace impedance from VSN to VIN + the on-resistance of MOS transistor is folded with the multiple relationship of 10mOhm Calculate. If the actual impedance is 20mOhm, which is 2 times of 10mOhm, then LSB is also theoretical 1/2 of the value The ADC needs to be active only when VINOK and VBUSOK are active at the same time in the charging state and VIN MOS is turned on. will start (Complement format, discharge is positive, charge is negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.46 VBUSIADC_DAT0

Register Address = 0x6E default 0x00

Bit(s)	Name Description	VBUSIADC data	R/W
	VBUSIADC [7: 0]	low 8bit 7:0	R

2.47 VBUSIADC_DAT1

register address = 0x6F

Bit(s)	Name Description	VBUSIADC[15:8]	R/W
7:0	High 8bits of VBUSIADC data	VBUSI=VBUSIADC*LSB LSB=0.6394mA corresponds to 10mOhm sampling resistance, the actual situation needs to be based on the PCB The wiring impedance from VSN to VBUS + the on-resistance of MOS transistor is carried out with the multiple relationship of 10mOhm discount. If the actual impedance is 20mOhm, which is 2 times of 10mOhm, then LSB is also reasonable 1/2 of the argument It is required when VINOK and VBUSOK are active at the same time in the charging state and VBUS MOS is turned on; or The ADC will only start when VBUS MOS is turned on and other MOSs are also turned on; (Complement format, discharge is positive, charge is negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.48 VOUT1IADC_DAT0

register address = 0x70

Bit(s)	Name Description	VOUT1IADC[7:0]	R/W
	Low 8bit of VOUT1IADC data 7:0		R

2.49 VOUT1IADC_DAT1

Register Address = 0x71 default 0x00

Bit(s)	Name Description	VOUT1IADC[15:8]	R/W
	High 8bit of VOUT1IADC data 7:0		R

		VOUT1I= VOUT1IADC *LSB LSB=0.6394mA corresponds to 10mOhm sampling resistance, the actual situation needs to be based on the PCB The wiring impedance from VSN to VOUT1 + the on-resistance of MOS transistor is carried out with the multiple relationship of 10mOhm discount. If the actual impedance is 20mOhm, which is 2 times of 10mOhm, then LSB is also reasonable 1/2 of the argument The ADC will only start when other MOSs are also turned on when the VOUT1 MOS is turned on; (Complement format, discharge is positive, charge is negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	

2.50 VOUT2IADC_DAT0

register address = 0x72

Bit(s)	Name	Description	R/W
7:0	VOUT2IADC[7:0] Low 8bit of	VOUT2IADC data	R

2.51 VOUT2IADC_DAT1

register address = 0x73

Bit(s)	Name Description VOUT2IADC[15:8] High 8bit of		R/W
7:0	VOUT2IADC data	VOUT2I= VOUT2IADC *LSB LSB=0.6394mA corresponds to 10mOhm sampling resistance, the actual situation needs to be based on the PCB The wiring impedance from VSN to VOUT2 + the on-resistance of the MOS transistor is carried out with the multiple relationship of 10mOhm discount. If the actual impedance is 20mOhm, which is 2 times of 10mOhm, then LSB is also reasonable 1/2 of the argument The ADC will start only when other MOSs are also turned on when the VOUT2 MOS is turned on; (Complement format, discharge is positive, charge is negative) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.52 RSETADC_DAT0

register address = 0x74

Bit(s)	Name	Description	R/W
7:0	RSETADC [7: 0]	Low 8bit of RSETADC data	R

2.53 RSETADC_DAT1

register address = 0x75

Bit(s)	Name	Description High	R/W
7:0	RSETADC [15: 8]	8bit of RSETADC data RSET=RSETADC*0.26855mv+1.5V (complement format) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.54 GPIADC_DAT0

register address = 0x78

Bit(s)	Name	Description	R/W
7:0	GPIADC [7:0]	Low 8bit of GPIADC data	R

2.55 GPIADC_DAT1

register address = 0x79

Bit(s)	Name	Description	R/W
7:0	GPIADC [15:8] High	8bits of GPIADC data GPI=GPIADC*0.26855mv+1.5V (complement format) For example: 00000000_00000001 means 1 11111111_11111111 means -1 11111111_11111110 means -2	R

2.56 BATOCV_DAT0

register address = 0x7A

Bit(s)	Name	Description	R/W
7:0	BATOCV [7: 0]	Low 8bit of BATOCV data BAT voltage is the voltage that is compensated by the internal resistance of the cell and the current of the cell	R

2.57 BATOCV_DAT1

register address = 0x7B

Bit(s)	Name	Description	R/W
7:0	BATOCV [15:8] High	8bit of BATOCV data OCV = BATOCV * 0.26855mv + 2.6V BAT voltage is the voltage that is compensated by the internal resistance of the cell and the current of the cell	R

2.58 POWER_DAT0

register address = 0x7C

Bit(s)	Name	Description	R/W
7:0	POWER[7:0]	Low 8bit of POWER data	R

2.59 POWER_DAT1

register address = 0x7D

Bit(s)	Name Description POWER [15:8]		R/W
7:0	High 8bit of POWER data	OCV=POWER*8.44mW	R

2.60 FLAG0

register address = 0x7E

Bit(s)	Name	Description	R/W
7		BOOST short circuit abnormal flag (requires write 1 to clear 0)	R/W
6		BOOST undervoltage abnormal flag (requires write 1 to clear 0)	R/W
5		BOOST Abnormal hiccup flag (need to write 1 to clear 0)	R/W
4		BOOST Abnormal shutdown flag (need to write 1 to clear 0)	R/W
3		BOOST startup failure flag (requires writing 1 to clear 0)	R/W
2		NTC low temperature flag (need to write 1 to clear 0)	R/W
1		NTC high temperature flag (need to write 1 to clear 0)	R/W
0		IC internal high temperature flag (need to write 1 to clear 0)	R/W

2.61 FLAG1

register address = 0x7F

Bit(s)	Name	**Description** Button	R/W
7		double-click sign (requires writing 1 to clear 0)	R/W
6		Button long press sign (requires writing 1 to clear	R/W
5		0) Button short press sign (requires writing 1 to clear 0)	R/W
4			
3			
2			
1		VBUS overvoltage flag (requires writing 1 to clear 0)	R/W
0		VIN overvoltage flag (requires writing 1 to clear 0)	R/W

2.62 **BST_POWERLOW**

register address = 0x81

Bit(s)	Name	Description	R/W
7:5			
4:0	Set_power_th Config BOOST powerlow hreshold	powerlow LSB 16.88mW	RW

2.63 **RSET**

register address = 0x82

Bit(s)	Name	Description	R/W
7:4	Set_bat_imp Register Config impendece	6.25mOhm* set_bat_imp The internal register sets the internal compensation of the cell	RW
3:2	Set_imp_offse t	Config impendence offset 00: 0 mohm 01: 12.5 mohm 10:25 mohm 11:50 mohm Set internal resistance = offset+6.25mOhm* set_bat_imp	RW
1	Sel_ext_imp	Select external impendence 1:external impendence control 0:internal register control When DPB DMB works in I2C mode, RSET pin will be used as INT wake-up function, this RSET will automatically switch to the internal register setting when	RW
0			

2.64 BST_ISYSLOW

register address = 0x84

Bit(s)	Name	Description	R/W
7	En_isyslow_r ISYSLOW BOOST state output total current light load shutdown enable	1:enable 0:disable	RW
6	En_powerlow _r	POWERLOW BOOST state output total power light load shutdown enable 1:enable 0:disable (The threshold setting register is at 0x81 bit4:0)	RW
5:0	Set_isys_th	Config ISYS_LOW hreshold (light load output current threshold setting) isyslow LSB 2.55766mA	RW

2.65 IPMOSLOW

register address = 0x86

Bit(s)	Name	Description	R/W
7:0	Set_ipmos_th Config IPMOS hreshold	The current threshold setting of actively closing the light-load output port when multi-port output LSB=2.55766mA corresponds to 10mOhm sampling resistance, the actual situation needs to be based on the PCB	RW

		The trace impedance from VSN to VOUT1 or VOUT2 + MOS transistor on-resistance and 10mOhm The multiple relationship is converted. If the actual impedance is 20mOhm, which is 2 times of 10mOhm, Then the LSB is also 1/2 times the theoretical value	

2.66 BATOCV_LOW

register address = 0x88

Bit(s)	Name	Description	R/W
7:5			
4	en_dndcp	BATOCV low voltage closes the chip's own fast charge output function enable 1:enable 0:disable *The fast charging triggered by the external fast charging protocol IC is not subject to this control	RW
3:0	Set_dndcpth_r	BATOCV low voltage shutdown fast charge threshold (Offset = 2.6V ÿ LSB = 69mV)	RW

2.67 IPMOSLOW_TIME

register address = 0x90

Bit(s)	Name	Description	R/W
7:6		The relationship between PMOS ilow time and light load shutdown time: 00: Half of the light load shutdown time 01: Same as light-load shutdown time 10: 2 times the light load shutdown time 11: 4 times the light load shutdown time	R/W
5:0			

2.68 QC_VMAX

register address = 0x96

Bit(s)	Name 7	Description	R/W
6		Set the MAX maximum voltage supported by QC SRC mode 1:12V 0: 9V	R/W
5:0			

2.69 BATOCV_LOW_DN

register address = 0x9F

Bit(s)	Name 7:6	Description	R/W
5:0		BATOCV_LOW ÿdefault 2.900Vÿ 2900+data*8.59375mv	R/W

2.70 DCP_DIG_CTL0

register address = 0xA0

Bit(s)	Name	Description	R/W
7:4			
3	En_vbus_dcp_r	DPC DMC enable for VBUS 1:enable 0:disable	RW

2	En_vin_dcp_r	DPB DMB enable of VIN (when DPB DMB is used as I2C, this BIT is invalid) 1:enable 0:disable	RW
1	En_vout2_dcp_r	DPA2 DMA2 enable of VOUT2 (this BIT is invalid in IP5322FB specification) 1:enable 0:disable	RW
0	En_vout1_dcp_r	DPA1 DMA1 enable for VOUT1 1:enable 0:disable	RW

2.71 DCP_DIG_CTL2

register address = 0xA2

Bit(s)	Name	Description	R/W
7	En_mtkrx9v_r	Maximum voltage setting supported by MTK PE 1.1 RX 0ÿ12V 1 ÿ 9V	RW
6	En_mtkrx2_r	MTK PE2.0 RX enable 1:enable 0:disable	RW
5	En_mtkrx1_r	MTK PE1.1 RX enable 1:enable 0:disable	RW
4	en_sfcpsrc_r	SFCP SRC enable 1:enable 0:disable	RW
3	En_afcsrc_r	AFC SRC Enable 1:enable 0:disable	RW
2	En_fcpsrc_r	FCP SRC Enable 1:enable 0:disable	RW
1	En_qc3src_r	QC3.0 SRC enable 1:enable 0:disable	RW
0	En_qc2src_r	QC2.0 SRC enable (QC SRC output is always enabled) 1:enable 0:disable	RW

2.72 BOOST_5V_ISET

register address = 0xA8

Bit(s)	Name	Description	R/W
7:6			
5:0	Iset_5v_r	The total output current limit setting when BST is 5V, the default value is about 3.4A, step50mA (This register does not affect the 18W power limit when greater than 5V)	RW

2.73 DCP_DIG_CTL10

register address = 0xAA

Bit(s)	Name	Description	R/W
7:6	At_same_mode is the state of charging and discharging port DP DM	11: Support Apple, Samsung, BC1.2 10: Floating 01: short circuit 00: Support Apple, Samsung, BC1.2	RW
5:0			

2.74 SYS_STATUS

register address = 0xD1

Bit(s)	Name	Description	R/W
7:5			R
4	CHG_EN	current status indication 0: Discharge state 1: charging state	R
3			R
2:0	SYS_STATE 000: Standby	001: 5V charging 010: Single-port charging and discharging 011: Multi-port charging and discharging at the same time 100: High-voltage fast charging 101: 5V discharge 110: Multi-port 5V discharge 111: High voltage fast charge and discharge	R

2.75 KEY_IN

register address = 0xD2

Bit(s)	Name	Description	R/W
7:6			R
5	VBUSOK	VBUS voltage valid flag, TYPEC charging and discharging this bit will be valid	R
4	VINOK	VIN voltage valid flag	R
3:1			R
0	Key_in	The real-time status of the button pins, 0 means the button is currently pressed	R

2.76 OV_FLAG

register address = 0xD3

Bit(s)	Name	Description	R/W
7:4			R
3	BATLOW	The BAT voltage is lower than the low power threshold set by the 0x10 register	R
2	VSYSOV	VSYS voltage is higher than 5.6V	R
1	VBUSOV	VBUS voltage is higher than the overvoltage threshold set by register 0x12	R
0	WINE	VIN voltage is higher than the overvoltage threshold set by register 0x11	R

2.77 VIN_VBUS_STATE

register address = 0xD5

Bit(s)	Name	Description	R/W
7:6			R
5:3	VBUS_STATE	The range to which the input voltage falls when VBUS is charging 000:5V voltage range 001:7V voltage range 011: 9V voltage range 111:12V voltage range	R
2:0	VIN_STATE	The range to which the input voltage falls when VIN is charging 000:5V voltage range 001:7V voltage range 011: 9V voltage range 111:12V voltage range	R

2.78 CHG_STATUS

register address = 0xD7

Bit(s)	Name		R/W
7	Chgop	**DescriptionCharging** working status: 0: It may just stop charging detection, it may be full, or it may be abnormal protection (Timer Out, or input OV, or NTC abnormal), or it may not start charging, For the specific state, please refer to sys_state, chg_state and NTC. 1: Charging	R
6	Chg_end	Charge full Charger end sign: 0: not fully charged 1: fully charged	R
5	Chg_ovtime Constant voltage and constant current total time Timer Out	0: No timeout when totaling constant voltage and constant current 1: Timeout when constant voltage and constant current total	R
4	Cv_ovtime	Constant voltage timer Timer Out 0: The constant voltage timer has not timed out 1: Constant voltage timer timeout	R
3	Tk_ovtime	Trickle Timer Out 0: The trickle timer has not timed out 1: Trickle timer timeout	R
2:0	Chg_state	charging 000ýIDLE 001: Trickle charge phase 010: Constant current charging stage 011: Constant voltage charging stage 100: stop charging detection 101: The battery is fully charged and finished 110ýTimer Out	R

2.79 LOW_STATUS

register address = 0xD9

Bit(s)	Name	Description	R/W
7			R
6	POWLOW	The current total output power is less than the set low-power shutdown threshold	R
5			R
4	BATOCV_LOW	The BAT_OCV voltage is lower than the low-power shutdown threshold set by the 0x9F register.	R
3	ISYSLOW	The current total output current is less than the set low-current shutdown threshold.	R
2:0			R

2.80 NTC_FLAG

register address = 0xDA

Bit(s)	Name	Description	R/W
7	NTC_SC	NTC short-circuit flag 0: External short to ground, NTC is invalid 1: Externally connected to NTC resistor, NTC is valid	R
6:4	NTC_IN	000: high temperature 100: Moderate temperature 110: normal temperature 111: low temperature	R
3:0			R

2.81 MOS_ON

register address = 0xE5

Bit(s)	Name	Description	R/W

7	CELEBRATION	0: The current charging is using the VIN channel 1: The current charging is using the VBUS channel	R
6	VINOK_in	VIN voltage valid flag	R
5	VBUSOK_in	VBUS voltage valid flag, TYPEC charging and discharging this bit will be valid	R
4	VIN_pmos_en	VIN MOS on	R
3			R
2	VBUS_pmos_en VBUS MOS on		R
1	VOUT2_mos_en VOUT2 MOS on		R
0	VOUT1_mos_en VOUT1 MOS on		R

2.82 BST_V_FLAG

register address = 0xFB

Bit(s)	Name	Description	R/W
7:4			R
3	BST_V_FLAG[3]	BOOST output is greater than 10V and less than or equal to 12V	R
2	BST_V_FLAG[2]	BOOST output is greater than 8V and less than or equal to 10V	R
1	BST_V_FLAG[1]	BOOST output is greater than 6V and less than or equal to 8V	R
0	BST_V_FLAG[0]	BOOST fast charging logo	R

2.83 TYPE-C_OK

register address = 0XB8

Bit(s)	Name	Description	R/W
7:6			R
5	CC_SRC_OK	Type-C power adapter connected	R
1	CC_SNK_OK	Type-C has power output turned on	R
0			R

IP5328P register is updated here , IP5328 is 0XFD register

2.84 TYPE-C_FLAG

register address = 0xFF

Bit(s) 7	Name	Description The power	R/W
	Snk_at_3p0a	output capacity of TYPE-C connection is 3.0A The power output	R
6	Snk_at_1p5a	capacity of TYPE-C connection is 1.5A The power output capacity of	R
5	Snk_at_usb	TYPE-C connection is standard USB	R

IP5328P register is updated here , IP5328 is 0XFF register

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