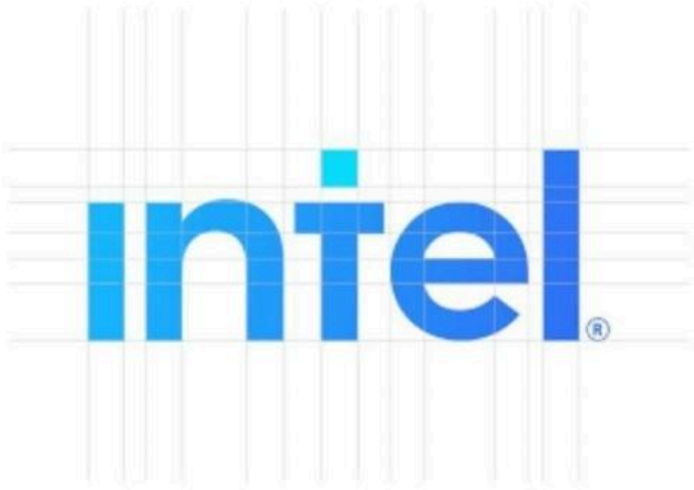
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On

The Design and Implementation of Automated Teller Machine(FSM)Controller

By

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&

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DEPARTMENT OF

COMPUTER SCIENCE AND ENGINEERING

SREE VENKATESWARA COLLEGE OF ENGINEERING

(Approved by AICTE, New Delhi and Affiliated to Jawaharlal Nehru Technological University – Anantapur)

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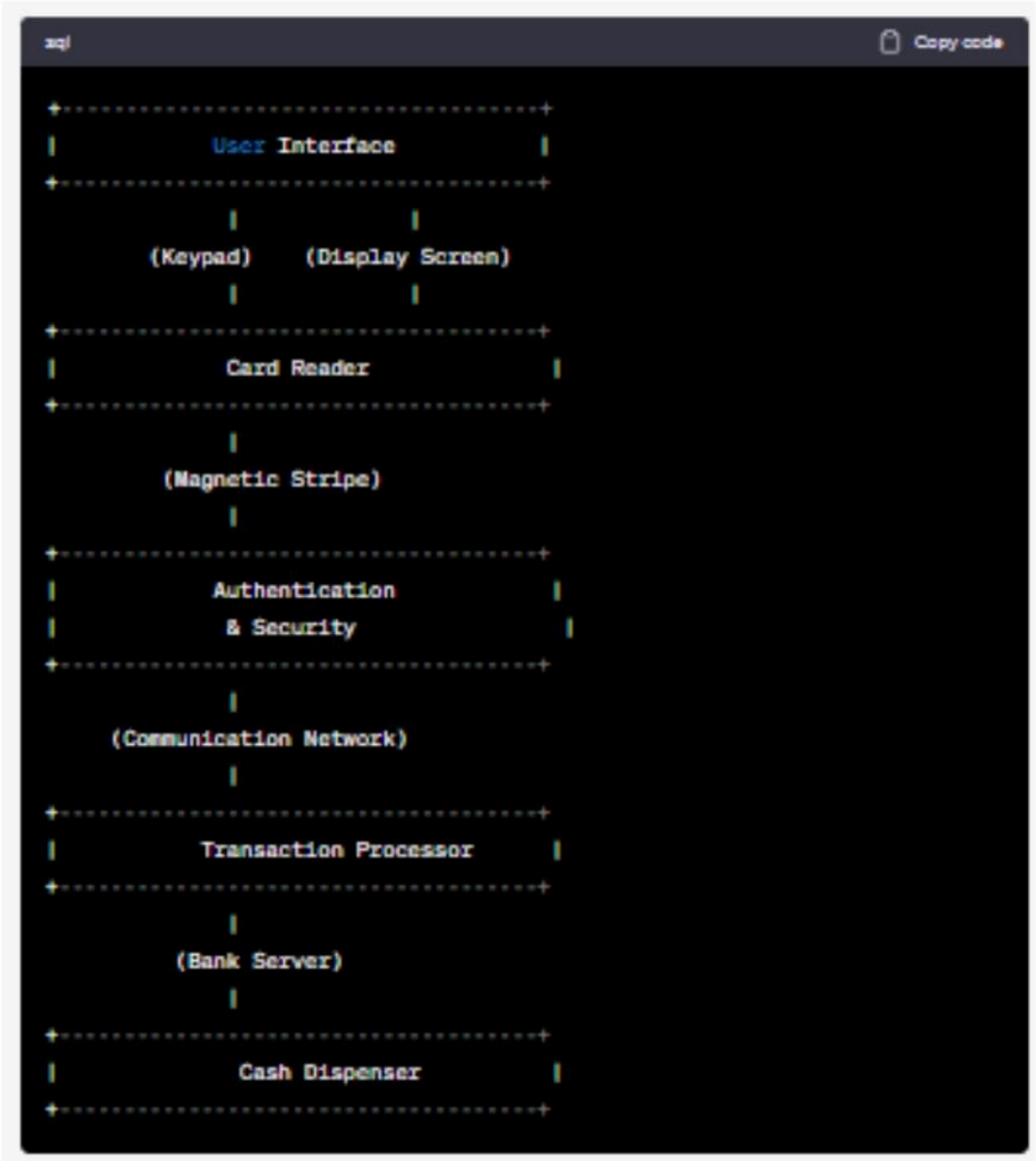
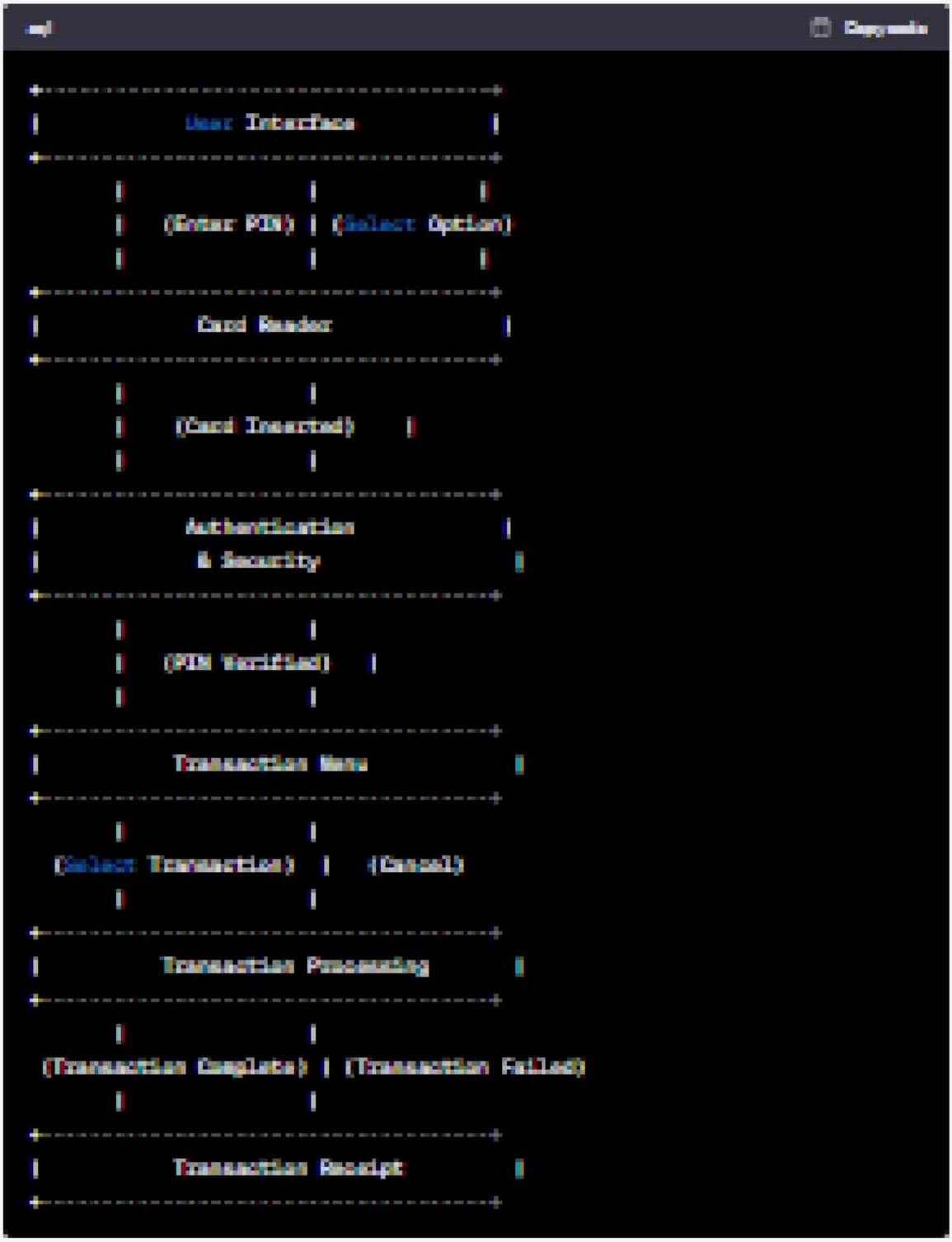
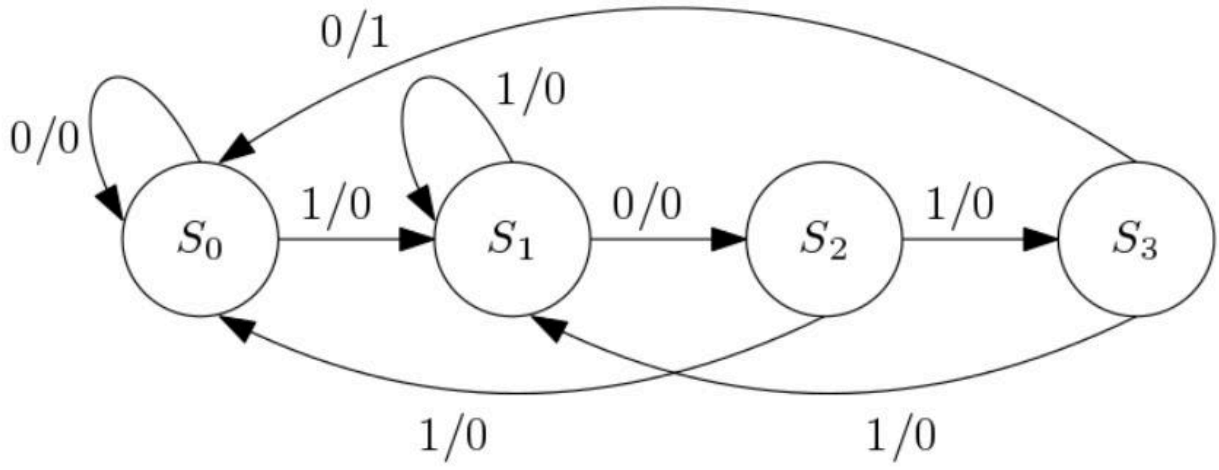
BLOCK DIAGRAM



FSM STATE DIAGRAM



FSM (mealy/moore) of the Design and Implementation of Automated Teller Machine(FSM)



Verolig Code:

```
module ATM_Withdrawal(
  input wire clk,
  input wire reset,
```

```
  input wire enable,
  input wire keypad,
  input wire card_detected,
  input wire pin_entered,
  input wire withdrawal_button,
  output reg dispense_cash,
  output reg transaction_complete
);

  // Internal state definition
  typedef enum logic [2:0] {
    IDLE,
    CARD_INSERTED,
    PIN_ENTERED,
    TRANSACTION,
    CASH_DISPENSED
  } state_t;

  // Registers
```

```
reg [2:0] state_reg;
reg [3:0] incorrect_attempts_reg;
reg [3:0] cash_count_reg;
reg [7:0] pin_reg;

// Constants
parameter MAX_INCORRECT_ATTEMPTS = 3;
parameter WITHDRAWAL_AMOUNT = 100;

// State register and next state logic
always @(posedge clk, posedge reset) begin
  if (reset) begin
    state_reg <= IDLE;
    incorrect_attempts_reg <= 0;
    cash_count_reg <= 0;
    pin_reg <= 0;
  end else begin
    case (state_reg)
      IDLE:
```

```
  if (enable && card_detected)
    state_reg <= CARD_INSERTED;
CARD_INSERTED:
  if (enable && pin_entered)
    state_reg <= PIN_ENTERED;
  else if (!card_detected)
    state_reg <= IDLE;
PIN_ENTERED:
  if (enable && keypad)
    state_reg <= TRANSACTION;
  else if (!pin_entered)
    state_reg <= CARD_INSERTED;
TRANSACTION:
  if (cash_count_reg >= WITHDRAWAL_AMOUNT)
    state_reg <= CASH_DISPENSED;
  else if (!withdrawal_button)
    state_reg <= PIN_ENTERED;
CASH_DISPENSED:
  if (enable)
```

```
        state_reg <= IDLE;
    endcase
  end
end

// State actions and outputs
always @(state_reg or withdrawal_button) begin
  case (state_reg)
    IDLE:
      dispense_cash <= 0;
      transaction_complete <= 0;
    CARD_INSERTED:
      dispense_cash <= 0;
      transaction_complete <= 0;
    PIN_ENTERED:
      dispense_cash <= 0;
      transaction_complete <= 0;
    TRANSACTION:
```

```
        if (withdrawal_button && cash_count_reg <
WITHDRAWAL_AMOUNT) begin
          cash_count_reg <= cash_count_reg + 10;
          dispense_cash <= 1;
        end else begin
          dispense_cash <= 0;
        end
        transaction_complete <= 0;
      CASH_DISPENSED:
        cash_count_reg <= cash_count_reg -
WITHDRAWAL_AMOUNT;
        dispense_cash <= 0;
        transaction_complete <= 1;
    endcase
  end
```

endmodule The designed ATM controller FSM should perform the followingchecks

- Invalid PIN entry (3 times allowed and later it should lock theaccount for next 24 hours)

• Withdraw

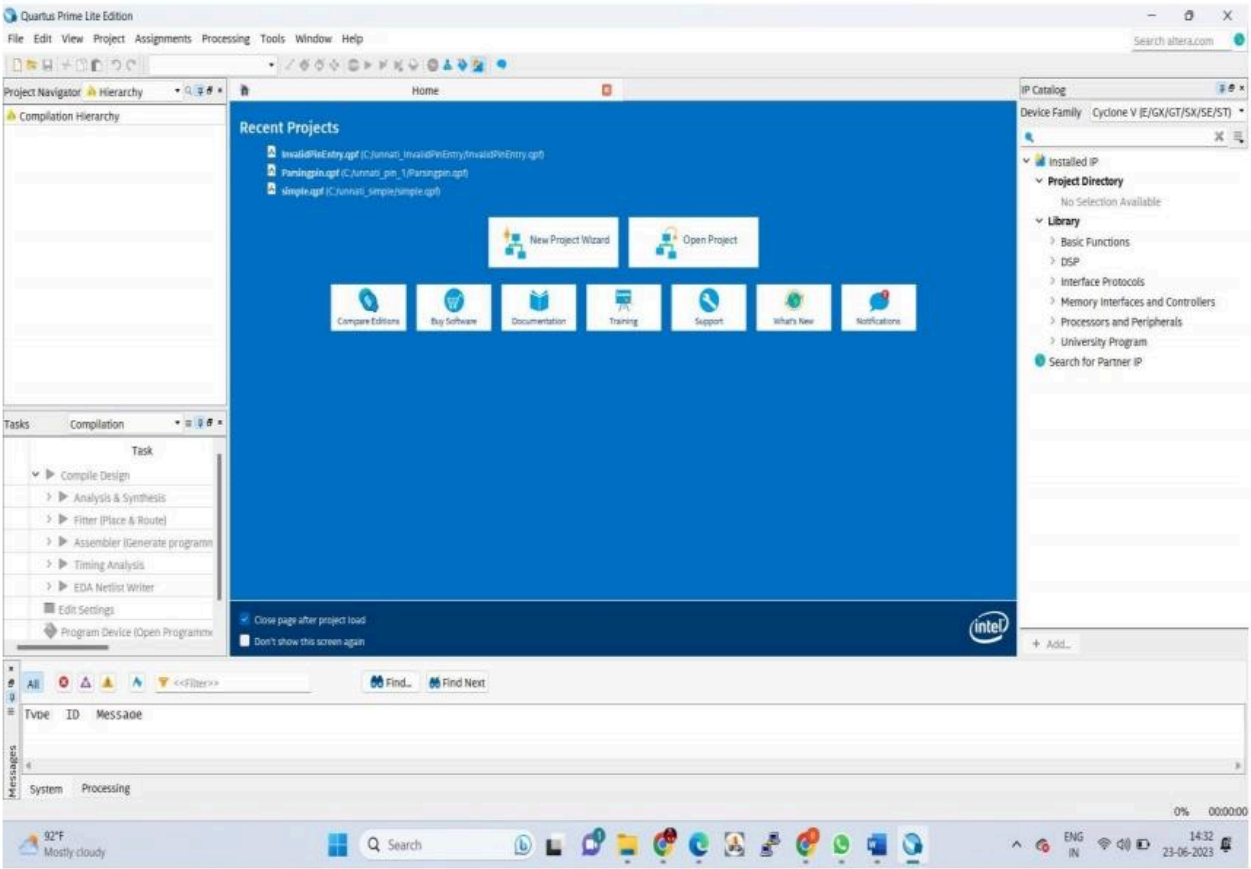
• Deposit

• Old balance and new balance display

• Mini statement for the

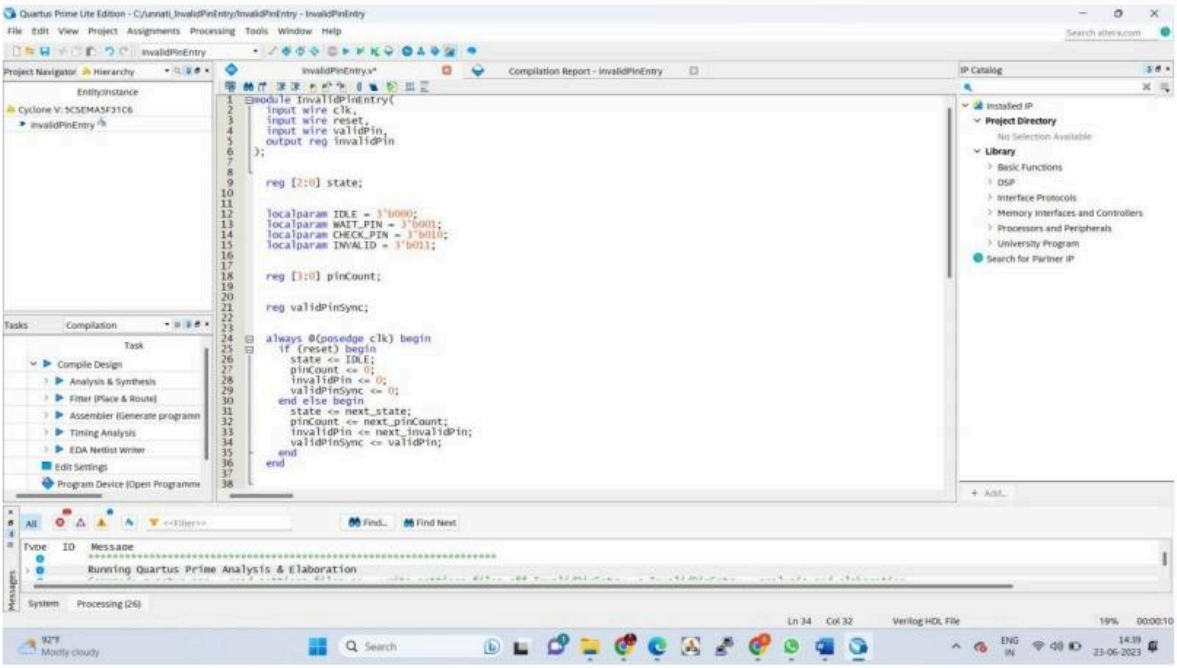
recent transactions

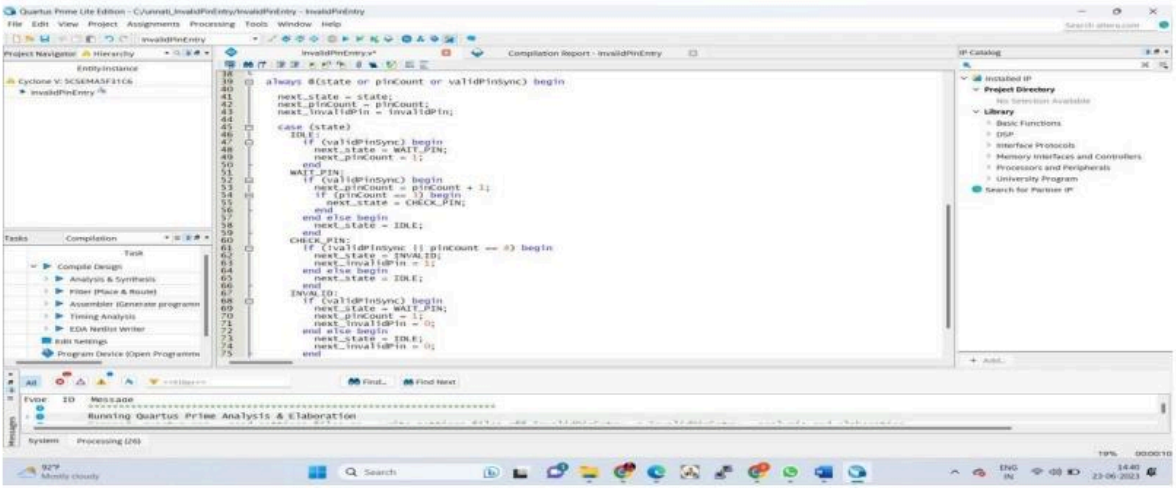
Software Installation:
https://www.intel.com/content/www/us/en/software-kit/665990/intel-quartus-prime-lite-edition-design-software-version-18-1-for- windows.html

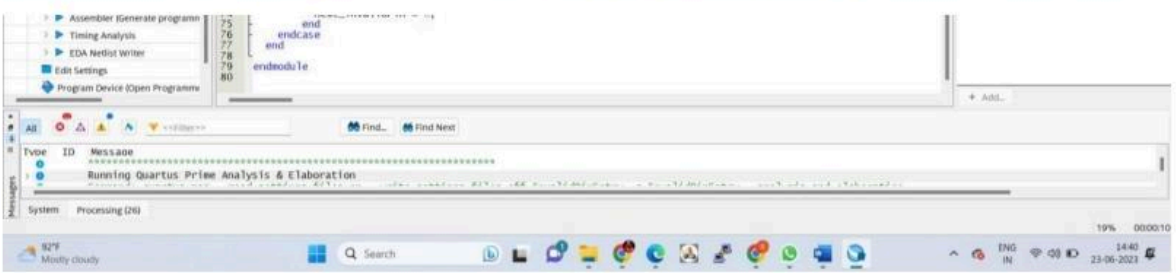


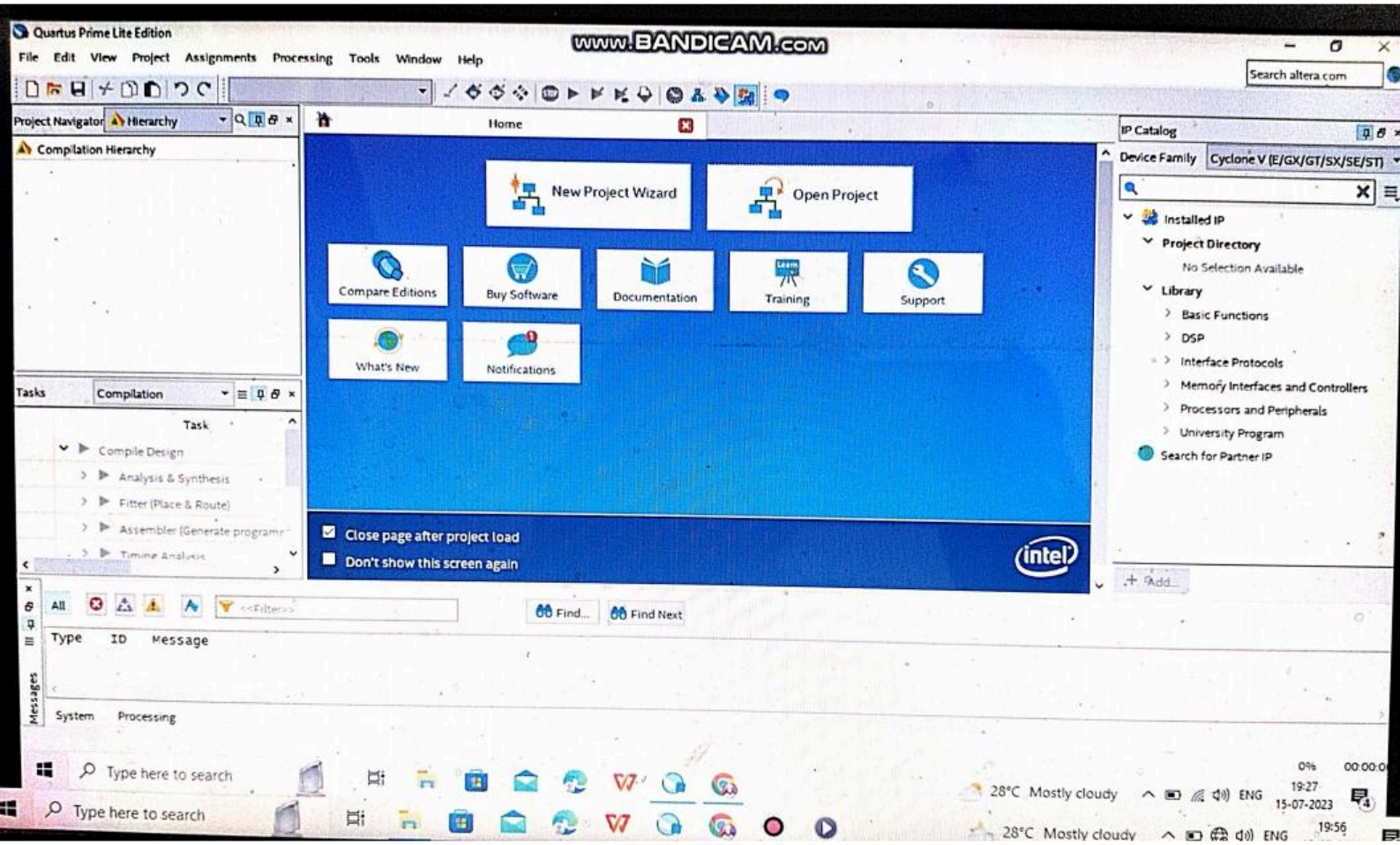
1.INVALID PIN ENTRY:

Verilog Code of Invalid Pin entry:





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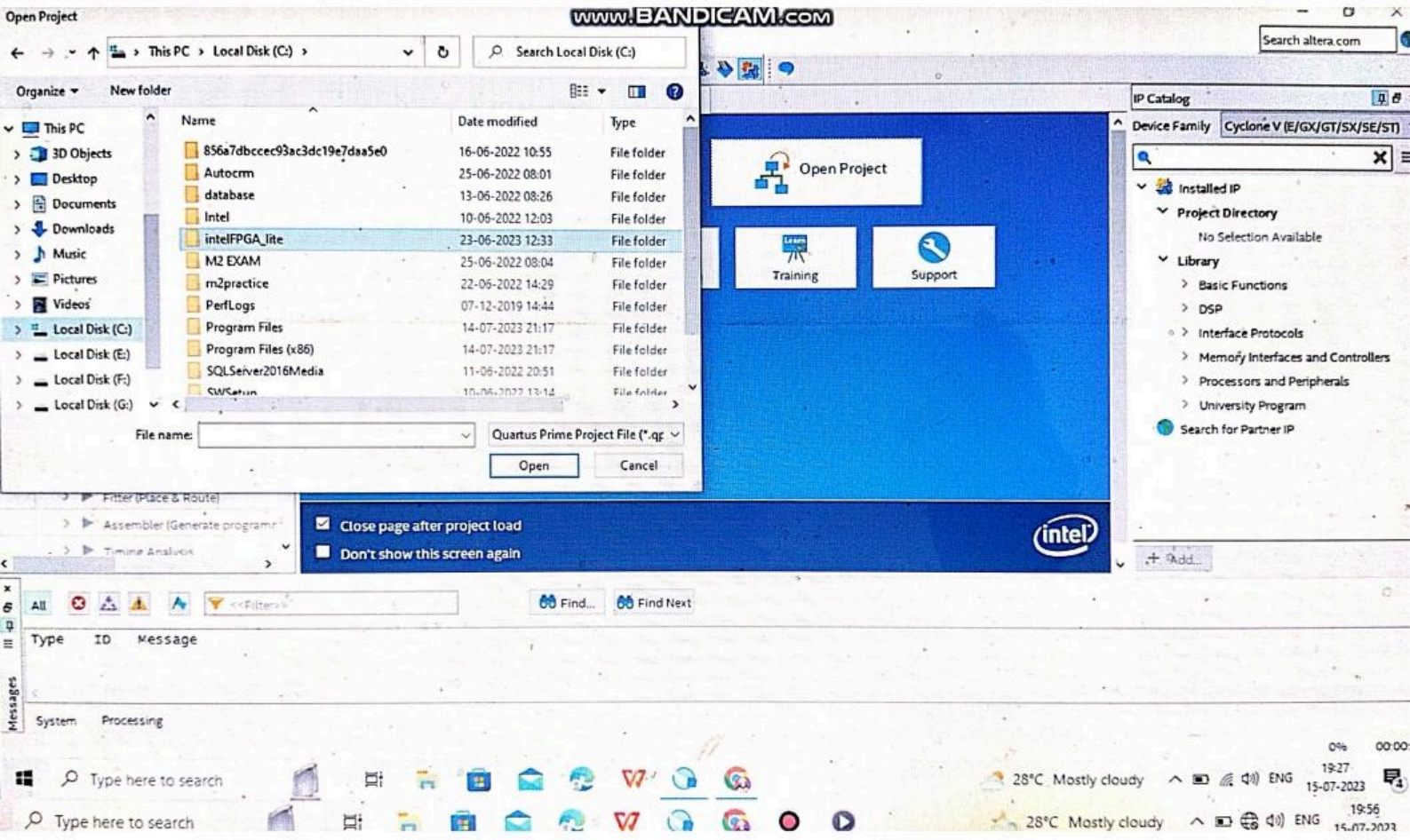
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Intel 10-06-2022 12:03 File folder
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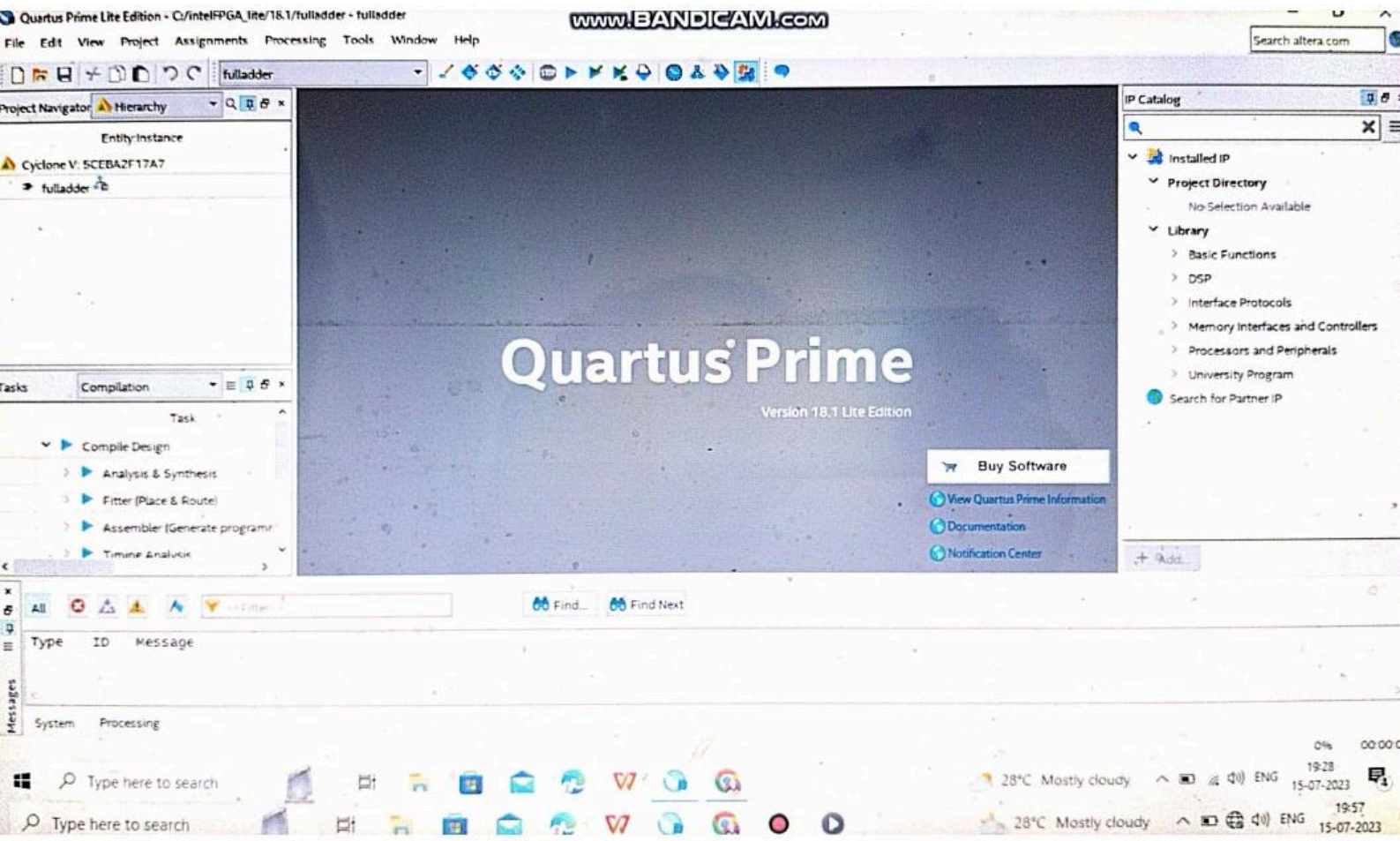
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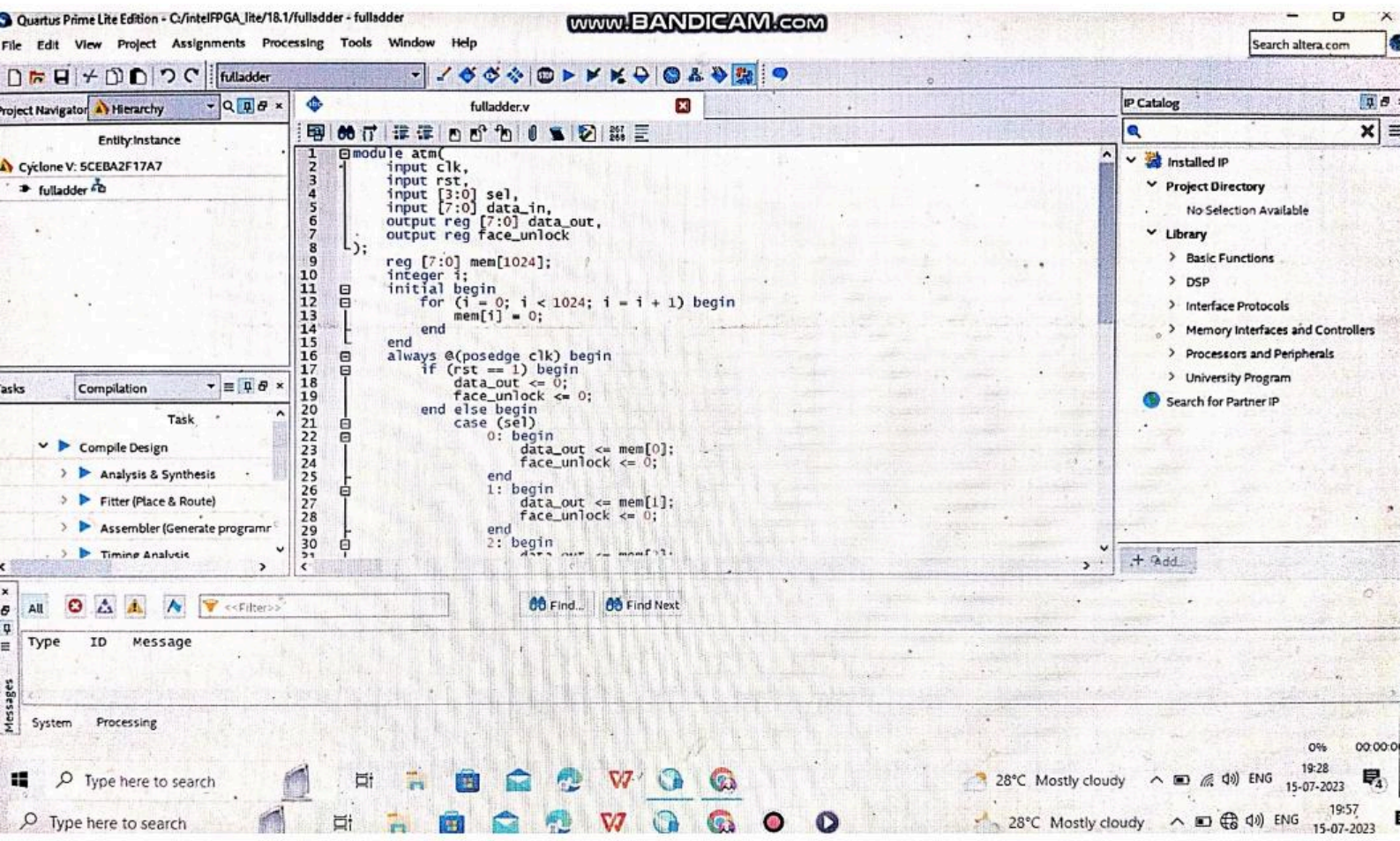
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1 module atm(
2 input clk,
3 input rst,
4 input [3:0] sel,
5 input [7:0] data_in,
6 output reg [7:0] data_out,
7 output reg face_unlock
8);
9 reg [7:0] mem[1024];
10 integer i;
11 initial begin
12 for (i = 0; i < 1024; i = i + 1) begin
13 mem[i] = 0;
14 end
15 end
16 always @(posedge clk) begin
17 if (rst == 1) begin
18 data_out <= 0;
19 face_unlock <= 0;
20 end else begin
21 case (sel)
22 0: begin
23 data_out <= mem[0];
24 face_unlock <= 0;
25 end
26 1: begin
27 data_out <= mem[1];
28 face_unlock <= 0;
29 end
30 2: begin
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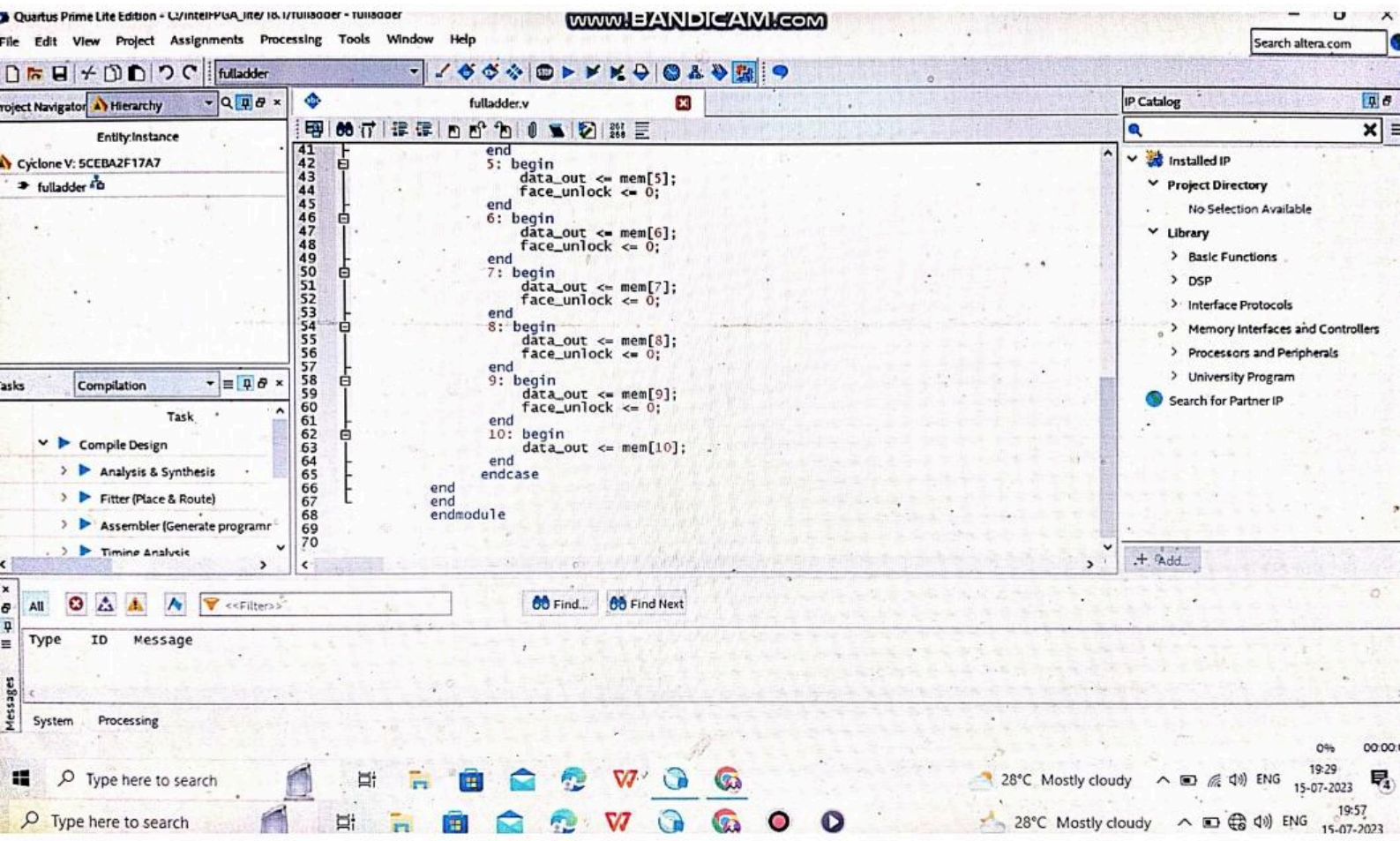
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41 end
42 5: begin
43 data_out <= mem[5];
44 face_unlock <= 0;
45 end
46 6: begin
47 data_out <= mem[6];
48 face_unlock <= 0;
49 end
50 7: begin
51 data_out <= mem[7];
52 face_unlock <= 0;
53 end
54 8: begin
55 data_out <= mem[8];
56 face_unlock <= 0;
57 end
58 9: begin
59 data_out <= mem[9];
60 face_unlock <= 0;
61 end
62 10: begin
63 data_out <= mem[10];
64 end
65 endcase
66 end
67 end
68 endmodule
69
70
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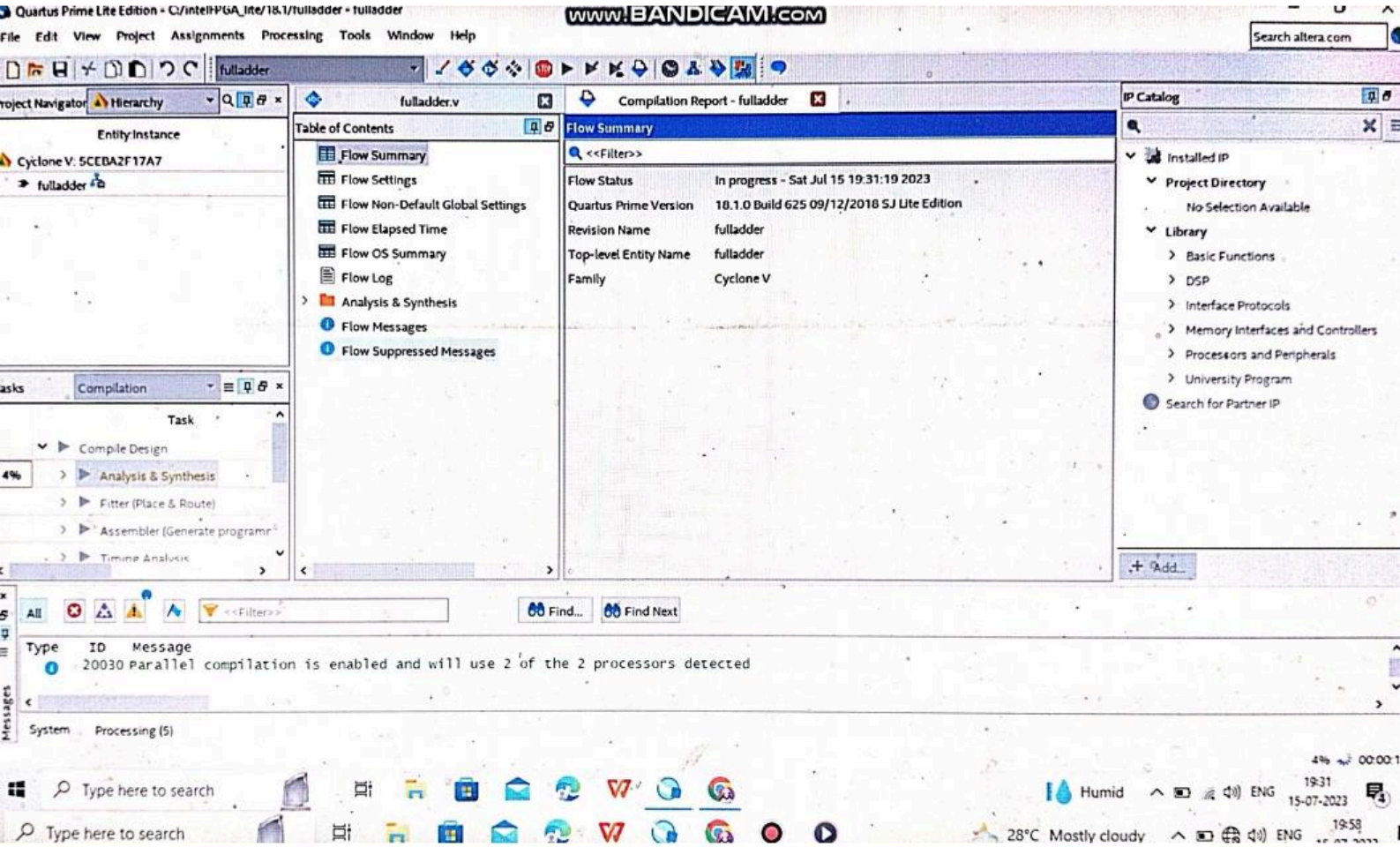
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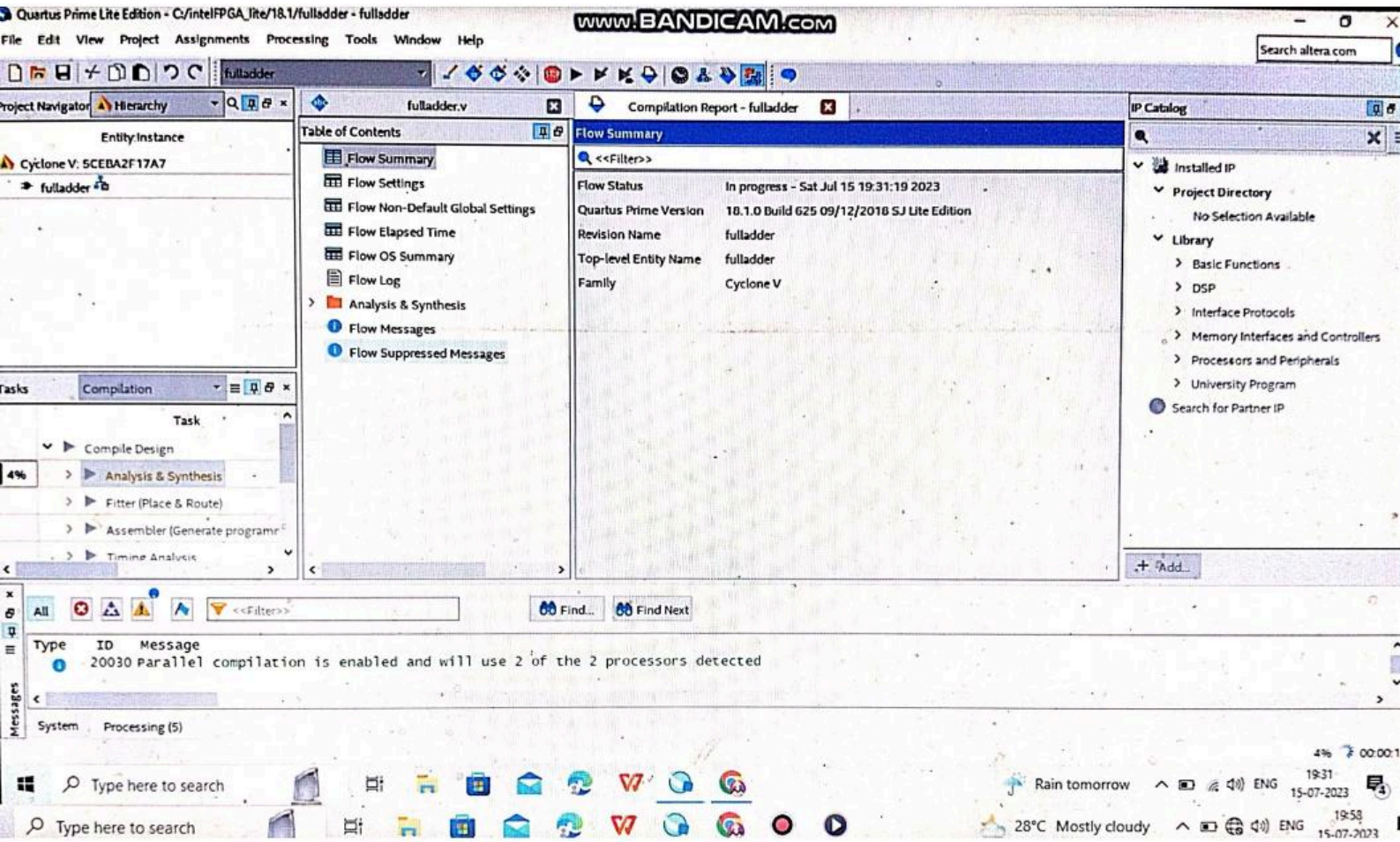
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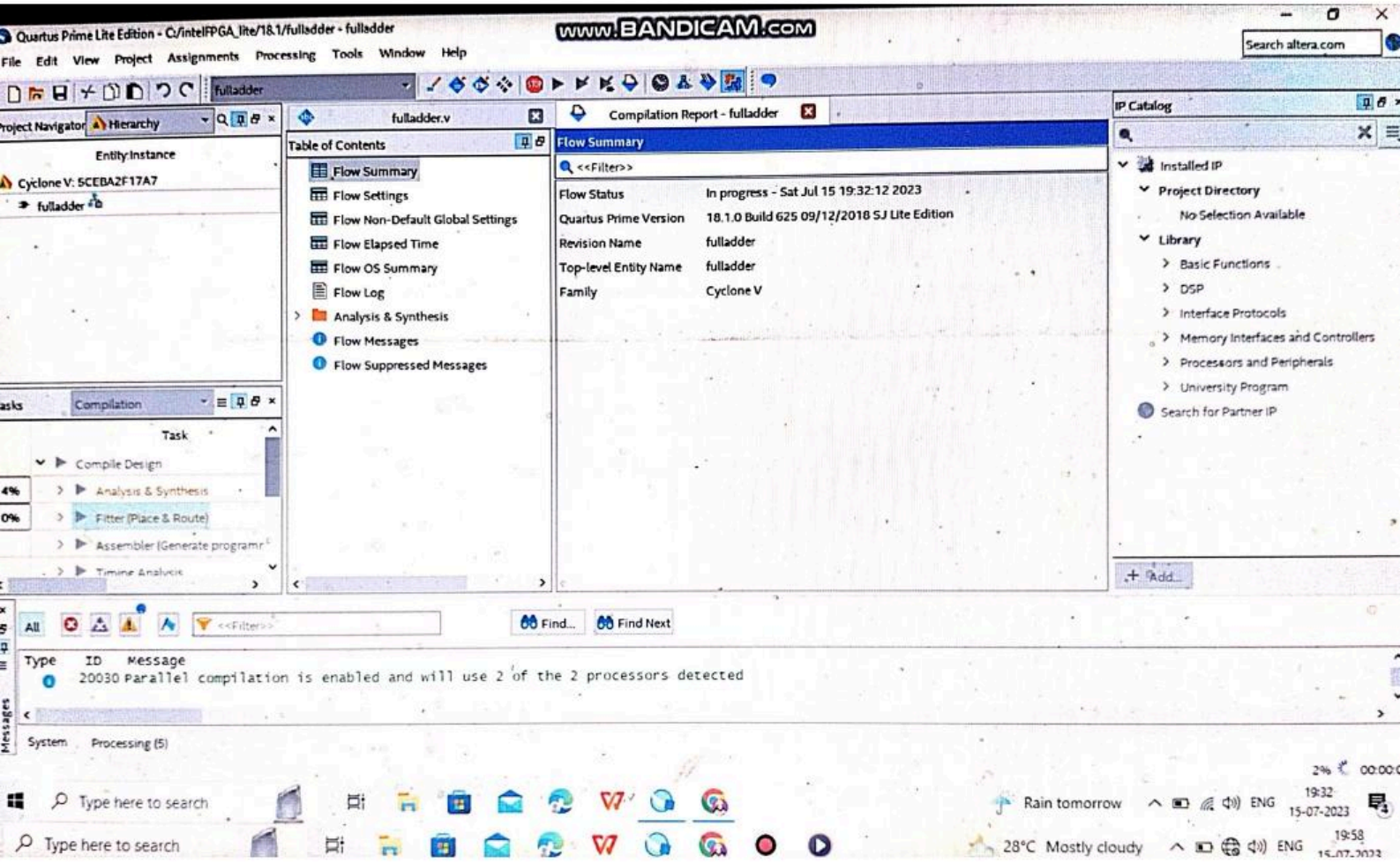
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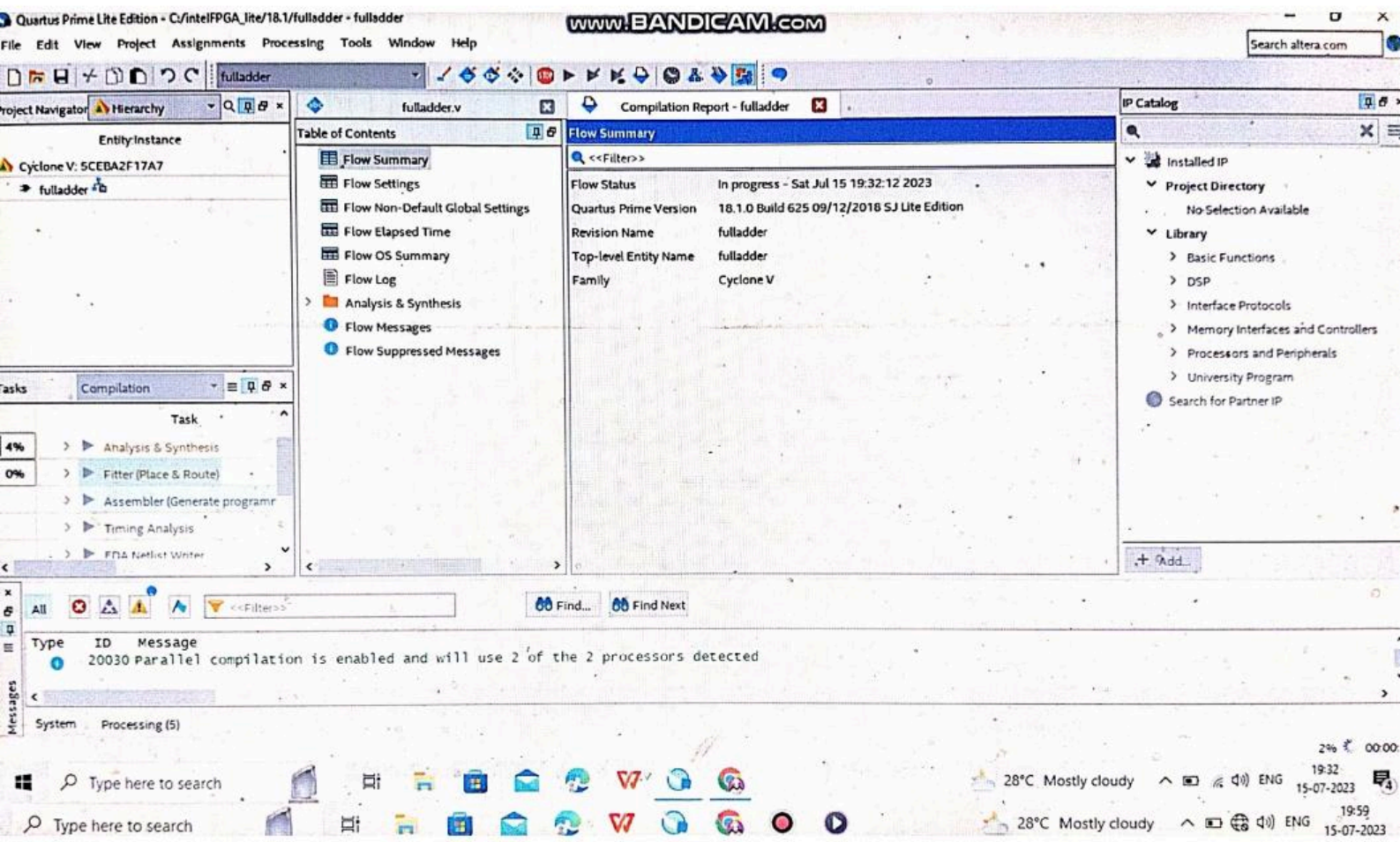
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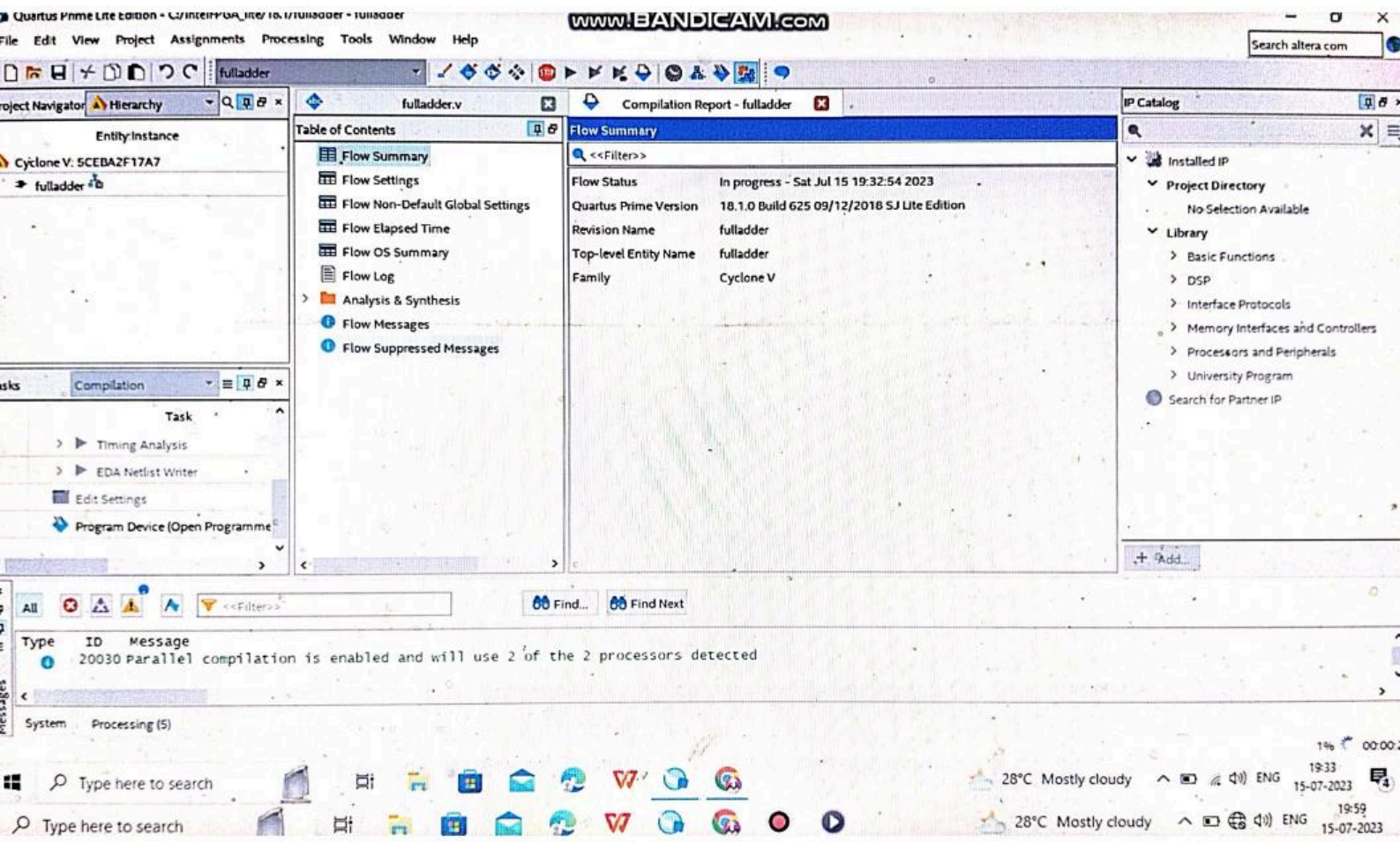
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