Exercise

(1) $F = (AB' + A'B)(C + D')$ Implement with NAND gate

(2) $F = (AB' + CD')E + BC(A + B)$

Design multilevel NAND & NOR ckts

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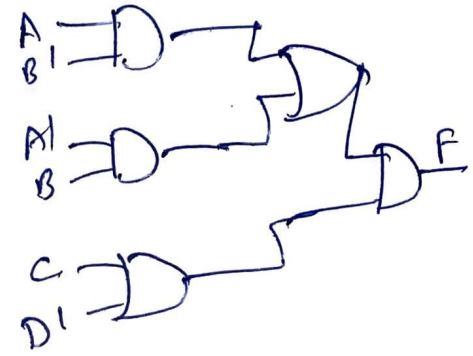
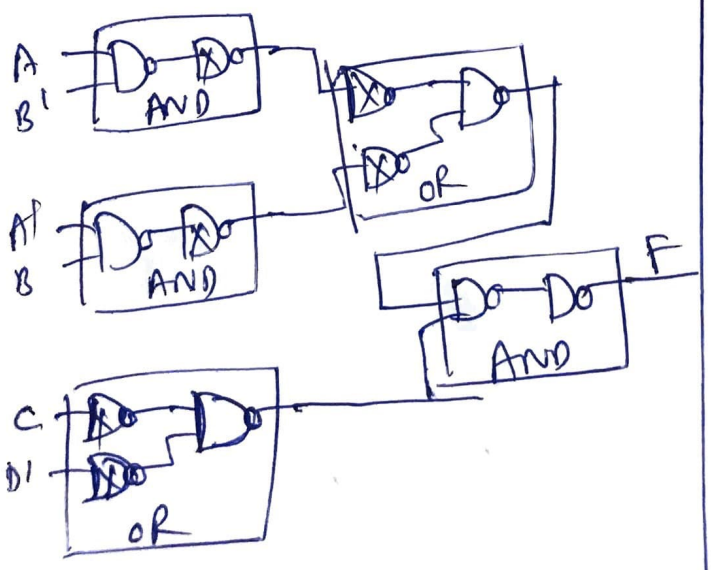
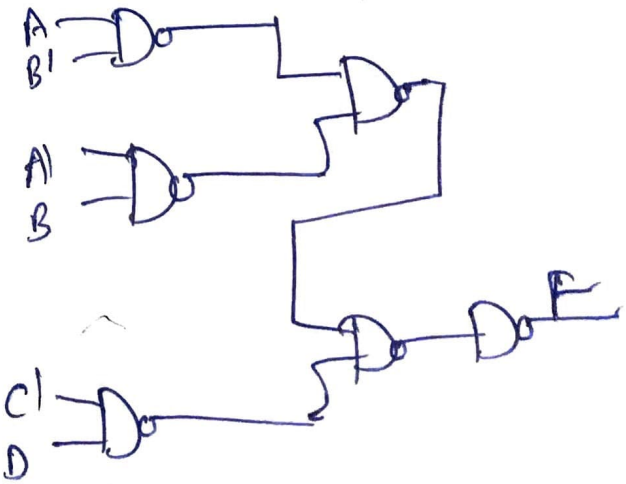
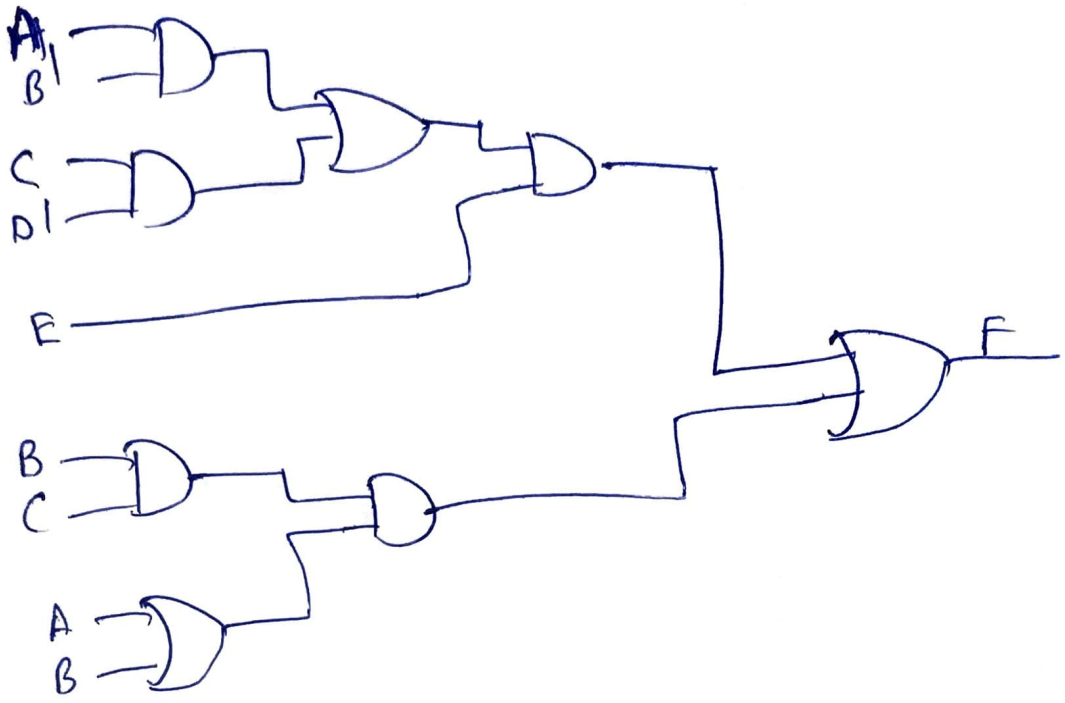
(1)

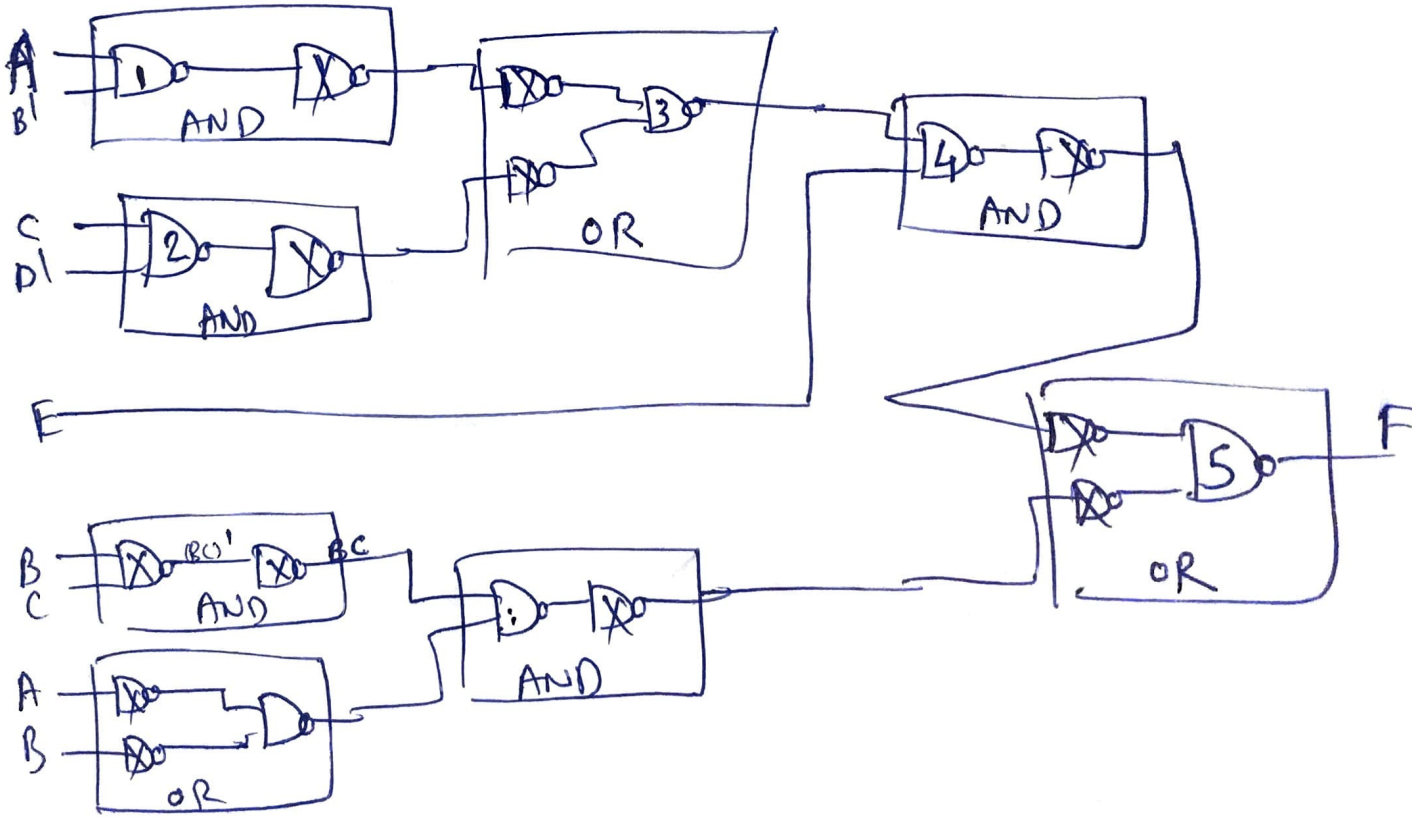


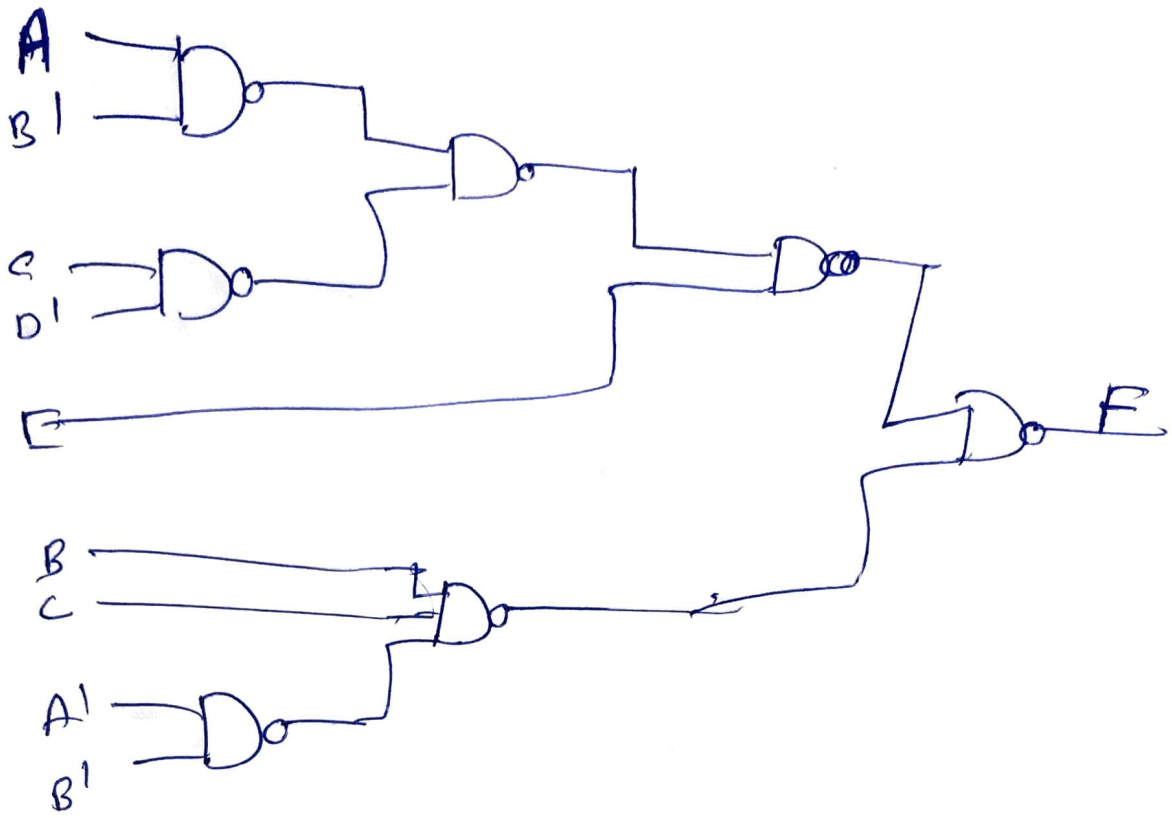




② $F = (AB' + CD')E + BC(A + B)$







NAND ckt