Current 3005 - flux_residual_mod_cat_flux_residual_ (9600, 1, 1) **Time:** 3.09 msecond **Cycles:** 2,627,026 **Regs:** 255 **GPU:** Quadro M5000 **SM Frequency:** 849.66 Mhz **CC:** 5.2

GPU Speed Of Light

SOL SM [%]	55.97	Duration [msecond]	3.09
SOL Memory [%]	18.14	Elapsed Cycles [cycle]	26,27,026.50
SOL TEX [%]	4.86	SM Frequency [Mhz]	849.66
SOL L2 [%]	13.28	Memory Frequency [Ghz]	6.60
SOL FB [%]	1.85		

GPU Utilization

Speed Of Light [%]

Recommendations

Bottleneck [Warning] Compute is more heavily utilized than Memory: Look at 'Compute Workload Analysis' report section to see what the compute pipelines are spending their time doing. Also, consider whether any computation is redundant and could be reduced.

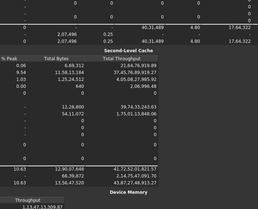
Compute Workload Analysis

Executed Ipc Elapsed [inst/cycle]	0.16	SM Busy [%]	55.97
Executed Ipc Active [inst/cycle]	0.21	Issue Slots Busy [%]	3.56
Issued Ipc Active [inst/cycle]	0.21		

Memory Workload Analysis

Memory Throughput [Gbyte/second]	2.86	Mem Busy [%]	18.14
L1 Hit Rate [%]	0.00	Max Bandwidth [%]	18.63
L2 Hit Rate [%]	98.22	Mem Pipes Busy [%]	1.16

Memory Chart



Shared Memory

	Instructions	Requests	% Peak	Bank Conflicts
Shared Load	0	0	0	0
Shared Store	0	0	0	0
Shared Atomic	0			
Total	0	0	0	0

First-Level Cache

	Instructions	SM->TEX Requests	% Peak	Hit Rate	TEX->L2 Requests	% Peak	L2->TEX Returns	% Peak	TEX->SM Returns	% Peak
Global Load Cached	2,65,310	1,76,438	0.57	0	-	-	20,916	0.02	-	-
Global Load Uncached	-	6,70,742	2.17	-	-	-	36,59,162	4.31	-	-
Local Load Cached	66,626	3,95,471	1.27	0	-	-	3,91,391	0.47	17,64,322	2.10
Local Load Uncached	-	20	0.00	-	-	-	20	0.00		
Surface Load	0	0	0	0	-	-	0	0		
Texture Load	0									
Global Store	1,204	9,604	0.03	-	38,400	0.05	-	-	-	-
Local Store	22,524	1,69,098	0.54	-	1,69,096	0.20	-	-	-	-
Surface Store	0	0	0	-	0	0	-	-	-	-
Global Reduction	0	0	0	-	0	0	-	-	-	-
Surface Reduction	0	0	0	-	0	0	-	-	-	-
Global Atomic	0	0	0	-	-	-	-	-	0	0
Global Atomic Cas		0	0	-	0	0	0	0	0	0
Surface Atomic		0	0	-					0	0
Surface Atomic Cas	0	0	0	-	0	0	0	0	0	0
Loads	3,31,936	12,49,573	4.01	0	2,07,496	0.25	40,51,489	4.80	17,64,322	2.10
Stores	23,728	1,78,702	0.57	-	-	-	-	-	-	-
Total	3,55,664	14,27,373	4.59	0	2,07,496	0.25	40,51,489	4.80	17,64,322	2.10

Second-Level Cache

	TEX->L2 Requests	% Peak	L2->TEX Returns	% Peak	Total Bytes	Total Throughput
Global Load Cached	-	-	20,916	0.06	6,68,112	21,64,76,919.89
Global Load Uncached	-	-	36,59,162	9.54	11,58,13,184	37,45,76,89,919.27
Local Load Cached	-	-	3,91,391	1.05	1,25,24,512	4,05,08,27,985.92
Local Load Uncached	-	-	20	0.00	640	2,06,996.48
Surface Load	0	0	0	0	0	0
Texture Load						
Global Store	38,400	0.10	-	-	12,28,800	39,74,33,243.63
Local Store	1,69,096	-	-	-	54,11,072	1,75,01,13,848.06
Surface Store	0	0	-	-	0	0
Global Reduction	0	0	-	-	0	0
Surface Reduction	0	0	-	-	0	0
Global Atomic	0	0	0	0	0	0
Global Atomic Cas					0	0
Surface Atomic	0	0	0	0	0	0
Surface Atomic Cas						
Loads		40,31,489	10.63		12,90,07,648	41,72,52,81,021.37
Stores	2,07,496	0.10	-	-	66,38,872	2,14,75,47,091.70
Total	2,07,496	0.10	40,31,489	10.63	13,56,47,520	43,87,27,48,913.27

Device Memory

	L2<->FB Sectors	% Peak	Bytes	Throughput
Load	1,89,636	0.54	35,08,352	1,13,47,13,309.87
Store	97,626	0.48	21,24,032	1,01,04,11,923.00
Total	2,87,262	1.02	66,32,384	2,14,51,25,232.87

Scheduler Statistics

Active Warps Per Scheduler [warp/cycle]	1.61	Instructions Per Active Issue Slot [inst/issue]	1.00
Eligible Warps Per Scheduler [warp/cycle]	0.05	No Eligible [%]	94.83
Issued Warp Per Scheduler [issue/cycle]	0.05	One or More Eligible [%]	5.21

Warps Per Scheduler

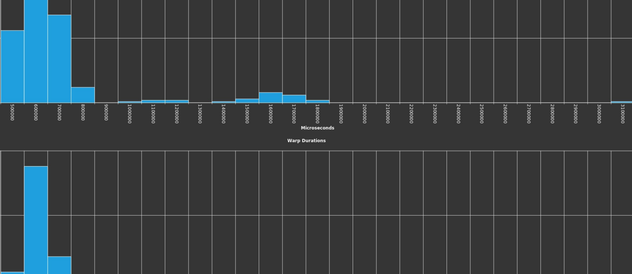
Recommendations

Issue Slot Utilization [Warning] Every scheduler is capable of issuing two instructions per cycle, but for this kernel each scheduler only issues an instruction every 19.2 cycles. This might leave hardware resources underutilized and may lead to less optimal performance. Out of the maximum of 16 warps per scheduler, this kernel allocates an average of 1.61 active warps per scheduler, but only an average of 0.05 warps were eligible per cycle. Eligible warps are the subset of active warps that are ready to issue their next instruction. Every cycle with no eligible warp results in no instruction being issued and the issue slot remains unused. To increase the number of eligible warps either increase the number of active warps or reduce the time the active warps are stalled.

Warp State Statistics

Warp Cycles Per Issued Instruction [cycle/inst]	28.68	Avg. Active Threads Per Warp [thread/inst]	26.33
Warp Cycles Per Issue Active [cycle/issue]	30.61	Avg. Not Predicated Off Threads Per Warp [thread/inst]	25.36
Warp Cycles Per Executed Instruction [cycle/inst]	28.71		

Warp State (All Cycles)



Recommendations

CPI Stall 'Short Scoreboard' [Warning] On average each warp of this kernel spends 21.0 cycles being stalled waiting for a scoreboard dependency on an MIO operation (not to TEX or L1). This represents about 67.8% of the total average of 30.9 cycles between issuing two instructions. The primary reason for a high number of stalls due to short scoreboards is typically memory operations to shared memory, but other contributors include frequent execution of special math instructions (e.g. MUFU) or dynamic branching (e.g. BRX, JMX). Consult the Memory Workload Analysis section to verify if there are shared memory operations and reduce bank conflicts, if reported.

CPI Stall 'Barrier'	Warp stall analysis for 'Barrier' issues	Apply
CPI Stall 'Dispatch Stall'	Warp stall analysis for 'Dispatch Stall' issues	Apply
CPI Stall 'Drain'	Warp stall analysis for 'Drain' issues	Apply
CPI Stall 'IMC Miss'	Warp stall analysis for 'Immediate constant cache (IMC)' issues	Apply
CPI Stall 'LG Throttle'	Warp stall analysis for 'LG Throttle' issues	Apply
CPI Stall 'Long Scoreboard'	Warp stall analysis for 'Long Scoreboard' issues	Apply
CPI Stall 'Math Pipe Throttle'	Warp stall analysis for 'Math Pipe Throttle' issues	Apply
CPI Stall 'Membar'	Warp stall analysis for 'Membar' issues	Apply
CPI Stall 'MIO Throttle'	Warp stall analysis for 'MIO Throttle' issues	Apply
CPI Stall 'Misc'	Warp stall analysis for 'Misc' issues	Apply
CPI Stall 'No Instructions'	Warp stall analysis for 'No Instructions' issues	Apply
CPI Stall 'Not Selected'	Warp stall analysis for 'Not Selected' issues	Apply
CPI Stall 'Sleeping'	Warp stall analysis for 'Sleeping' issues	Apply
CPI Stall 'TEX Throttle'	Warp stall analysis for 'TEX Throttle' issues	Apply
CPI Stall 'Wait'	Warp stall analysis for 'Wait' issues	Apply
Thread Divergence	Warp and thread control flow analysis	Apply

Instruction Statistics

Executed Instructions [inst]	60,34,680	Avg. Executed Instructions Per Scheduler [inst]	1,93,665.70
Issued Instructions [inst]	66,41,280	Avg. Issued Instructions Per Scheduler [inst]	1,91,768.75

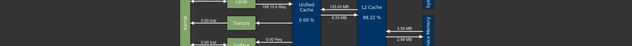
Executed Instruction Mix

Launch Statistics

Grid Size	300	Registers Per Thread [register/thread]	255
Block Size	32	Static Shared Memory Per Block [byte/block]	0
Threads [thread]	9,600	Dynamic Shared Memory Per Block [byte/block]	0
Waves Per SM	2.34	Shared Memory Configuration Size [Kbyte]	48

Block Durations

Warp Durations



Recommendations

Launch Configuration Kernel launch configuration analysis | Apply

Occupancy

Theoretical Occupancy [%]	12.50	Block Limit Registers [register]	8
Theoretical Active Warps per SM [warp/cycle]	4	Block Limit Local Mem [byte]	non
Achieved Occupancy [%]	9.50	Block Limit Warps [warp]	64
Achieved Active Warps Per SM [warp/cycle]	6.20	Block Limit SM [block]	32

Impact of Varying Register Count Per Thread

Impact of Varying Block Size

Impact of Varying Shared Memory Usage Per Block