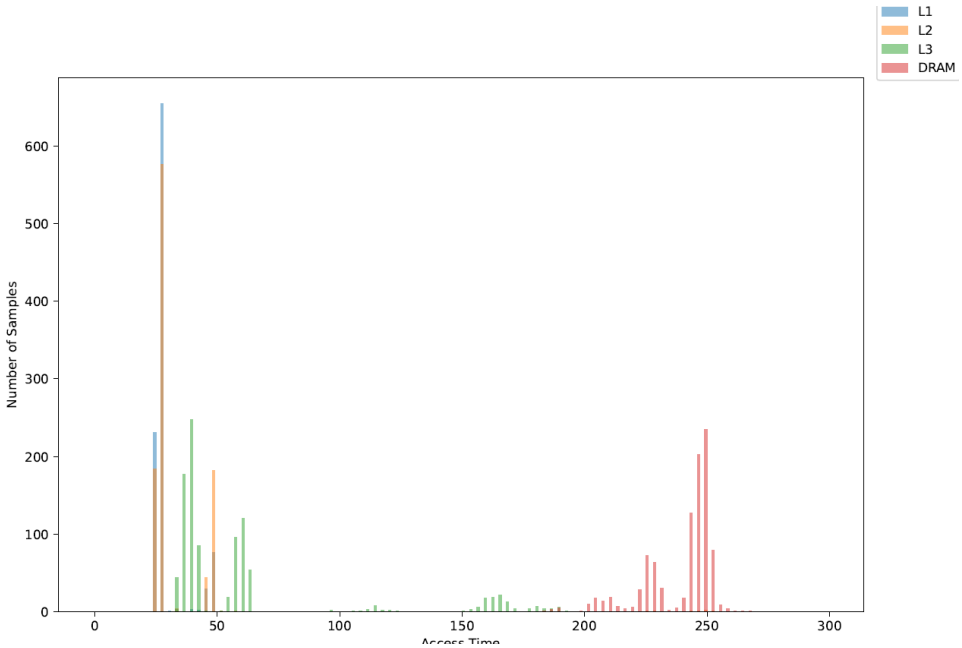
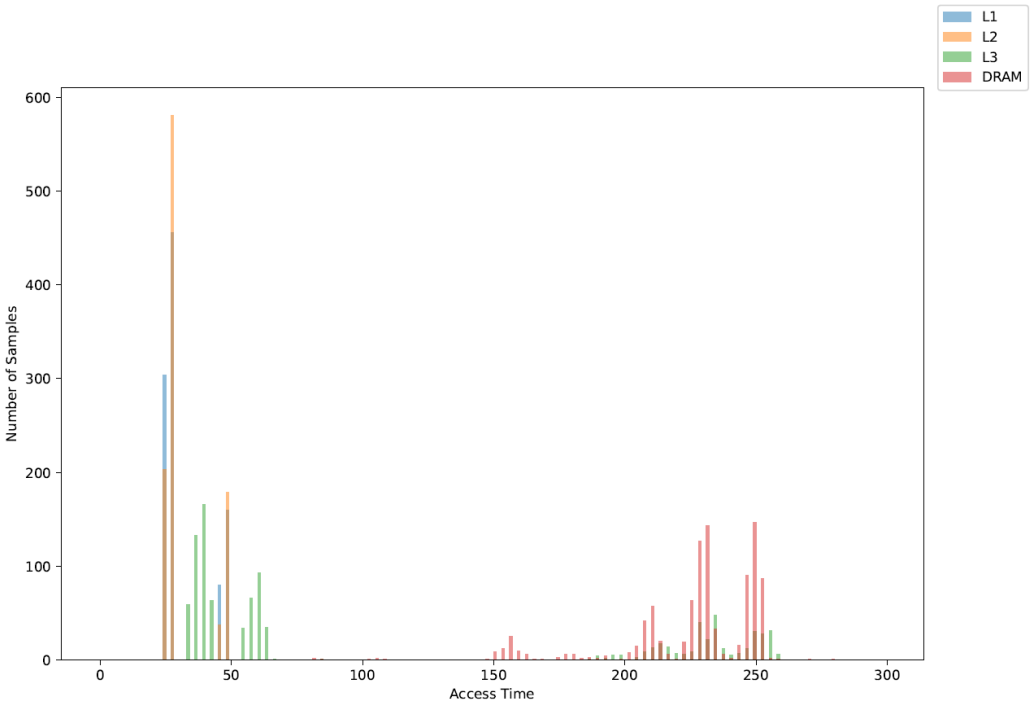
Securing Processor Architectures LAB 1

Reference histogram



Run histogram



Discussion Question 4 (Optional): Describe your communication protocol to communicate a single bit value.

For the communication protocol the sender and receiver use a 2MB buffer to ensure that the VA->PA mapping doesn't interfere with the set index. Reciever sets up 16 writes with bits 14:6 as zero to ensure that 8 addresses sit in L1 set 0 and 8 in L2 set 0. When the sender sees bit 0 is a 1 it writes into set 0 thereby evicting one of the receiver addresses to L3 set 0. The receiver will then probe the addresses it primed and if it sees an L3 delay (~55-60) cycles then it knows that the sender receiver bit 0 is 1 else it's 0.

Discussion Question 6: Describe your communication protocol. Please refer to Section 2.2 for the components involved in a protocol.

The same protocol from above extends to an 8 bit case where now the receiver primes 16 addresses into set0-set7 which is basically the base addresses of the 2MB buffer+0x40 increments to move to the next set. The sender will write to addresses which will map to set0-7 based on whether those bits are1. The receiver then probes the 8 sets and if it sees an L3 delay for one of the 16 addresses it had primed then it knows that corresponding bit is set.

Discussion Question 5 (Optional): Given a 64-bit virtual address, fill in the table below. The table is intended to help you to figure out how to find addresses that map to the same L2 cache set.

Page Size	4KB	2MB
Page Offset Bits	12	21
Page Number Bits	52	43
L2 Set Index Bits	9	9
L2 Set Index Fully Under Control?	No	Yes

Table 2: Address calculation.