NATIONAL INSTITUTE OF TECHNOLOGY JAMSHEDPUR

Department of Electronics and Communication Engineering

Mid Semester Examination, October 2024

B.Tech. (2nd Year): 3rd Semester Branch: Electronics and Communication Engineering

Course Name: Digital Circuits and System Design Course Code: EC1304

Date of Exam: 07.10.2024 Duration: 02 Hours Max. Marks: 30

Name of Faculty: Dr. Rashmi Sinha

Note:

i. All questions are compulsory.

ii. Assume any suitable missing data, if any.

1. a. Subtract $(1110.011)_2$ from $(11011.11)_2$ using basic rules of binary subtraction and verify the result by showing equivalent decimal subtraction. 5X1

   b. Perform the following addition operation

   $(AF1.B3)_{16} + (FFF.E)_{16}$

   c. Find out whether 16 bit 2's complement arithmetic can be used to add 14,276 and 18,490.

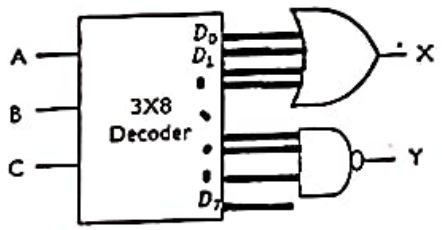
   d. The 7's complement of a certain Octal number is 5264. Determine the binary and Hexadecimal equivalent of that Octal number.

   e. How many Ex-OR gates are required to convert 8-bit binary to Gray code?

2. a. Design a logic circuit having 3 inputs A, B, and C such that output is 1, when A=0 or whenever B=C=1. Implement the logic circuit using minimum no. of NOR gates. (Reduce using Boolean Algebra) [3]

   b. Construct a K map for the function, $f = AB + A\bar{C} + C + AD + A\bar{B}CD$. How many implicants are there? Categorize. Minimize the expression and realize using minimum number of NAND gates only. [3]

3. a. What is the function implemented by the given 3 to 8 Decoder? [3]



b. Implement a 4:16 DECODER using 2:4 DECODER with the help of ENABLE input. [3]

c. Design a 4:2 Priority Encoder. [3]

4. Design a 4-bit Adder/ Subtractor circuit that can perform both addition and subtraction using IC7483 and SSI gate (if required). It must have the provision to indicate whether the result is positive or negative. Show and explain each step briefly. [4]

5. (i) Implement the Boolean function $f = \prod M(0,1,4,7)$ using [4]

   a. 4:1 MUX

   b. 8:1 MUX

   (ii) Implement a Half Subtractor (HS) using Demultiplexer [2]

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END SEMESTER EXAMINATION, DECEMBER 2024

B.Tech. (2nd Year): 3rd Semester Branch: Electronics and Communication Engineering

Course Name: **Digital Circuits and System Design** Course Code: **EC1304**

Duration: 03 Hours Max. Marks: 50 Name of Faculty: Dr. Rashmi Sinha

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Note:

i. **All questions are compulsory and all parts of a question should be written at one place.**
ii. **Assume any suitable missing data, if any.**

1 a. What will be the sequence of a counter which consists of 3 flip-flops where external clock pulse is given to the first flip-flop and the output 'Q' of each flip-flop is given to the clock pulse of next one. All flip-flops are positive edge triggered. [6]

b. Convert: Hexa-decimal value 16 to decimal

c. State the condition when XOR and XNOR gate degenerates into NOT gate.

d. Subtract using 2's compliment arithmetic: $(29.A)_{16}$ from $(4F.B)_{16}$

e. The content of a 4-bit register is initially 1101. The register is shifted six times to the left with the serial input being 101101. What is the new content of the register?

f. Simplify: $[1 + LM + L\bar{M} + \bar{L}M][(L + \bar{M}).(\bar{L}.M) + \bar{L}\bar{M}.(L + M)]$

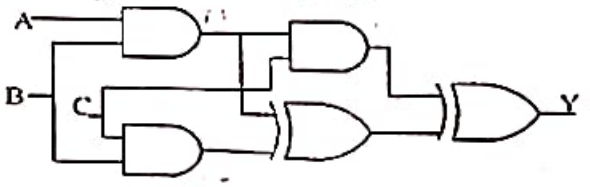
2 a. Design a combinational circuit (AND and NOT gates) with two inputs which produces output as logic 0 when only one input is 1. Use k map to design. [12]

b. Convert the function $f(A,B,C) = A(A + \bar{C})$ to canonical POS form.

c. Minimize the given switching function using K map: $G = \sum m(3,4,5,7,9,13,14,15)$ and mention PI's and EPI's.

d. Design a 32:1 MUX using two 16:1 MUX.

e. Find the output of the given combinational circuit



f. A ripple counter has 5 flip-flops of 10 nsec time delay each, then determine
   (i) Modulus of counter
   (ii) Output frequency when clock frequency is 16 MHz
   (iii) Total time delay of counter
   (iv) Maximum allowed clock frequency

3 a. Implement a Full Adder using Decoder Circuit. 5X4

b. Design a 4-bit shift register which can perform following functions [20]
   (i) Left Shift
   (ii) Right Shift
   (iii) Serial data transfer
   (iv) Parallel data transfer

c. Consider a JK' FF i.e a JK FF with an Inverter between external inputs K' and internal input K.
   (i) Obtain the FF characteristics table
   (ii) Obtain the characteristics equation

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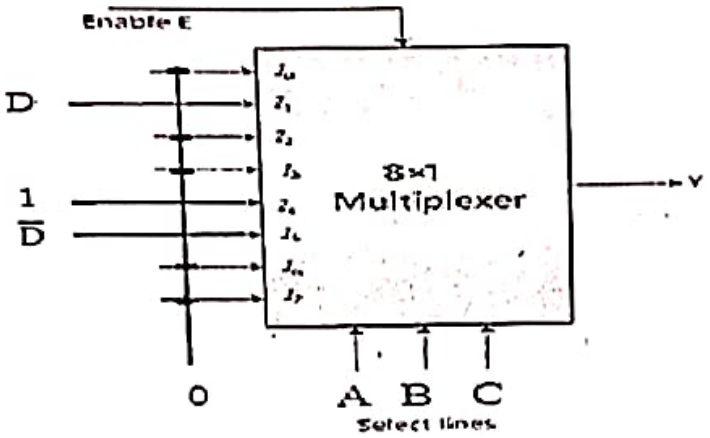
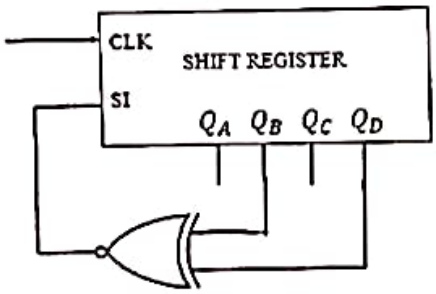
(iii) Obtain the excitation table

d. Design a synchronous counter to count the sequence 2,5,6,2,5,6,2..... with the help of positive edge triggered D flipflop.

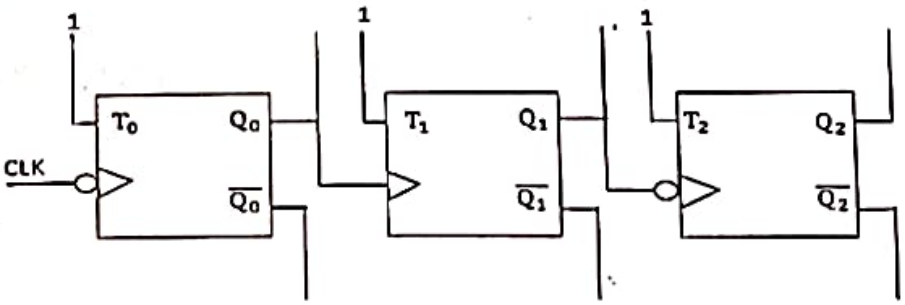
4. a. Derive the switching function implemented by the given multiplexer in terms of both Maxterm and Minterm representation. 4X3 [12]



b. A 4 bit SIPO shift register is used with a feedback as shown in the figure below. The shifting sequence is $Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$. If all flip flops are in reset state initially, after how many clock pulses the output will be repeated?



c. In the following ripple counter, obtain the clock sequence when output is taken from (i) Q_0, Q_1, Q_2 (ii) $\overline{Q_0}$, $\overline{Q_1}$, $\overline{Q_2}$



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