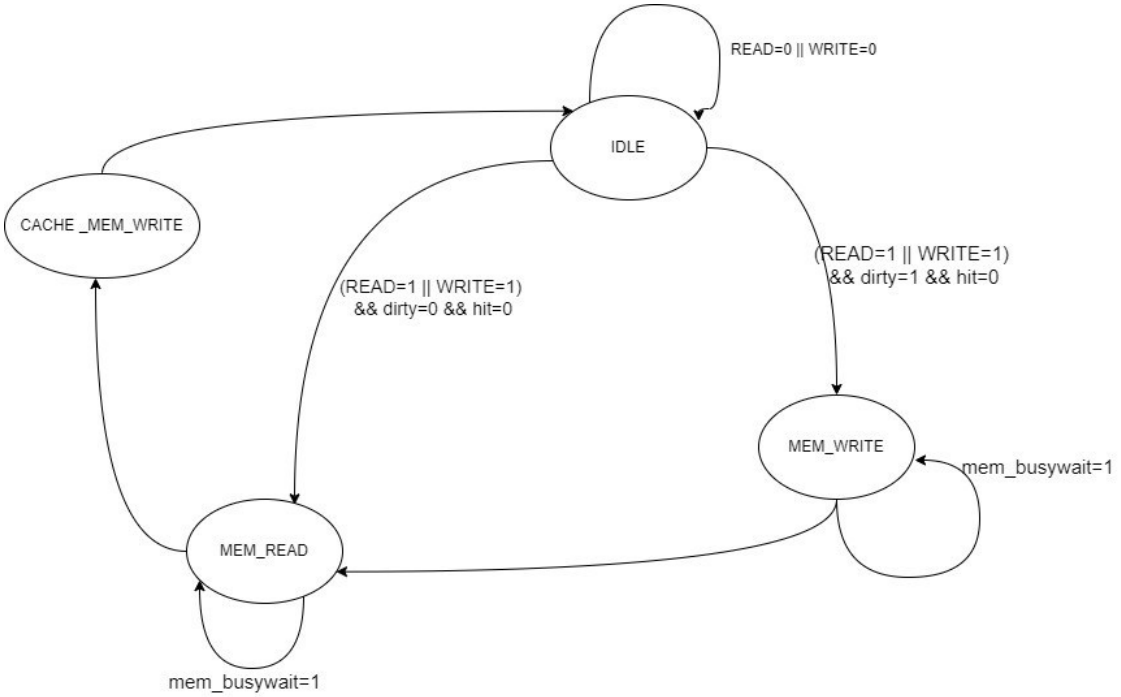
Lab 6 Part2

Group 26 (E/18/017 E/18/245)

Finite State Machine



Write hit

Without cache	With cache
Data memory is stalled. Only memory reading/writing should be done.	Data Memory access should not happen. PC should not stall. Therefore, data access happens much quicker than the instance without the cache.

Read miss

Without cache	With cache
Data memory is stalled. Reading/Writing in the data memory is done.	Data memory should be stalled. But the time taken should be more than the instance without the cache.

Write Miss

Without cache	With cache
Data memory is stalled. Reading/Writing in the data memory is done	Data memory should be stalled. But the time taken should be more than the instance without the cache.

Used Sample Program

loadi 0 0x09
loadi 1 0x01
swd 0 1
swi 1 0x00
lwd 2 1
lwd 3 1
sub 4 0 1
swi 4 0x02
lwi 5 0x02
swi 4 0x20
lwi 6 0x20

Output without Cache memory

```
PS C:\Users\Futuremind\OneDrive\Desktop\Lab6_Part1\group26_lab6_part1> iverilog -o cpu.vvp cpu_tb0.v cpu_0.v
PS C:\Users\Futuremind\OneDrive\Desktop\Lab6_Part1\group26_lab6_part1> vvp cpu.vvp
WARNING: cpu_tb0.v:53: $readmemb(instr_mem.mem): Not enough words in the file for the requested range [0:1023
VCD info: dumpfile cpu_wavedata.vcd opened for output.
                  0 REG0:   x  REG1:   x  REG2:   x  REG3:   x  REG4:   x  REG5:   x  REG6:   x  REG7:   x
                  5 REG0:   0  REG1:   0  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                 13 REG0:   9  REG1:   0  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                 21 REG0:   9  REG1:   1  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                125 REG0:   9  REG1:   1  REG2:   9  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                133 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                141 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   0  REG6:   0  REG7:   0
                237 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   8  REG6:   0  REG7:   0
                333 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   8  REG6:   8  REG7:   0
cpu_tb0.v:84: $finish called at 5060 (100ps)
PS C:\Users\Futuremind\OneDrive\Desktop\Lab6_Part1\group26_lab6_part1>
```

Output with Cache memory

```
PS C:\Users\Futuremind\OneDrive\Desktop\Lab6_Part1\group26_lab6_part2> iverilog -o cpu.vvp cpu_tb0.v
PS C:\Users\Futuremind\OneDrive\Desktop\Lab6_Part1\group26_lab6_part2> vvp cpu.vvp
WARNING: cpu_tb0.v:65: $readmemb(instr_mem.mem): Not enough words in the file for the requested range [0:1023].
VCD info: dumpfile cpu_wavedata.vcd opened for output.
                  0 REG0:   x  REG1:   x  REG2:   x  REG3:   x  REG4:   x  REG5:   x  REG6:   x  REG7:   x
                  5 REG0:   0  REG1:   0  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                 13 REG0:   9  REG1:   0  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                 21 REG0:   9  REG1:   1  REG2:   0  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                221 REG0:   9  REG1:   1  REG2:   9  REG3:   0  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                229 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   0  REG5:   0  REG6:   0  REG7:   0
                237 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   0  REG6:   0  REG7:   0
                253 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   8  REG6:   0  REG7:   0
                613 REG0:   9  REG1:   1  REG2:   9  REG3:   9  REG4:   8  REG5:   8  REG6:   8  REG7:   0
cpu_tb0.v:99: $finish called at 1005000 (1ps)
```

Wave data without Cache memory

Wave data with Cache memory