Lab 3

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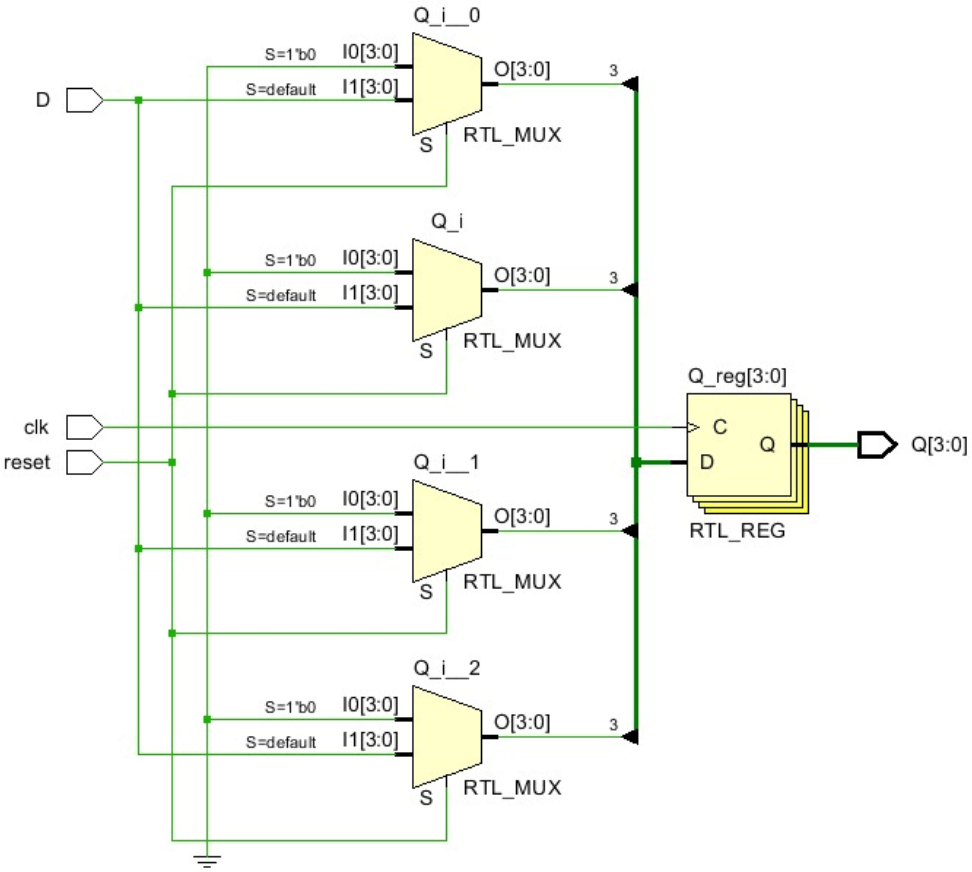
Code for blocking:

```
`timescale 1ns / 1ps


module shiftregister(input D,
input clk,
input reset,
output reg [3:0]Q);


always @ (posedge clk, negedge reset)
begin
    if (!reset)
    Q=4'b0;
    else
    Q[3]=D;
    Q[2]=Q[3];
    Q[1]=Q[2];
    Q[0]=Q[1];
 end
endmodule
```

Schematic for blocking:

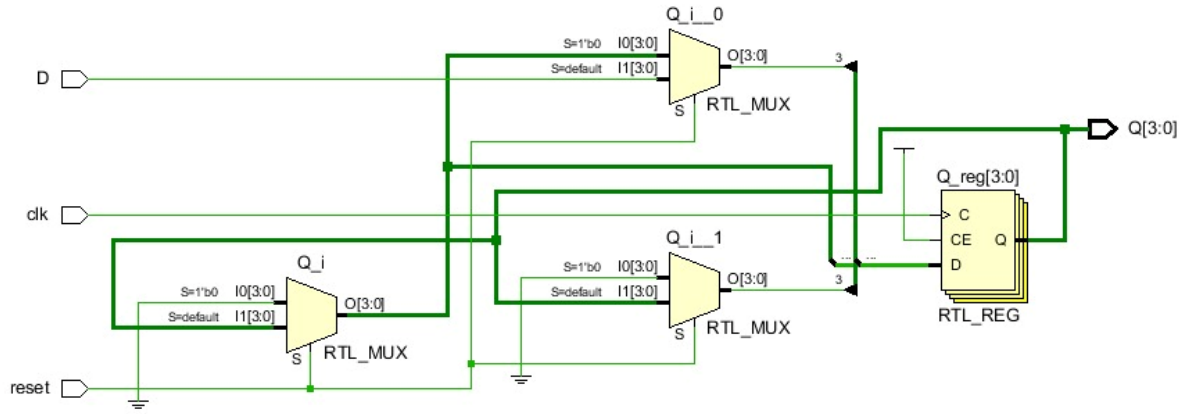


Simulation for blocking:

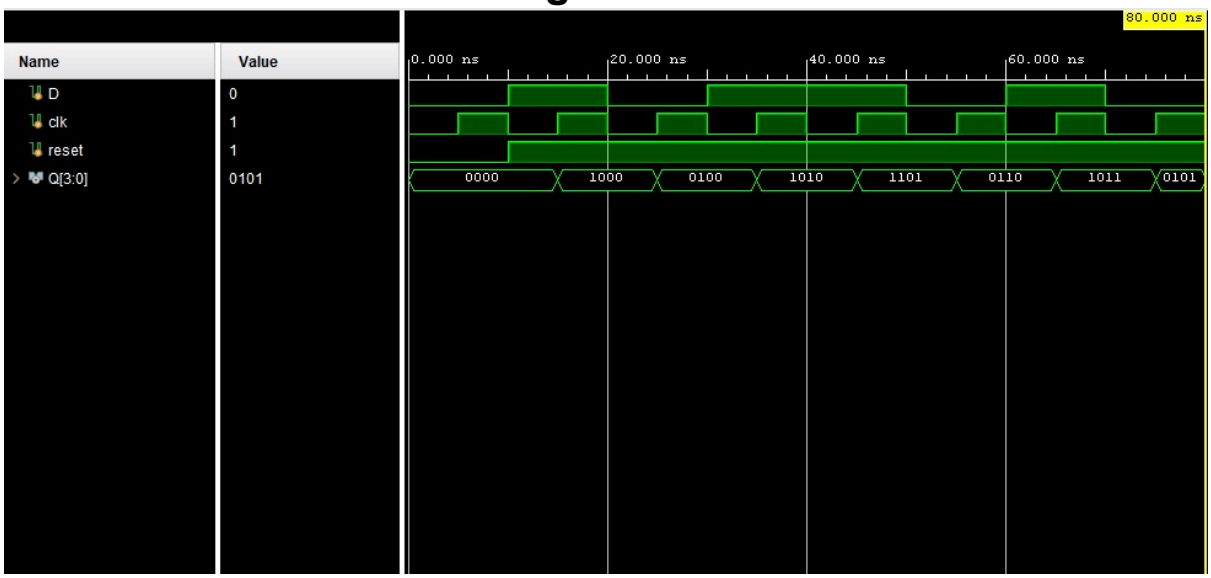
Code for non-blocking:

```
`timescale 1ns / 1ps

module shiftregister(input D,
input clk,
input reset,
output reg [3:0]Q);

always @ (posedge clk, negedge reset)
begin
    if (!reset)
    Q=4'b0;
    else
    Q[3]<=D;
    Q[2]<=Q[3];
    Q[1]<=Q[2];
    Q[0]<=Q[1];
 end
endmodule
```

Schematic for non-blocking:



Simulation for non-blocking:



Testbench for both are the same:

```
`timescale 1ns / 1ps


module shiftregister_tb();
reg D;
reg clk;
reg reset;
wire [3:0]Q;
shiftregister uut(D,clk,reset,Q);
initial
begin
clk=0;
    forever #5 clk=~clk;
end
initial
begin
reset=0;
D=1'b0;
#10;
reset=1;
D=1'b1;
#10;
D=1'b0;
#10;
D=1'b1;
#10;
D=1'b1;
#10;
D=1'b0;
#10;
```

```
D=1'b1;
#10;
D=1'b0;
#10;
$finish;
end
endmodule
```