Lab 4

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Code for toggle:

```
`timescale 1ns / 1ps


module toggle ( input clk, input rst, input t, output reg q);


  always @ (posedge clk or negedge rst)
  begin


       if (!rst)
         q <= 0;
       else
          if (t)
             q <= ~q;
          else
             q <= q;
     end
endmodule
```

Code for counter:

```
`timescale 1ns / 1ps


module asynch(
input clk,
input wire rst,
input t,
output [3:0]q);
```

```
toggle a1(.clk(clk),.rst(rst),.t(t),.q(q[0]));
toggle a2(.clk(~q[0]),.rst(rst),.t(t),.q(q[1]));
toggle a3(.clk(~q[1]),.rst(rst),.t(t),.q(q[2]));
toggle a4(.clk(~q[2]),.rst(rst),.t(t),.q(q[3]));

endmodule
```

Testbench :

```
`timescale 1ns / 1ps

module asynch_up_tb();

reg t;
reg rst;
reg clk;
wire [3:0]q;
asynch uut(clk,rst,t,q);

initial
begin
clk=0;
   forever #5 clk=~clk;
end

initial
begin
t=1;
rst=0;
```

```
clk=1;
#5;
rst=1;
#107;
rst=0;
t=1;
#150;
$finish();
end
endmodule
```

Simulation: