Lab – 7
Mumuksh Jain – 22110160
Nishant Kumar – 22110170

Code:

```
`timescale 1ns / 1ps
module hazards(
input A,
input B,
input C,
output f);
or #5 g1(o1,A,B);
not #5 G1(n1,A);
or #5 g2(o2,n1,C);
and #5 g3(o3,o1,o2);
not #5 G2(n2,B);
and #5 g4(o4,A,n2);
or #5 g5(f,o3,o4);

//or g1(o1,A,B);
//not G1(n1,A);
//or g2(o2,n1,C);
//and g3(o3,o1,o2);
//not G2(n2,B);
//and g4(o4,A,n2);
//or g5(f,o3,o4);
endmodule
```

Commented out code gives outputs without delay, showing the output without any hazard, and the other lines give outputs with delays and show a static hazard.

If want to see intermediate signal as we showed for static hazard, write input o3,o4 in the module definition and similar in testbench too.

Testbench:

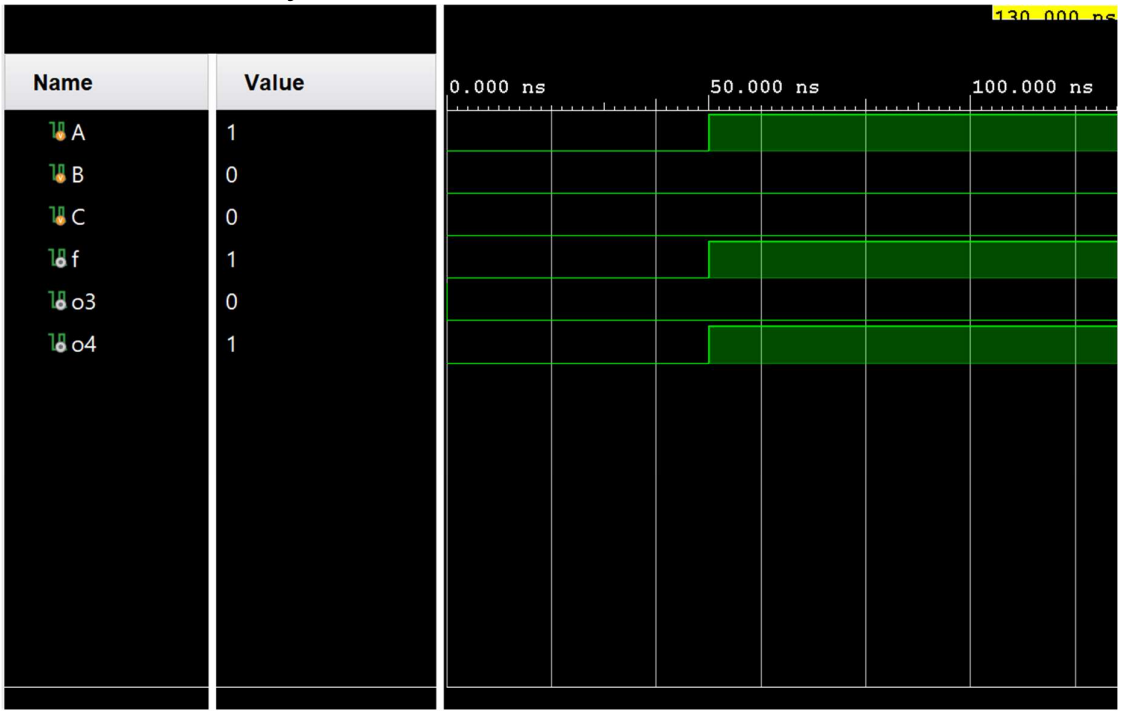
```
`timescale 1ns / 1ps

module hazards_tb();
reg A;
reg B;
reg C;
wire f;

hazards uut(A,B,C,f);
initial
begin

A=0;
B=0;
C=0;
#50;
A=1;
B=0;
C=0;
#80;


$finish();
end
endmodule
```

We can see static hazard in output o3 from the gate g3.

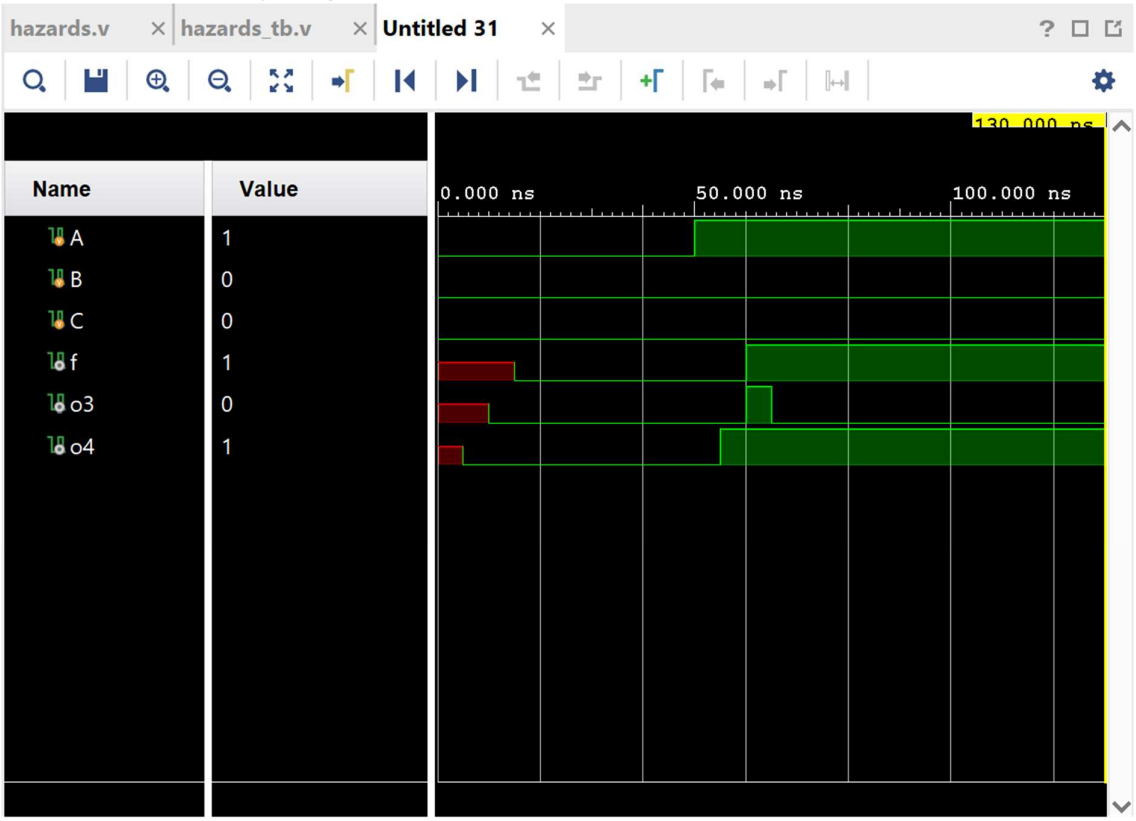
This is static 0 hazard

Simulation:

Without Gate Delay:



When Gate Delay is given, Static Hazard is seen:



Dynamic Hazard:

Code:

```
`timescale 1ns / 1ps

module hazards(
input A,
input B,
input C,
output f);

or #5 g1(o1,A,B);
not G1(n1,A);
or #8 g2(o2,n1,C);
and g3(o3,o1,o2);
not G2(n2,B);
and #11 g4(o4,A,n2);
or g5(f,o3,o4);

//or g1(o1,A,B);
//not G1(n1,A);
//or g2(o2,n1,C);
//and g3(o3,o1,o2);
//not G2(n2,B);
//and g4(o4,A,n2);
//or g5(f,o3,o4);

endmodule
```

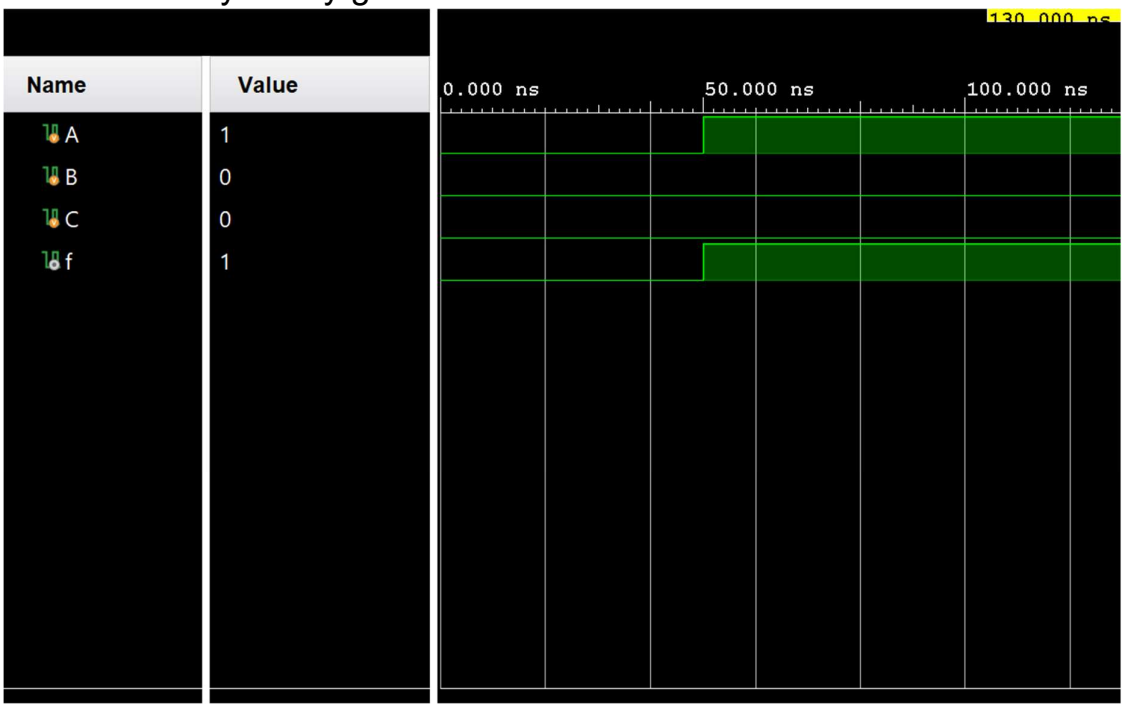
The difference here is that we realise that we cannot see a dynamic hazard if we keep the same delay in every gate and thus, we changed the delay in each gate(also removed delays in some gates)

Testbench:

```
`timescale 1ns / 1ps

module hazards_tb();
reg A;
reg B;
reg C;
wire f;

hazards uut(A,B,C,f);
initial
begin

A=0;
B=0;
C=0;
#50;
A=1;
B=0;
C=0;
#80;

//A=0;
//B=1;
//C=1;
//#50;
//A=1;
//B=1;
//C=1;
//#80;

$finish();
end
endmodule
```

Simulation:

When no delay in any gate:



Dynamic Hazard: