Lab 6

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Code:

```
`timescale 1ns / 1ps

module clock_divider(
input main_clk,
output slow_clk
);
reg [31:0] counter;
always@ (posedge main_clk)
begin
   counter <=counter+1;
end
assign slow_clk=counter[27];
endmodule



module counter(input sel1,sel2, output reg [3:0]Q, input clk1, input rst);

wire slowclk;

clock_divider inst((clk1),(clk));



always @(posedge clk)
   if (!rst)
      Q=4'b0000;
   else if (~sel1&~sel2)
```

```
    Q=Q+1;
  else if(sel1&~sel2)
    Q=Q-1;
  else if(~sel1&sel2)
    begin
    if (Q==4'b1001)
      Q=4'b0000;
    else
    Q=Q+1;
    end
  else if(sel1&sel2)
    begin
    if(Q==4'b0000)
    Q=4'b1001;
    else
    Q=Q-1;
    end


endmodule
```

Testbench:

```
`timescale 1ns / 1ps



module counter_tb();
reg clk;
reg rst;
reg sel1,sel2;
wire [3:0]Q;
```

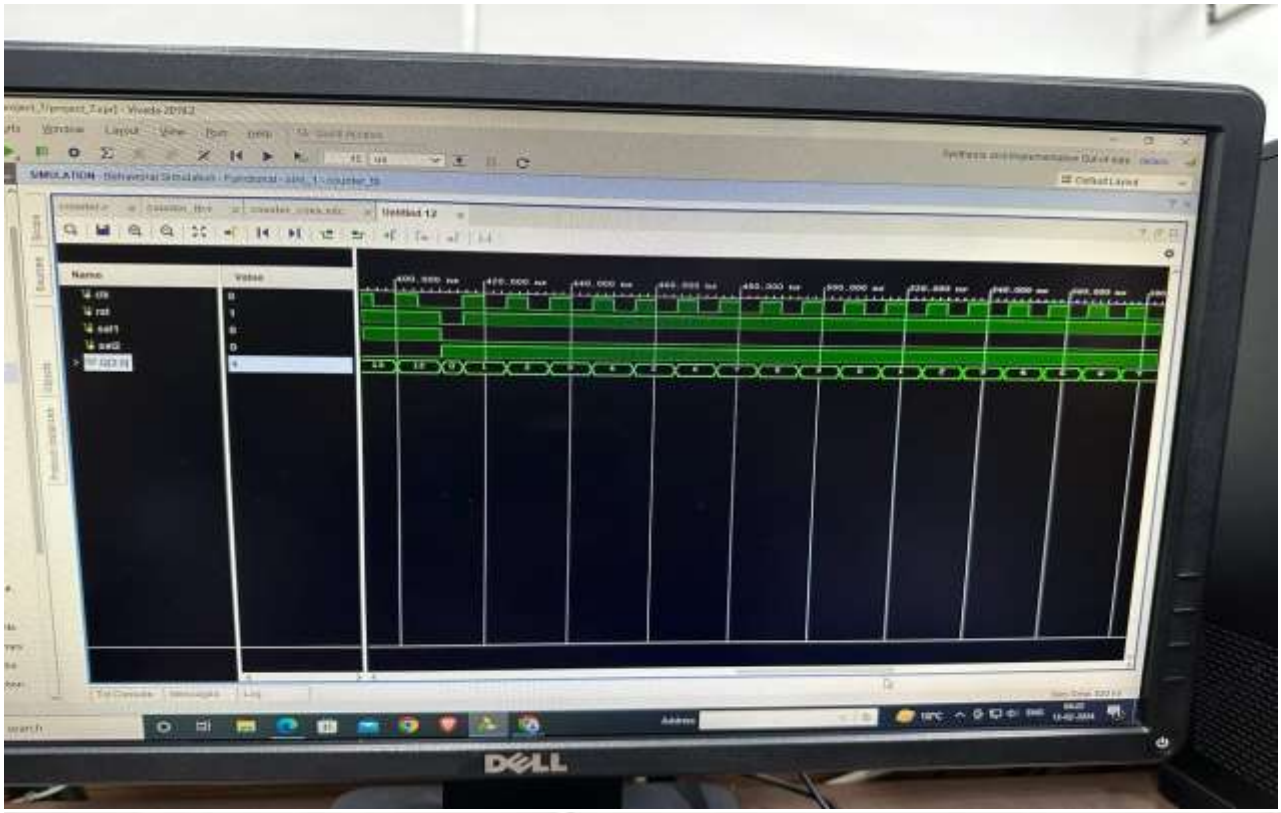
```
counter uut(sel1,sel2,Q,clk,rst);



initial
begin
clk=0;
forever #5 clk=~clk;
end

initial
begin
rst=0;
sel1=1;
sel2=1;
clk=1;
#5;
rst=1;
#200;
rst=0;
sel1=1;
sel2=0;
clk=1;
#5;
rst=1;
#200;
rst=0;
sel1=0;
sel2=1;
clk=1;
#5;
rst=1;
```

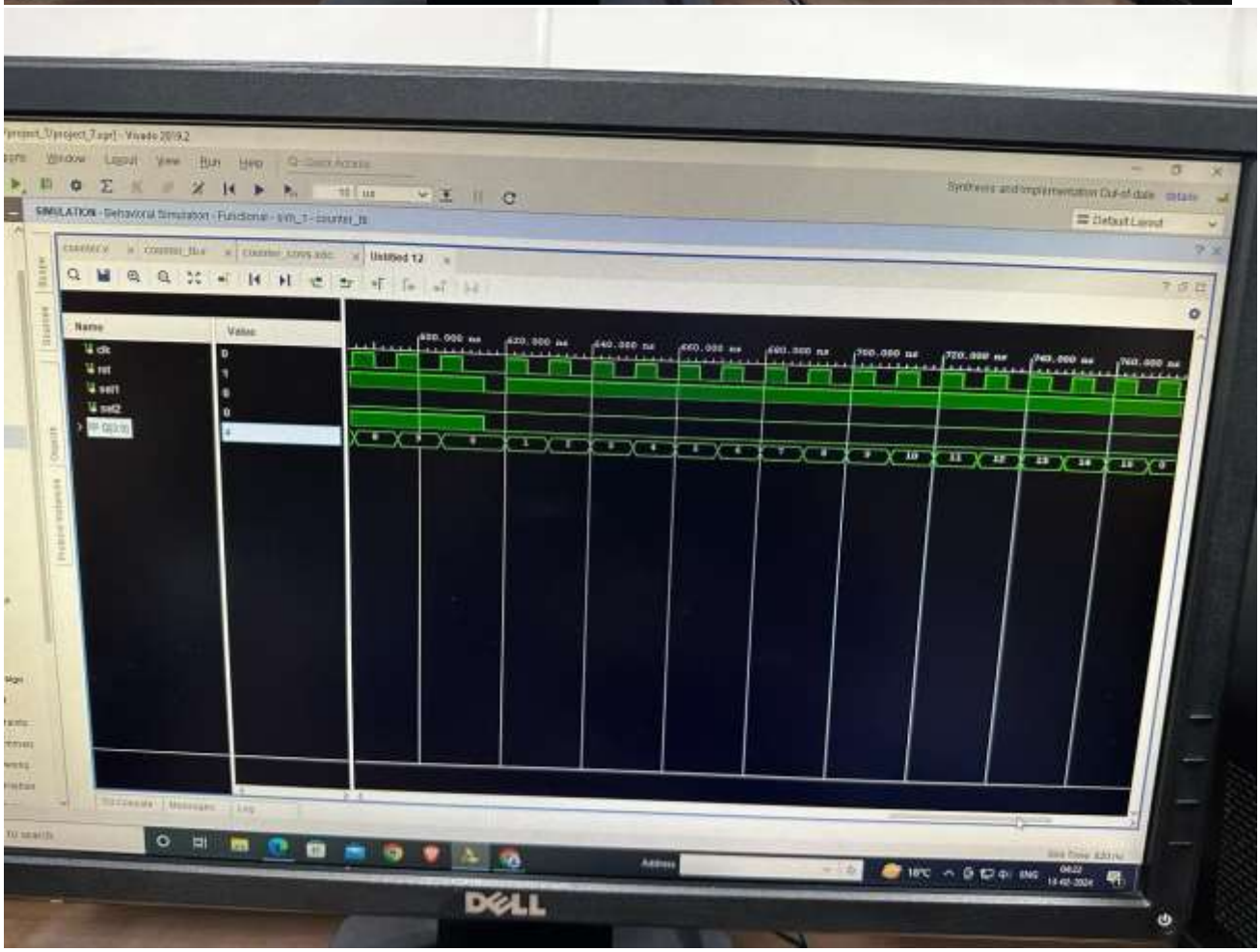
```
#200;
rst=0;
sel1=0;
sel2=0;
clk=1;
#5;
rst=1;
#200;
$finish();
end

endmodule
```

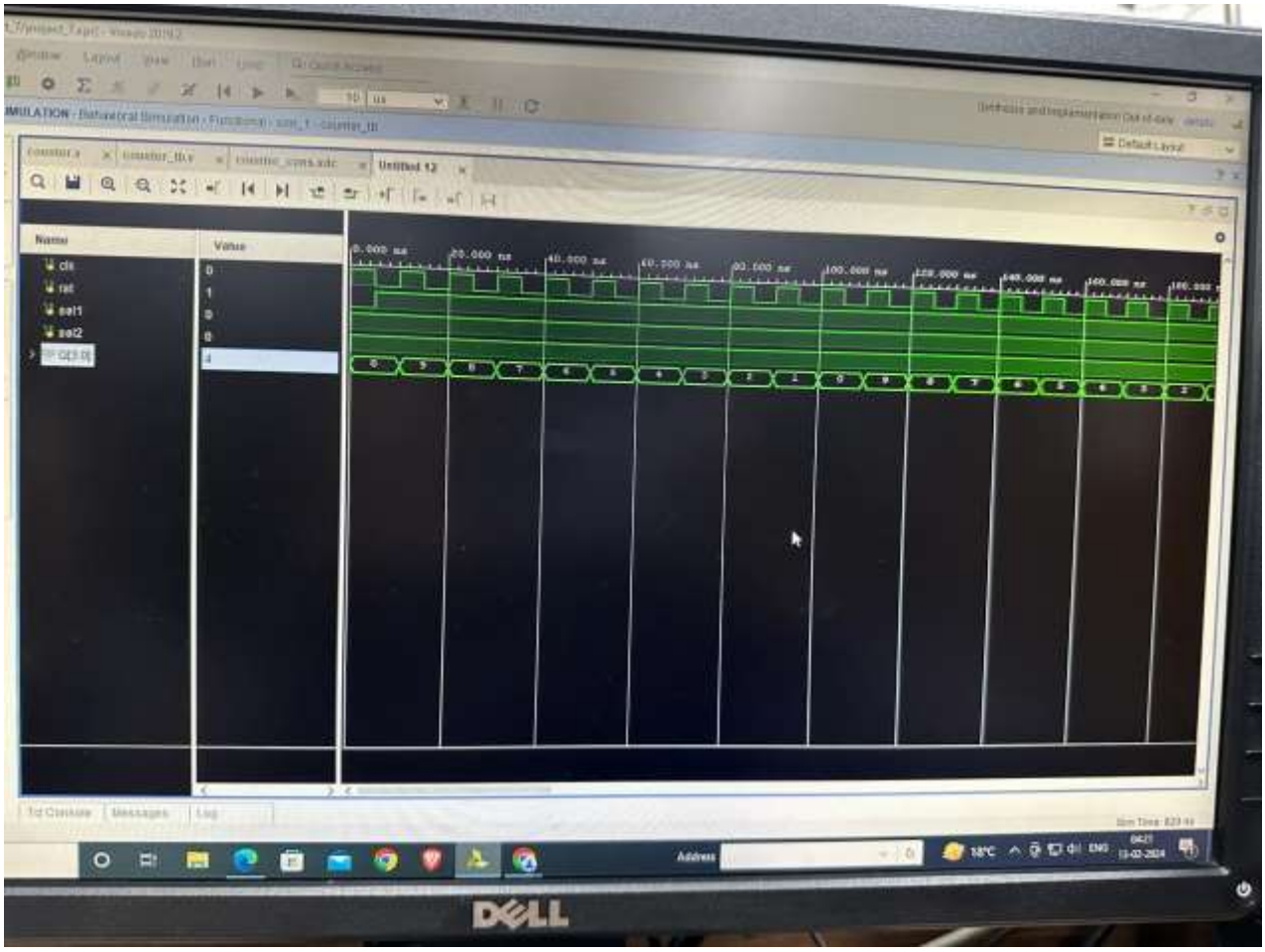
Constraint File:

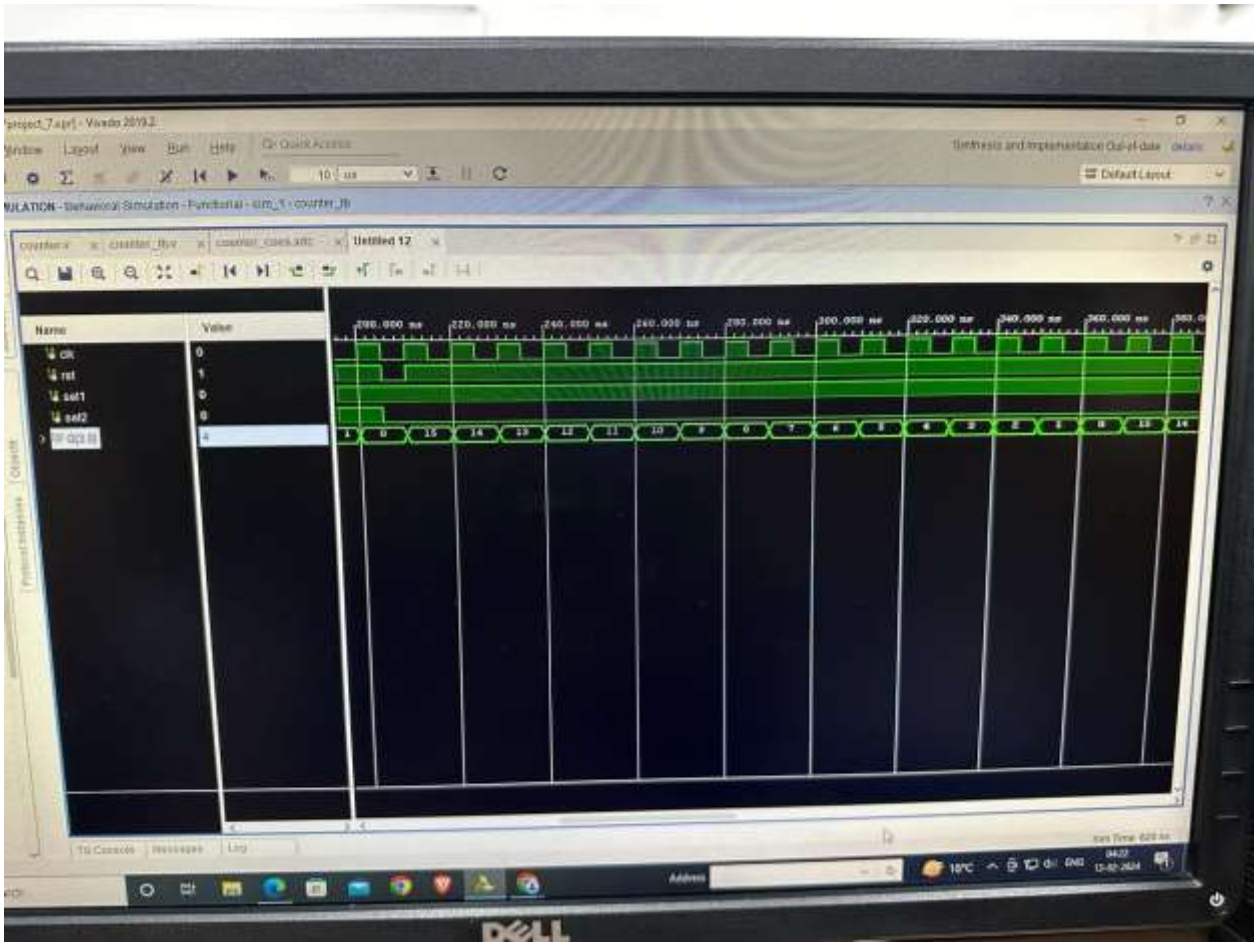
```
set_property IOSTANDARD LVCMOS33 [get_ports main_clk]
set_property IOSTANDARD LVCMOS33 [get_ports mode_select]
set_property IOSTANDARD LVCMOS33 [get_ports reset]
set_property IOSTANDARD LVCMOS33 [get_ports up]
set_property IOSTANDARD LVCMOS33 [get_ports {c[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {c[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {c[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {c[0]}]
set_property PACKAGE_PIN W5 [get_ports main_clk]
set_property PACKAGE_PIN R2 [get_ports mode_select]
set_property PACKAGE_PIN T1 [get_ports reset]
set_property PACKAGE_PIN U1 [get_ports up]
set_property PACKAGE_PIN W2 [get_ports {c[3]}]
set_property PACKAGE_PIN R3 [get_ports {c[2]}]
set_property PACKAGE_PIN T2 [get_ports {c[1]}]
set_property PACKAGE_PIN T3 [get_ports {c[0]}]
```

Simulation:






Name
Value
clk
rst
sel1
sel2
0
1
0
0
4
DELL


Name
Value
clk
rst
sel1
sel2
Untitled 12
Default Layout
DELL