Lab 5

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Code:

```
`timescale 1ns / 1ps
module comparator(
input [3:0]A,
input [3:0]B,
output f
);
assign f=(A==B)?1:0;
endmodule
```

Testbench:

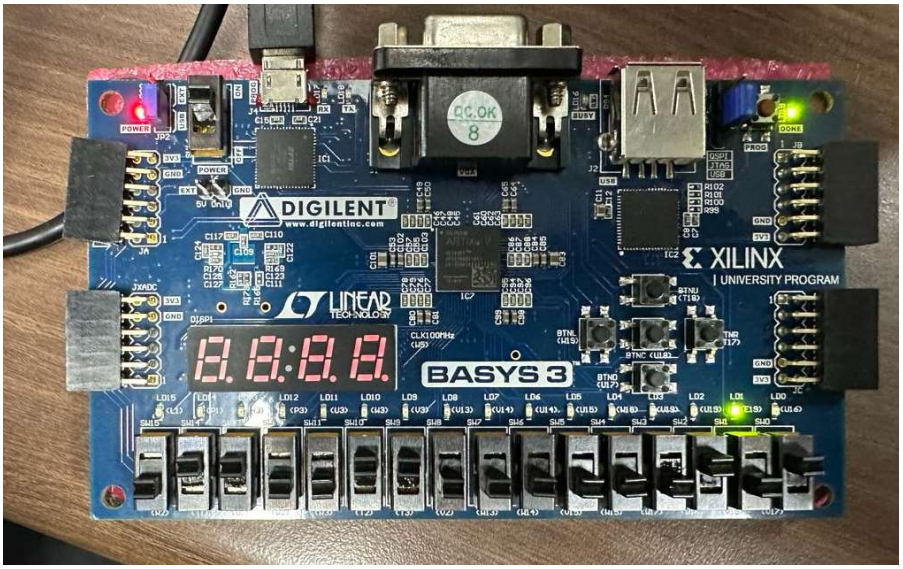
```
`timescale 1ns / 1ps
module comparator_tb();
reg [3:0]A;
reg [3:0]B;
wire f;
comparator uut(A,B,f);
initial
begin
A=4'b0011;
B=4'b0011;
#10;
A=4'b0101;
B=4'b0110;
#10;
A=4'b0111;
```

```
B=4'b1110;
#10;
$finish();
end
endmodule
```

Constraint File:

```
set_property IOSTANDARD LVCMOS33 [get_ports f]
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
set_property PACKAGE_PIN E19 [get_ports f]
set_property PACKAGE_PIN V17 [get_ports {A[3]}]
set_property PACKAGE_PIN T1 [get_ports {A[2]}]
set_property PACKAGE_PIN U1 [get_ports {A[1]}]
set_property PACKAGE_PIN V16 [get_ports {A[0]}]
set_property PACKAGE_PIN W16 [get_ports {B[3]}]
set_property PACKAGE_PIN T2 [get_ports {B[2]}]
set_property PACKAGE_PIN T3 [get_ports {B[1]}]
set_property PACKAGE_PIN V2 [get_ports {B[0]}]
```

Photos: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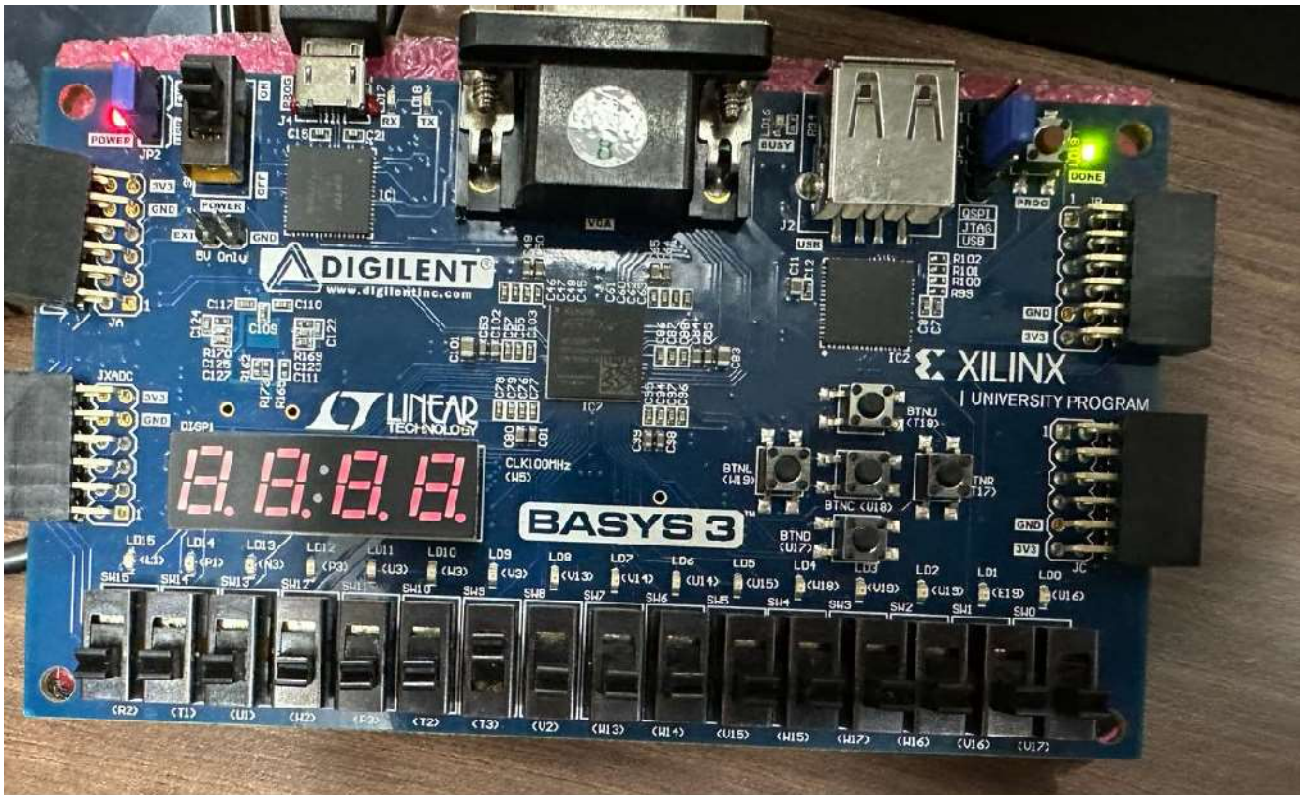
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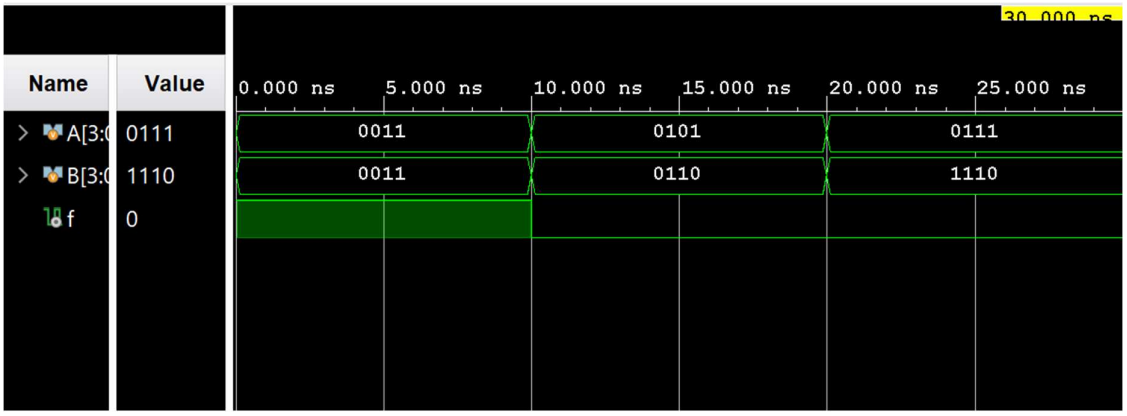
Simulation:


Name
Value
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
A[3:
0111
0011
0101
0111
B[3:
1110
0011
0110
1110
f
0