3 bit Gray to Binary Converter

Group Number: 8

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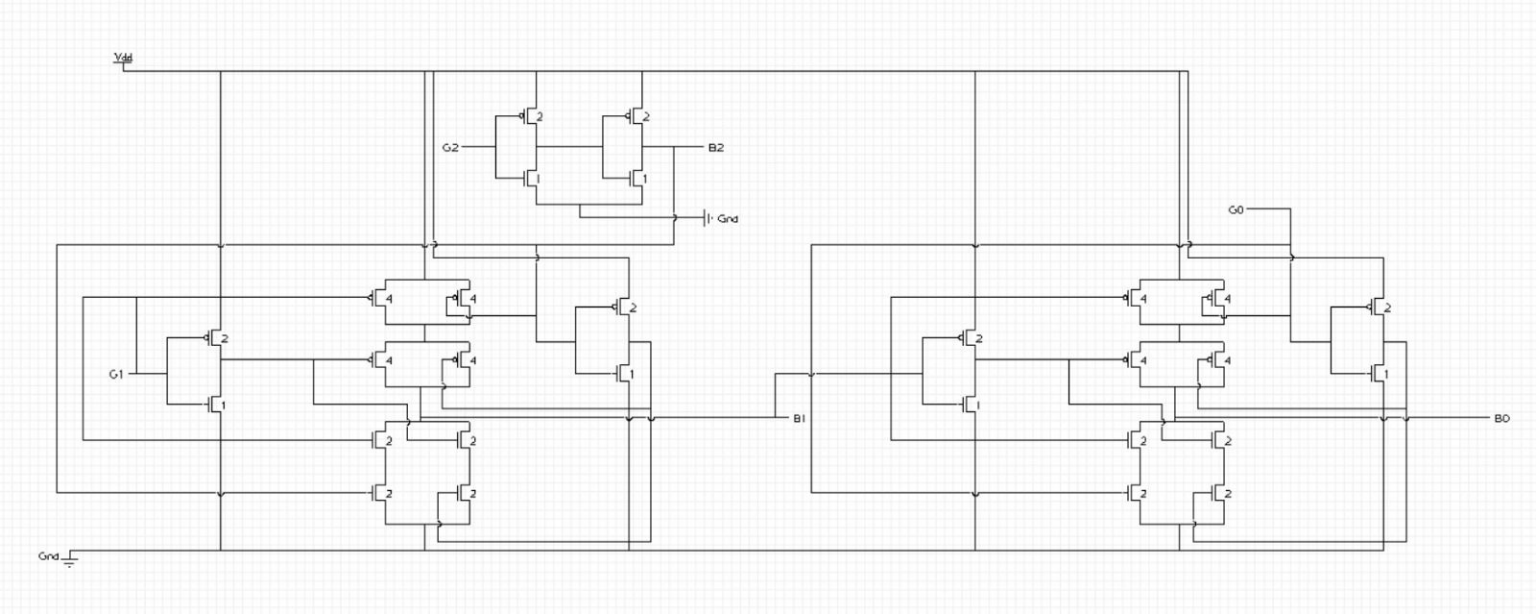
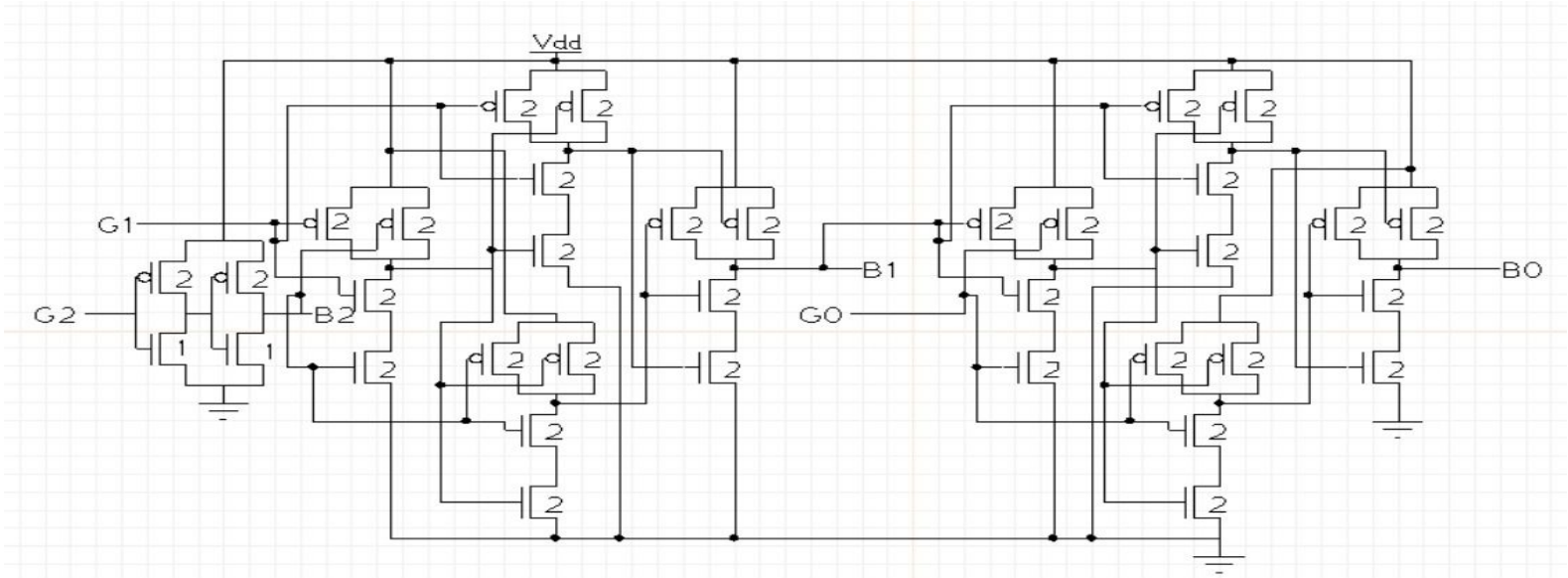
Schematic + Sizing



Circuit using Xor logic
PMOS - 4*0.135 = 0.540um
NMOS - 2*0.135 = 0.270 um

Unit Inverter
PMOS - 2*0.135 = 0.270um
NMOS - 1*0.135um

Schematic + Sizing

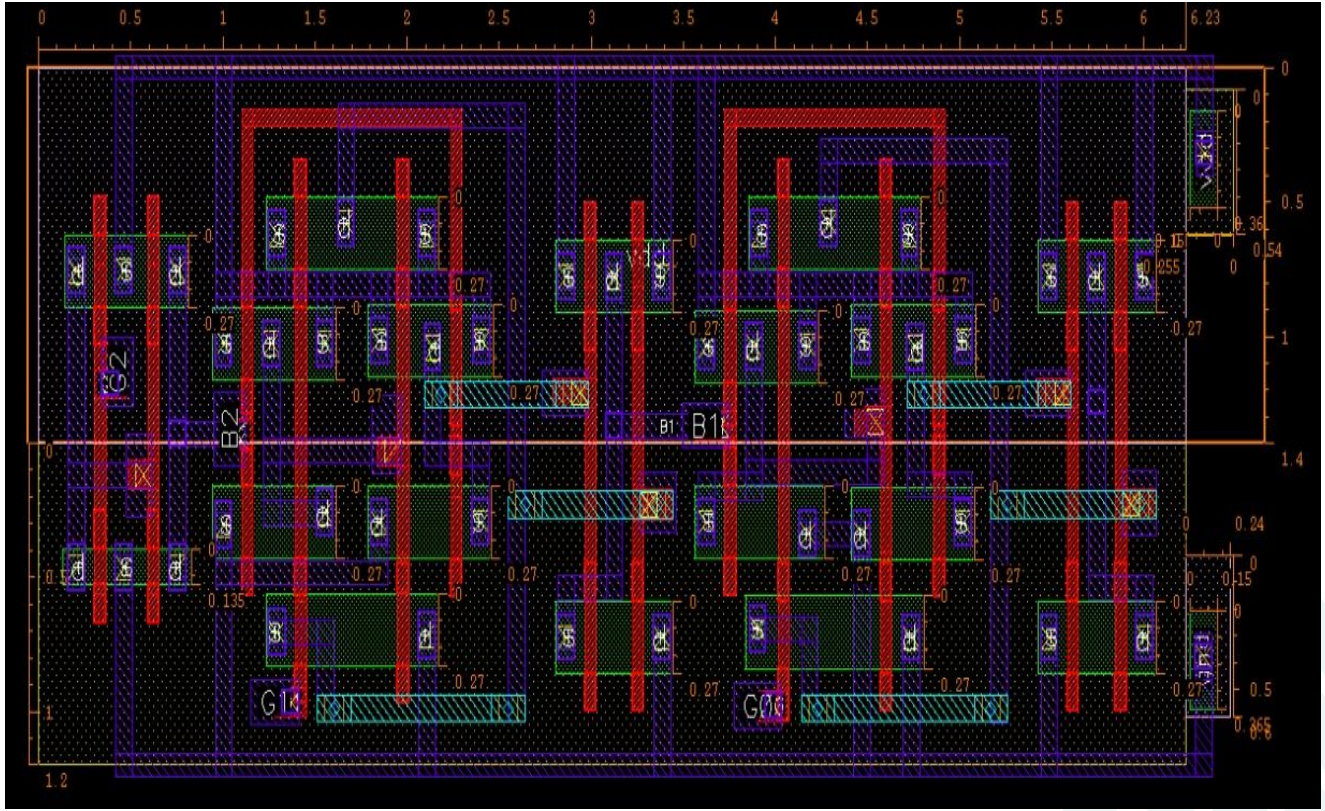


Circuit using Nand logic
PMOS - 2*0.135 = 0.270um
NMOS - 2*0.135 = 0.270 um

Unit Inverter
PMOS - 2*0.135 = 0.270um
NMOS - 1*0.135um

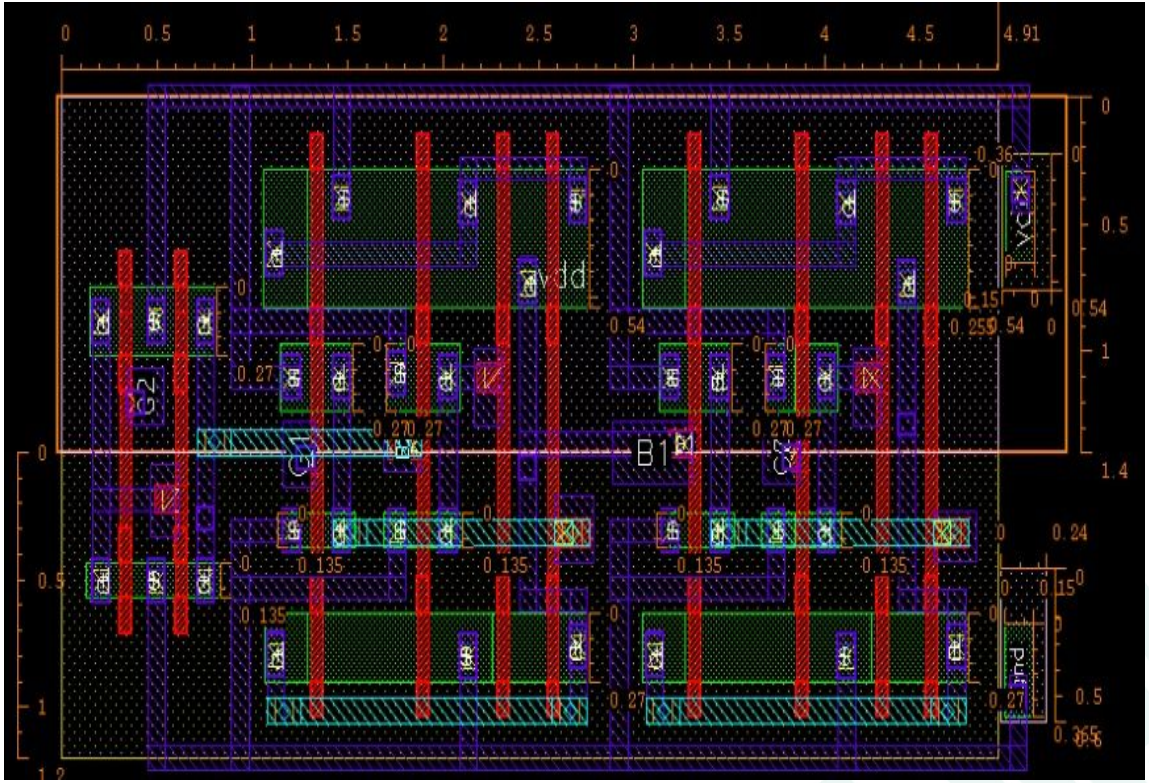
Layout - NAND

Nand area: 16.198 um2
Height: 13 tracks
Width: 31.15 tracks



Layout - XOR

Xor area: 12.766 um2
Height: 13 tracks
Width: 24.55 tracks

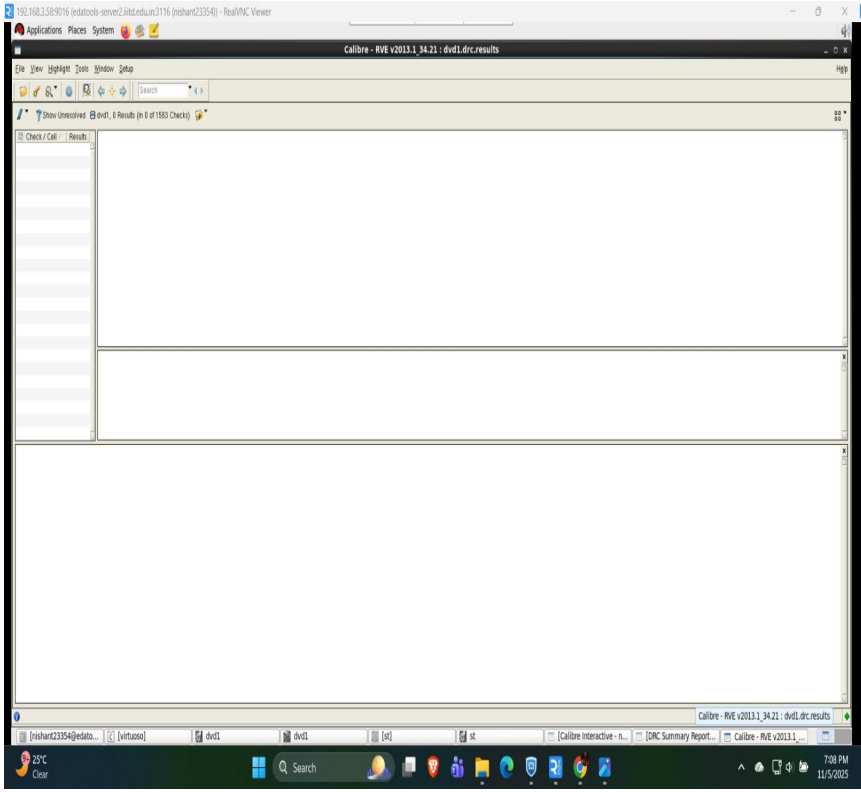


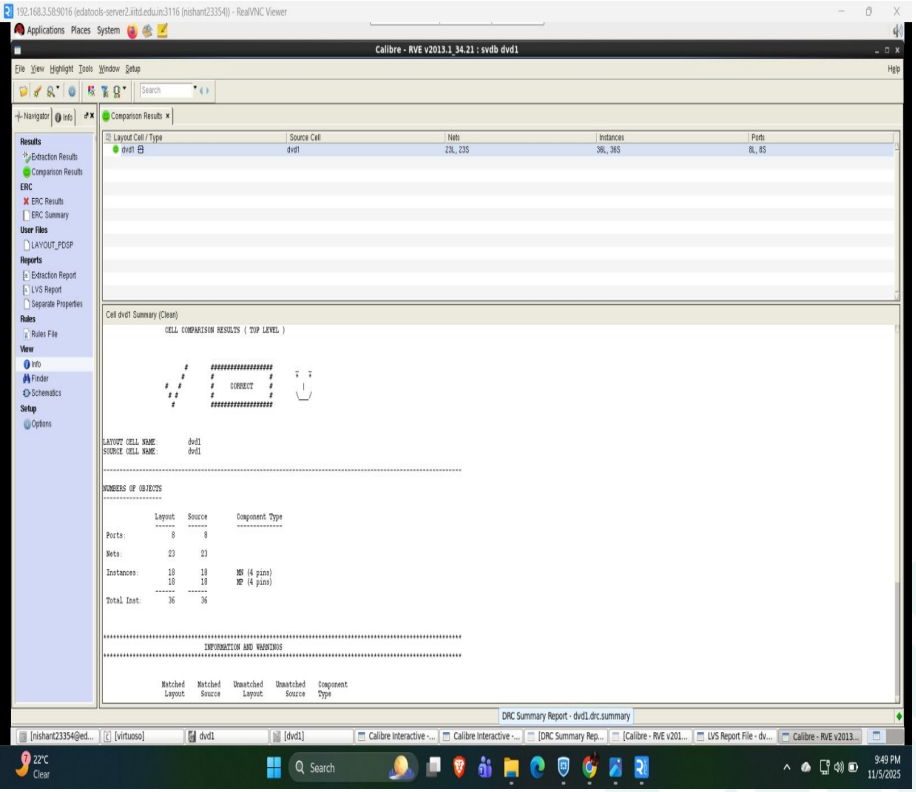
Area Optimization: Maximized density by interleaving transistors and utilizing common poly gates.

Via Placement: Resolved DRC violations caused by insufficient poly/M1 overlap for M2-M1 vias.

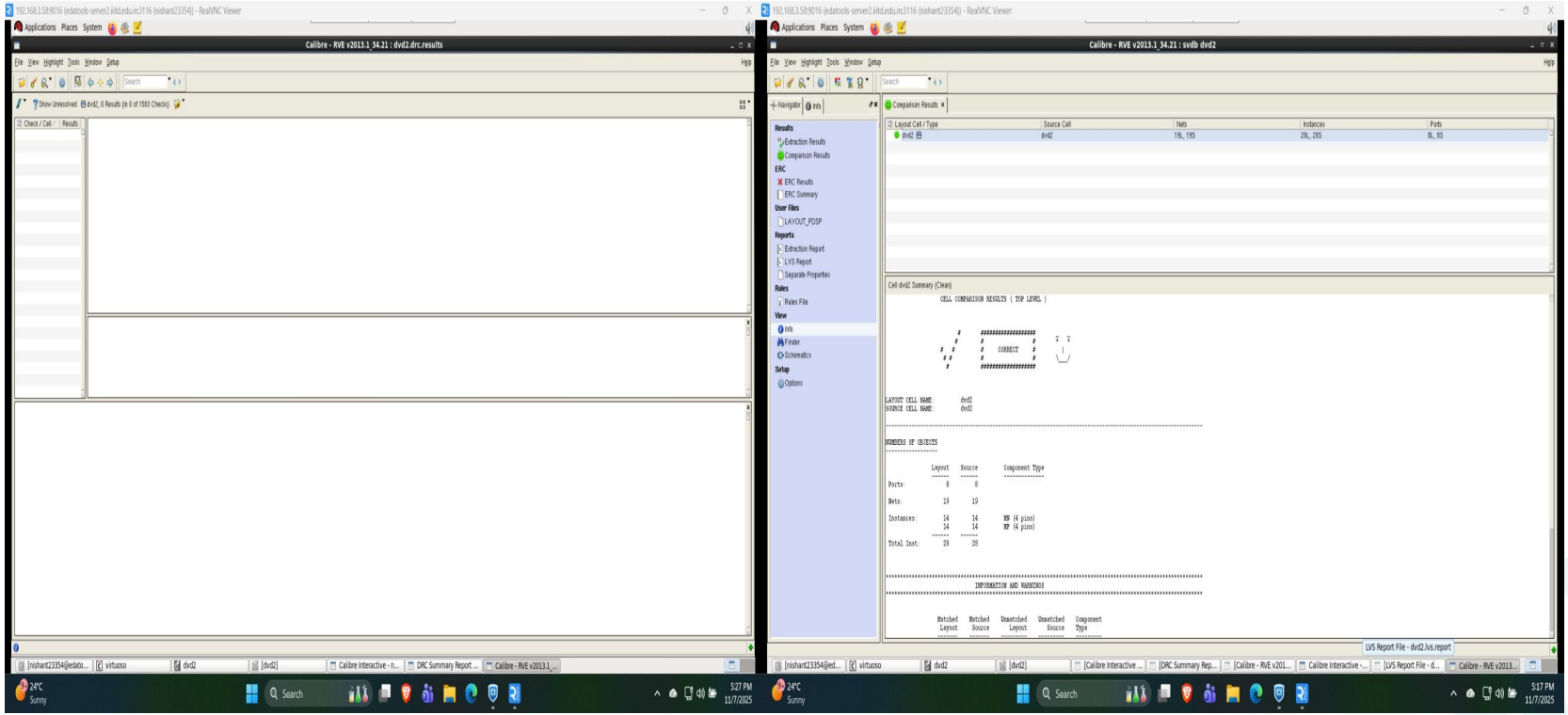
Routing Congestion: Iteratively rerouted dense metal tracks to maintain minimum spacing rules.

DRC/LVS Reports - NAND





DRC/LVS Reports - XOR



Delays - NAND

Post-Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	240	243
B1	309	341
B0	258	278

Pin -TT,1.08V,125C	Rise	Fall
B2	201	197
B1	255	266
B0	212	219

Pin -FF,1.08V,125C	Rise	Fall
B2	159	159
B1	208	207
B0	173	173

Pre -Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	227	231
B1	299	321
B0	232	255

Pin -TT,1.08V,125C	Rise	Fall
B2	191	190
B1	247	261
B0	192	205

Pin -FF,1.08V,125C	Rise	Fall
B2	157	151
B1	205	199
B0	159	158

Delays were measured by keeping rest of the bits constant

Active Bit parameters:
Type - Pulse
High value - VDD
Rise time - 100ps
Fall time - 100ps
Width - 30 ns
Period - 80 ns

Delays - XOR

Post-Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	239	242
B1	255	267
B0	269	268

Pin -**TT,1.08V,125C**	Rise	Fall
B2	200	196
B1	214	198
B0	223	217

Pin -FF,**1.08V,125C**	Rise	Fall
B2	167	159
B1	180	149
B0	186	168

Pre -Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	229	233
B1	254	261
B0	264	263

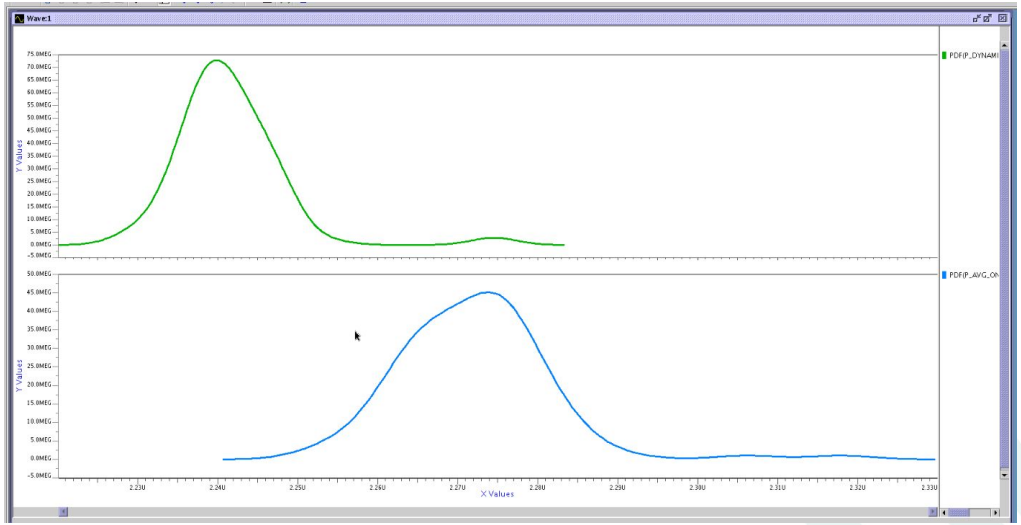
Pin -**TT,1.08V,125C**	Rise	Fall
B2	192	191
B1	212	193
B0	216	215

Pin -FF,**1.08V,125C**	Rise	Fall
B2	158	154
B1	178	147
B0	180	168

Delays were measured by keeping rest of the bits constant

Power Analysis -NAND

	Mean (uW)	Dev (uW)
Dynamic	2.24	0.006
Average	2.27	0.009
Static	0.0308	0.004



Stimuli

Vdd- 1.08 V Corner- TT Temp-125c

G1: Vdd
G2: Vdd
G0: Pulse
Frequency - 100Mhz
Delay - 20ns
Width - 5ns
Rise and fall time - 100ps

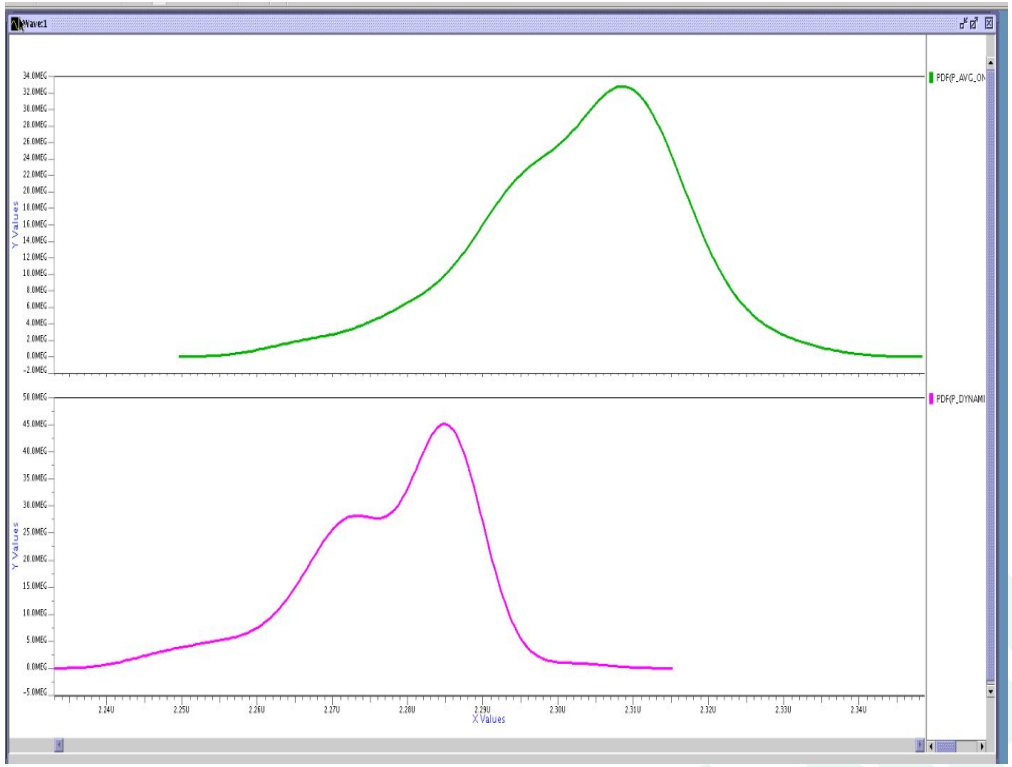
Power Analysis - XOR

	Mean (uW)	Dev (uW)
Dynamic	2.27	0.010
Average	2.30	0.012
Static	0.025	0.005

Stimuli

Vdd- 1.08 V Corner- TT Temp-125c

G1: Vdd
G2: Vdd
G0: Pulse
Frequency - 100Mhz
Delay - 20ns
Width - 5ns
Rise and fall time - 100ps



Conclusion

	NAND	XOR
Area	16.19	12.76
Power	Less and stable	Slightly more with high Variance
Delay	Less	Slightly more
No. of Transistors	36	28

- **Power Stability vs. Area:** While the **XOR** design is **~21% smaller** (12.76 vs 16.19 µm2), the **NAND** design demonstrates greater power stability with a lower standard deviation (0.009 µW vs 0.012 µW)
- **Device Efficiency:** The **XOR** implementation is more device-efficient, achieving the same logic with **22% fewer transistors** (28 vs 36) compared to the NAND implementation.
- **Performance Uniformity:** The **NAND** implementation offers slightly tighter control over delay variations across different process corners compared to the XOR design.

Work Distribution

Layout and sizing - Sameer and Nishant

Delay and PVT calculations - Khushal

Xcircuit and Presentation - Cumulative Effort

THANK YOU