

# 3 bit Gray to Binary Converter

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Group Number: 8

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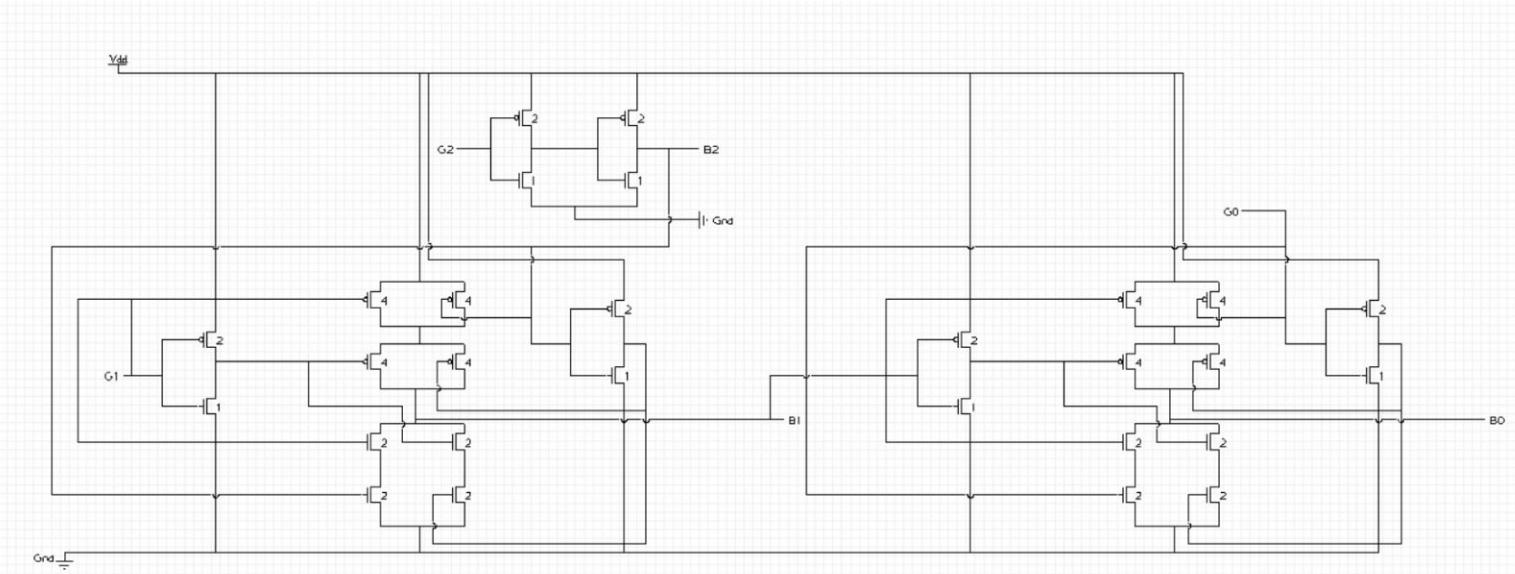
**Nishant Prajapati** : 2023354



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# Schematic + Sizing



**Circuit using Xor logic**

$$\text{PMOS} - 4 \cdot 0.135 = 0.540\mu\text{m}$$

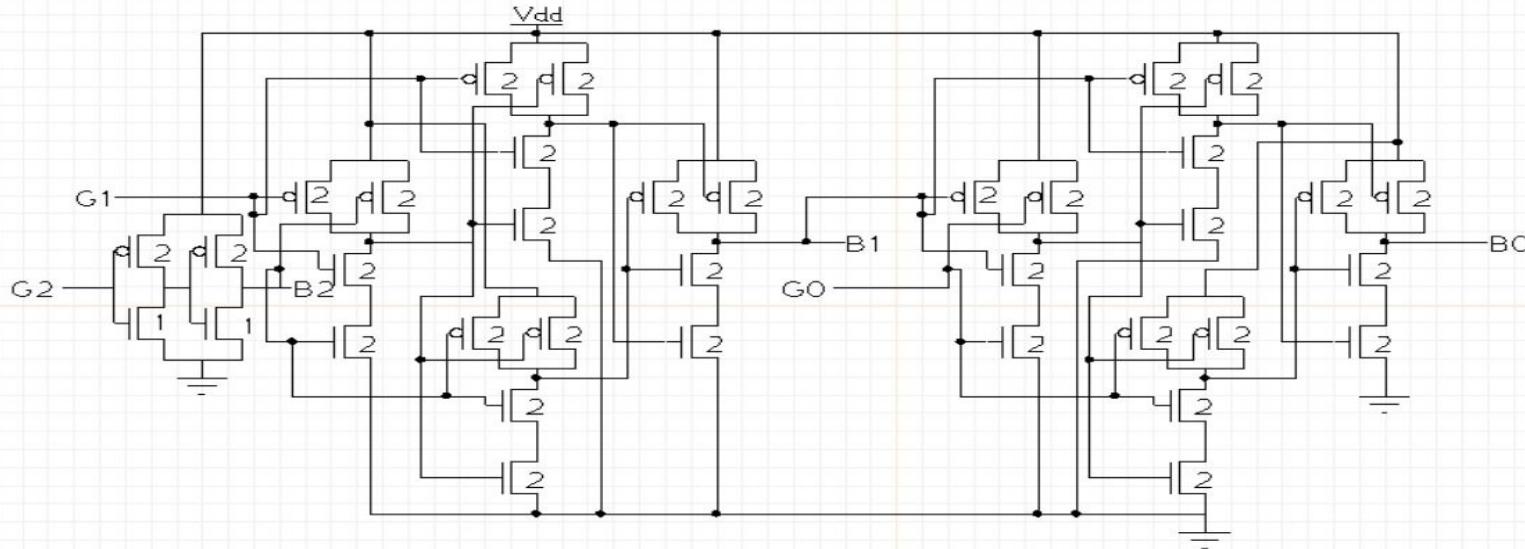
$$\text{NMOS} - 2 \cdot 0.135 = 0.270 \mu\text{m}$$

**Unit Inverter**

$$\text{PMOS} - 2 \cdot 0.135 = 0.270\mu\text{m}$$

$$\text{NMOS} - 1 \cdot 0.135\mu\text{m}$$

# Schematic + Sizing



Circuit using Nand logic

$$\text{PMOS} - 2 \cdot 0.135 = 0.270\mu\text{m}$$

$$\text{NMOS} - 2 \cdot 0.135 = 0.270 \mu\text{m}$$

Unit Inverter

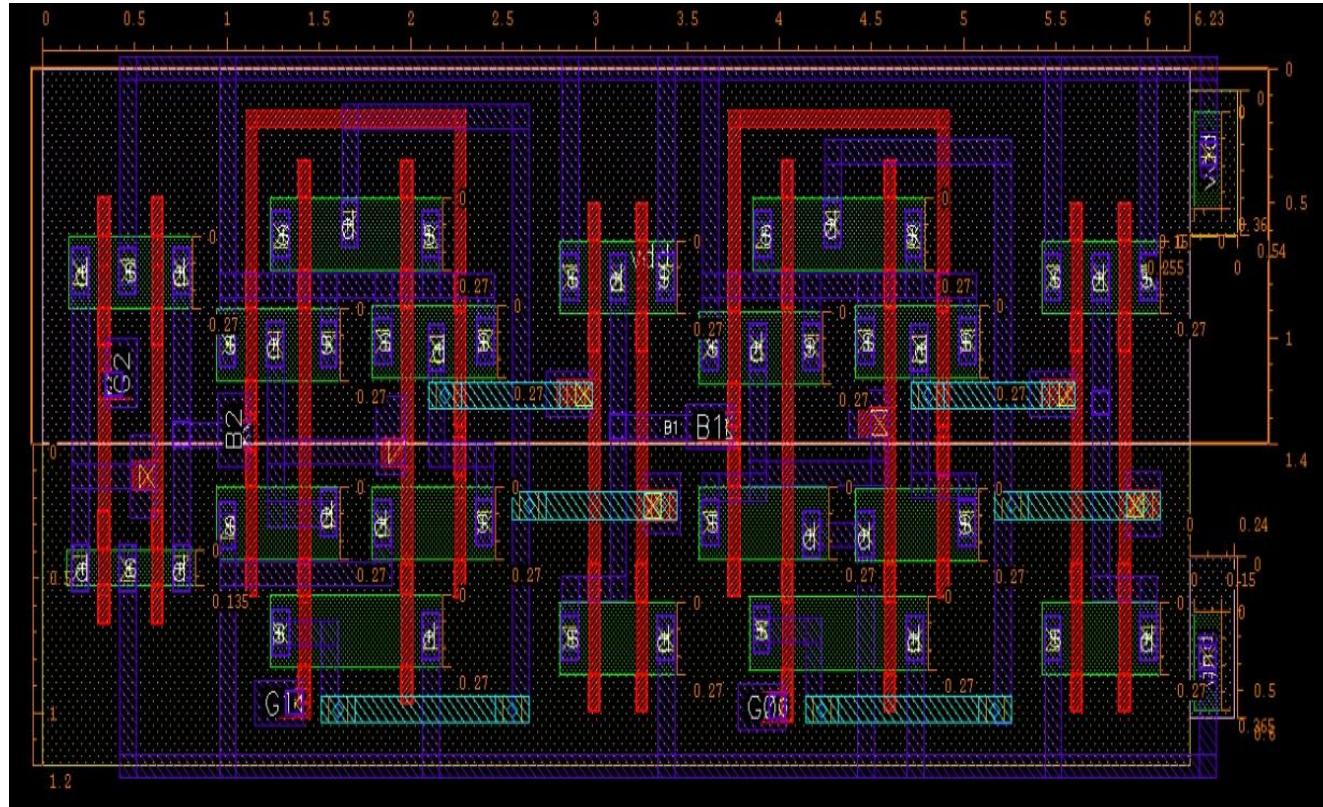
$$\text{PMOS} - 2 \cdot 0.135 = 0.270\mu\text{m}$$

$$\text{NMOS} - 1 \cdot 0.135\mu\text{m}$$

# Layout - NAND



Nand area: 16.198 um<sup>2</sup>  
Height: 13 tracks  
Width: 31.15 tracks



# Layout - XOR



Xor area: 12.766 um<sup>2</sup>

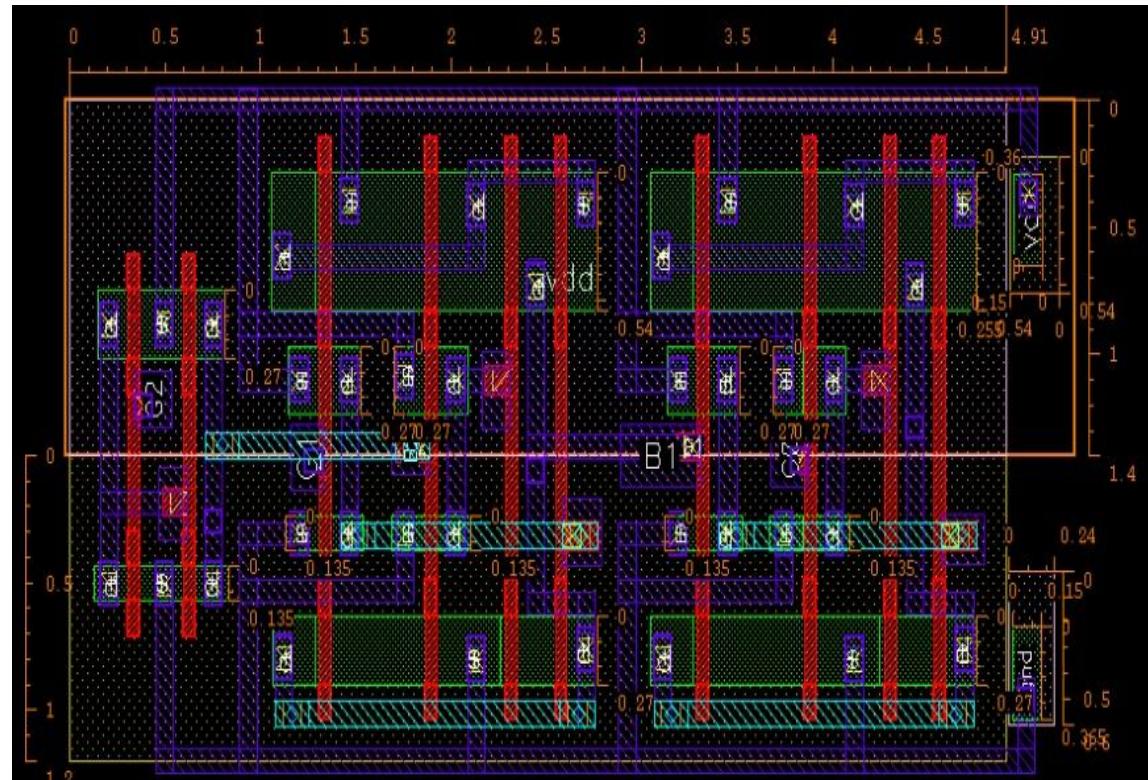
Height: 13 tracks

Width: 24.55 tracks

**Area Optimization:** Maximized density by interleaving transistors and utilizing common poly gates.

**Via Placement:** Resolved DRC violations caused by insufficient poly/M1 overlap for M2-M1 vias.

**Routing Congestion:** Iteratively rerouted dense metal tracks to maintain minimum spacing rules.



# DRC/LVS Reports - NAND



Two windows of Calibre RVE v2013.1 are displayed side-by-side, showing DRC and LVS results for a NAND design.

**Left Window (dvd1.drc.results):**

- Shows the "Calibre - RVE v2013.1\_34.21 : dvd1.drc.results" interface.
- The left pane displays a large, mostly empty workspace with a few small red markers.
- The right pane shows the "Results" tree and a summary table:

Layout Cell / Type	Source Cell	Nets	Instances	Perf
dvd1	dvd1	23, 23S	36, 36S	8, 8S

- Below the table, the "Cell dvd1 Summary (Clear)" section provides detailed statistics:

  - LAYOUT CELL NAME: dvd1
  - SOURCE CELL NAME: dvd1
  - NUMBERS OF OBJECTS:

	Layout	Source	Component Type
Ports:	8	8	
Mets:	23	23	
Instances:	18	18	NP (4 pins)
	18	18	NP (4 pins)
Total Inst:	36	36	
  - INFORMATION AND WARNINGS:

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type

**Right Window (svdb.dvd1):**

  - Shows the "Calibre - RVE v2013.1\_34.21 : svdb.dvd1" interface.
  - The left pane shows the "Comparison Results" table:

Layout Cell / Type	Source Cell	Nets	Instances	Perf
dvd1	dvd1	23, 23S	36, 36S	8, 8S

  - The right pane displays the "Cell dvd1 Summary (Clear)" section, which is identical to the one in the left window.

# DRC/LVS Reports - XOR



Two windows of Calibre - RVE v2013.1\_34.21 are displayed side-by-side, showing DRC and LVS results for the dv2 cell.

**Left Window (DRC Results):**

- File View Highlight Tools Window Setup
- Search
- Show Unresolved: dv2: 0 Results (n = 0 of 1533 Checks)
- Check / Cell / Results

**Right Window (LVS Results):**

- File View Highlight Tools Window Setup
- Search
- dv2: Comparison Results
- Results Extraction Results Comparison Results ERC
- ERC Results ERC Summary
- User Files LAYOUT\_PSP Reports Extraction Report LVS Report Separate Properties
- Rules Rule File
- View Info Finder Schematics Setup Options

**Comparison Results:**

Layout Cell / Type	Source Cell	Net	Instances	Ports
dv2	dv2	15, 155	20, 105	8, 85

**Cell dv2 Summary (Clean): CELL COMPARISON RESULTS ( TOP LEVEL )**

LAYOUT CELL NAME: dv2  
SOURCE CELL NAME: dv2

**NUMBER OF OBJECTS**

Layout	Source	Component Type
Ports	8	8
Wires	19	19
Instances	14	14
Total Inst:	28	28

**Instances:** 14 (4 pins), 14 (4 pins)

**INFORMATION AND WARNINGS**

Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
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LVS Report File - dv2.lvs.report

Taskbar:

- Irishan2354@edt00
- virtuso
- dv2
- Calibre Interactive - n...
- DRC Summary Report...
- Calibre - RVE v2013.1\_...
- Irishan2354@edt00
- virtuso
- dv2
- Calibre Interactive -...
- DRC Summary Report...
- Calibre - RVE v2013.1\_...
- LVS Report File - d...
- Calibre - RVE v2013.1\_...

System tray:

- 24°C Sunny
- 24°C Sunny

Bottom status bar:

- 5:27 PM 11/7/2025
- 24°C Sunny
- 5:27 PM 11/7/2025

# Delays - NAND



Post-Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	240	243
B1	309	341
B0	258	278

Pin -TT,1.08V,125C	Rise	Fall
B2	201	197
B1	255	266
B0	212	219

Pin -FF,1.08V,125C	Rise	Fall
B2	159	159
B1	208	207
B0	173	173

Pre -Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	227	231
B1	299	321
B0	232	255

Pin -TT,1.08V,125C	Rise	Fall
B2	191	190
B1	247	261
B0	192	205

Pin -FF,1.08V,125C	Rise	Fall
B2	157	151
B1	205	199
B0	159	158

*Delays were measured by keeping rest of the bits constant*

*Active Bit parameters:*  
*Type - Pulse*  
*High value - VDD*  
*Rise time - 100ps*  
*Fall time - 100ps*  
*Width - 30 ns*  
*Period - 80 ns*

# Delays - XOR



Post-Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	239	242
B1	255	267
B0	269	268

Pin -TT,1.08V,125C	Rise	Fall
B2	200	196
B1	214	198
B0	223	217

Pin -FF,1.08V,125C	Rise	Fall
B2	167	159
B1	180	149
B0	186	168

Pre -Layout

Pin -SS,1.08V,125C	Rise	Fall
B2	229	233
B1	254	261
B0	264	263

Pin -TT,1.08V,125C	Rise	Fall
B2	192	191
B1	212	193
B0	216	215

Pin -FF,1.08V,125C	Rise	Fall
B2	158	154
B1	178	147
B0	180	168

*Delays were measured by keeping rest of the bits constant*

# Power Analysis -NAND



	Mean (uW)	Dev (uW)
Dynamic	2.24	0.006
Average	2.27	0.009
Static	0.0308	0.004

## Stimuli

Vdd- 1.08 V Corner- TT Temp-125c

G1: Vdd

G2: Vdd

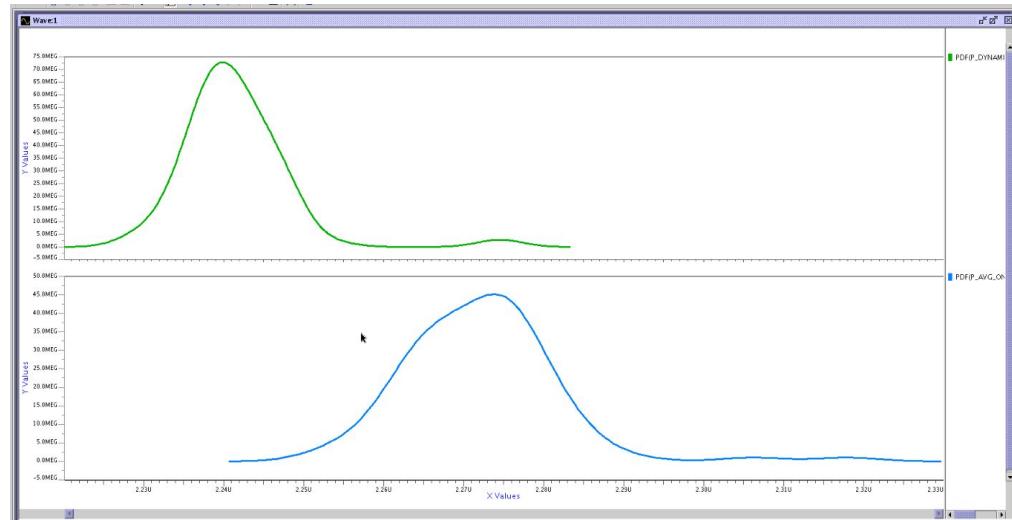
G0: Pulse

Frequency - 100Mhz

Delay - 20ns

Width - 5ns

Rise and fall time - 100ps



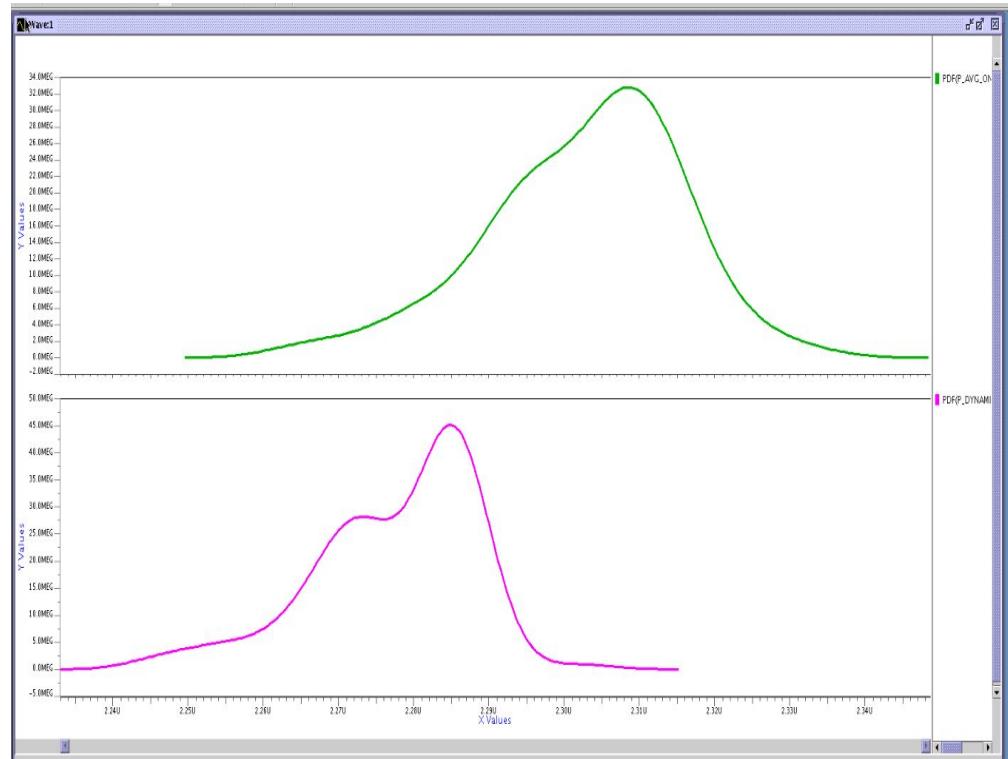
# Power Analysis - XOR



	Mean (uW)	Dev (uW)
Dynamic	2.27	0.010
Average	2.30	0.012
Static	0.025	0.005

**Stimuli**  
**Vdd- 1.08 V Corner- TT Temp-125c**

G1: Vdd  
G2: Vdd  
G0: Pulse  
Frequency - 100Mhz  
Delay - 20ns  
Width - 5ns  
Rise and fall time - 100ps



# Conclusion



	NAND	XOR
Area	16.19	12.76
Power	Less and stable	Slightly more with high Variance
Delay	Less	Slightly more
No. of Transistors	36	28

- **Power Stability vs. Area:** While the **XOR** design is **~21% smaller** ( $12.76 \text{ vs } 16.19 \mu\text{m}^2$ ), the **NAND** design demonstrates greater power stability with a lower standard deviation ( $0.009 \mu\text{W}$  vs  $0.012 \mu\text{W}$ )
- **Device Efficiency:** The **XOR** implementation is more device-efficient, achieving the same logic with **22% fewer transistors** (28 vs 36) compared to the NAND implementation.
- **Performance Uniformity:** The **NAND** implementation offers slightly tighter control over delay variations across different process corners compared to the XOR design.

# Work Distribution

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Layout and sizing - Sameer and Nishant

Delay and PVT calculations - Khushal

Xcircuit and Presentation - Cumulative Effort

THANK YOU

