Course: B.Tech Computer Science and Engineering
(Artificial Intelligence & Machine Learning)
Subject: Digital Logic & System Design, Subject Code: ETEE104
Semester: II

Time: 03 Hours **Max Marks: 70**

Instructions to the Students:

1. This Question paper consists of two Sections. All sections are compulsory.
2. Section A comprises 10 questions of short answer type. All questions are compulsory. Each question carries 02 marks.
3. Section B comprises 8 long answer type questions out of which students must attempt any 5. Each question carries 10 marks.
4. Do not write anything on the question paper.
5. Assume suitable parameters (if not given).

Q. No.	SECTION –A (SHORT ANSWER TYPE QUESTIONS)	Marks
1. a.	What do you understand by Digital Signal? Illustrate with examples.	(2)
b.	Convert decimal number $(25.125)_{10}$ into Binary $(\ )_2$ and hexadecimal $(DAD)_{16}$ into Binary $(\ )_2$.	(2)
c.	What are Maxterms? Give examples.	(2)
d.	What is significance of code conversion? Draw the logic diagram of Binary to Grey code conversion.	(2)
e.	Compare Latch and Flip Flop.	(2)
f.	Realize T - Flip Flop using J-K Flip Flop.	(2)
g.	Explain with examples the need of A/D and D/A converters.	(2)
h.	What is encoding? Explain in context to Analog to Digital conversion	(2)
i.	How can the access time of semiconductor memory be improved? Explain.	(2)
j.	Explain briefly the importance of programmable logic devices in Digital System Design.	(2)

SECTION –B (LONG ANSWER TYPE QUESTIONS)

2. a. Implement the logic function $F = A\bar{B} + \bar{A}B$ using two input NAND gate only. (5)

   b. What is CMOS logic Family? Realize the logic function $F = \overline{AB}$ using CMOS. (5)

3. Given the following Boolean Function: $F = \bar{A}C + \bar{A}B + A\bar{B}C + BC$

   a. Express it in sum of Minterms. (5)

   b. Find the minimal sum of products expression. (5)

4. What is Parity Bit? Explain Even Parity generator and Even parity checker with example.. (10)

5. What is race around condition in J-K Flip Flop and How it can be minimized? Explain. (10)

6. Elaborate the role of counter in Digital System Design? Design a synchronous 3- bit up/down counter using J-K Flip Flop. (10)

7. What is quantization? Explain successive approximation A/D converter. (10)

8. a. Explain the concept of memory organization and operation. (5)

   b. What is CAM? Explain. (5)

9. Write note on the following: (5)

   a. ROM as PLD.

   b. FPGA (5)

===END OF PAPER===