Practice Set -2 for 5th Semester COA ETE Examination

Q.1 Discuss the various pipeline conflicts or pipeline hazards.

Q.2 How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

Q.3 The main memory has 3-page frames (frame 0, frame 1 and frame 2). Pages from virtual memory are required in the order 2,3,2,1,5,2,4,5,3,2,5,2. Calculate the Hit ratio using FIFO replacement Algorithm

Q.4 What is the significance of page replacement? How many pages fault occurs in FIFO and LRU for the reference string 1,2,3,4,5,3,4,1,6,7,8,7,8,9,7,8,7,8,9,5,4,5,4,2 with 4-page frames?

Q.5 Examine the 8-bit programmable parallel port using a clear and well-organized diagram.

Q.6 Explain various types of I/O channels with the help of diagram.

Q.7 Determine the number of clock cycles that it takes to process 100 tasks in a six-segment pipeline.

Q.8 Discuss I/O interface with the help of its block diagram. What is the major requirement of an I/O interface?

Q.9 Describe Magnetic Disks and Magnetic Tapes in detail.

Q.10 How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? How many lines must be decoded for chip select? Specify the size of the decoders.

Q.11 A non-pipeline system takes 50 ns to process a task. The same task can process in a six-segment pipeline with a dock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can achieved? What is the maximum speedup that can achieved?

Q.12. A cache memory has access time of 40 ns and main memory access time is 160 ns. Calculate the average access time of CPU if the hit ratio is 80%.

Q.13 Discuss hardware organization of associative memory with the help of its block diagram.

Q.14 Consider a fully associative mapped cache of size 512 KB with block size 1 KB. There are 17 bits in the tag. Find-

a) Size of main memory
b) Tag directory size

Q.15 Distinguish between Strobe Control and Handshaking techniques for asynchronous data transfer.

Q.16 Demonstrate the block diagrams and functionalities of integrated circuit chips for RAM and ROM.

Q.17 Describe the concept of daisy-chaining. Devise a single-stage daisy-chaining priority logic circuit and elucidate its operation, detailing how it manages interrupt-initiated I/O requests.

Q.18 Design parallel priority interrupt hardware for a system with four interrupt sources using priority encoder.

Q.19 Explain the Direct Memory Transfer (DMA) techniques used for data transfer in a computer system in detail.

Q.20 Differentiate between the following:

a) RISC vs CISC Processor
b) Hardwired Control Unit vs Micro-programmed Control Unit

c) Vectored and Non- vectored Interrupts
d) Write -Through and Write Back policy of Cache

Q.21 Compare and contrast the following page replacement policies.

a) LRU page replacement
b) FIFO page replacement
c) Optimal page replacement

Assuming three frames, determine how many page faults would occur for the following page reference string: 1,2,3,4,2,1,5,6,2,1,2,1,5,6 in each of the mentioned replacement algorithm.

Q.22 Explain the concept of Virtual memory. Also, elaborate how memory management is done by using paging and segmentation.

Q.23 Design a common bus system for a digital computer system having four registers of 4-bit using 3-state buffers.

Q.24 Explain the three different modes of transfer: Programmed I/O, Interrupt- Initiated, and Direct Memory Transfer. Show the flowchart for CPU program flow in Programmed I/O.

Q.25 Distinguish between the following:

a) Isolated I/O vs Memory Mapped
b) SRAM vs DRAM
c) Serial Communication vs Parallel Communication
d) Primary memory vs Secondary memory