Practice Set -1 for 5th Semester COA ETE Examination

Q.1 In a digital computer system having 32 registers of size 64 bits each, a common bus system has to be designed using multiplexers. Determine the following for the common bus system design

a) How many multiplexers are required?
b) What is the size of each multiplexer?
c) How many selection inputs are there in each multiplexer?

Q.2 Apply binary multiplication method for signed- magnitude numbers and perform the multiplication of 11 as Multiplicand and 13 as Multiplier.

Q.3 Give the hardware implementation of the following register transfer language (RTL) statement using the block diagram

a) w + P: R5 ← R7, R7 ← R5
b) abc + a'bc +abc': AR ← AR + AC

Q.4 Perform conversion of the following arithmetic expressions from infix notation to reverse polish notation (RPN) for part (a), (b), and (c) and vice-versa in remaining parts of the question.

a) A + B*[C*D + E*(F + G)]
b) A*[B + C*(D + E)] / (F*(G + H))
c) P*Q + R*S + Y*Z
d) A B C D E + * - /
e) A B C D E * / - +
f) A B C * / D - E F / +
g) A B C D E F G + * + * + *

Q.5 An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

Q.6 The four 8-bit registers along with their values are: AR = 11110010, BR = 11111111, CR = 10111001 and DR = 11101010. Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

a) AR ← AR + BR
b) CR ← CR ^ DR
c) BR ← BR + 1
d) AR ← AR – CR

Q.7 Design a 4-bit Adder/ Subtractor using parallel adder.

Q.8 Design 4 bit carry look ahead adder.

Q.9 Explain the microoperations involved for the PUSH and POP operations in a register stack and also for a memory stack with an example.

Q.10 A computer is designed for 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions then calculate the maximum number of one-address instructions that can be generated?

Q.11 Execute the arithmetic calculations below using binary numbers and negative numbers represented in signed 2's complement form. Employ seven bits to represent each number along with its sign. For each case, ascertain the presence of overflow by examining the carries into and out of the sign bit:

a) (+35) + (+40) b) (-35) + (-40)

Q.12 Design and explain the working of 4-bit Arithmetic Circuit that can perform any of the following micro-operations: addition, subtraction, increment, and decrement.

Q.13 Perform multiplication of 5-bit numbers using Booth's Algorithm of the following

a) (+14) X (-14)
b) (-7) X (+3)
c) $(10010)_2$ X $(10100)_2$

Q.14 Explain the various addressing modes with the help of a numerical example.

Q.15 Display the values stored in registers E, A, Q, and SC throughout the multiplication procedure of the binary numbers 11111 (multiplicand) and 10101 (multiplier). The given binary representation does not include signs.

Q.16 Specify the control word that must be applied to the processor having general register organisation to implement the following microoperations. Define the control word necessary for a processor with a general register organization to execute the following microoperations. Note that operation codes for add, complement, decrement, shift left and input are 00010, 01110, 00110, 11000 and 00000 respectively.

a) R2 ← R3 - R5
b) R6 ← Complement of R6
c) R8 ← R8 -1
d) R4 ← SHL R7
e) R9 ← Input

Q.17 Show the contents of registers E, A, Q, and SC during the process of division of 00001111 by 0011.

Q.18 Design a common bus system for a digital computer system having 4 registers, each of 8-bit size.

Q.19 Create a program to assess the given arithmetic expression utilizing zero, one, two, or three address instructions: X = (A +B) * (C + D)

Q.20 Find 11 divided by 3 using restoring division algorithm.

Q.21 Perform following binary subtraction using 2's complement method where the values of X and Y are 1010100 and 1000011 respectively.

a) X – Y b) Y - X

Q.22 An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is: (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) index with R1 as the index register.

Q.23 Design a common bus system for a digital computer system having four registers of 4-bit using 3-state buffers.

Q.24 A bus-organized CPU (general register organisation) has 16 registers with 32 bits in each, an ALU, and a destination decoder. Evaluate following.
(a) How many multiplexers are there in the A bus (or B bus), and what is the size of each multiplexer.
(b) How many selection inputs are needed for MUX A and MUX B?
(c) How many inputs and outputs are there in the decoder?
(d) How many inputs and outputs are there in the ALU for data, including input and output carries?
(e) Formulate a control word for the system assuming that ALU has 40 operations.