Wilkinson Power Divider Design

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***Abstract*—This project focuses on the design and simulation of a 2 GHz, 50Ω Wilkinson power divider using Keysight ADS. The objective is to develop a two-metal layer PCB layout with copper as the conductive material and FR4 as the dielectric substrate with a dielectric constant of 4.6. The design utilizes a 0402 footprint for isolating resistors. The process begins with impedance line calculations using the Control Impedance Line Designer in ADS, followed by piecewise simulations of individual segments using S-parameter models. Subsequently, a complete EM simulation of the entire Wilkinson divider is performed to validate performance. Ideal resistors are assumed while simulating SnP files. The report documents the design choices, simulation results, and rationale behind the selected methodology.**

I. Introduction

The Wilkinson power divider is a widely used passive microwave component that splits an input signal into two equal and in-phase output signals while providing excellent impedance matching and high isolation between output ports. It is commonly used in RF and microwave systems such as communication networks, radar systems, and signal processing applications.

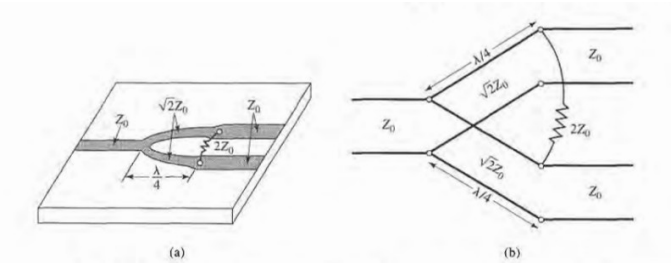

Fig. 1. Schematic Simulation output [1]

A Wilkinson power divider consists of a 50Ω input and output transmission lines, with two 70.7Ω lines connecting the input line to the output ports. Based on even-odd mode analysis, a Wilkinson power divider has reciprocity. This essentially means S21 = S12 and S13 = S31. Its high matching feature means that S23 = S32. This helps us get a picture of the output even before simulating.

This project focuses on designing a 2 GHz, 50Ω Wilkinson divider using electromagnetic (EM) simulation in Keysight ADS. The design process involves calculating preliminary line dimensions using the Linecalc and designing a schematic using T-line components and simulating for S-parameters. Then using the Controlled Impedance Line Designer (CILD) individual segments were simulated and the dimensions were finalized. Using these finalized dimensions for the Wilkinson Power Divider was designed and an EM simulation was conducted.

II. Design Methodology

The design methodology can be split into 4 parts -

A. Linecalc Analysis
B. Schematic Simulation
C. Piecewise EM Simulation
D. Total EM Simulation

A. Linecalc Analysis

The process begins by configuring the MSUB component to define the substrate's characteristics, including:

- Dielectric Constant (εr) = 4.6
- Substrate Height (H) = 10 mils
- Conductor Thickness (T) = 17μm
- Dielectric Loss Tangent (TanD) = 0.02

Linecalc is then used to determine the exact transmission line dimensions. For the input transmission line (TL1), the width came out to be 459.13μm for a 50Ω characteristic impedance. For the 70.7Ω transmission lines (TL2 and TL3), the width was calculated as 232.11μm, with the electrical length set to λ/4 (90°), translating to a length of 21.09 mm.

B. Schematic Simulation

With the dimensions obtained, the schematic was designed as shown in Fig. 2. The output transmission lines match the dimensions of the input transmission line. The schematic was terminated with ground terminations and an S-parameter block was placed to complete the simulation. The frequency was swept from 1 GHz to 3 GHz to capture the desired performance.

The schematic simulation was conducted to check whether the S-parameters met the expected criteria:

- S11, S22 and S33 below -15 dB, indicating low reflection.
- S21 and S31 as close to 0 dB as possible, indicating minimal loss.

As shown in Fig. 3, the simulation results demonstrated a matched and reciprocal S-parameters, with low return loss and minimal transmission losses, confirming that the circuit met the desired specifications. Although the schematic simulation provides a reasonable approximation of the expected results, it is inherently less accurate than electromagnetic (EM) simulation due to its reliance on lumped element models,

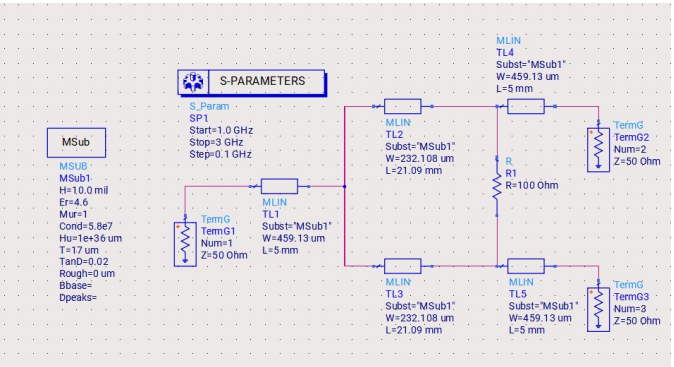

Fig. 2. Circuit Schematic

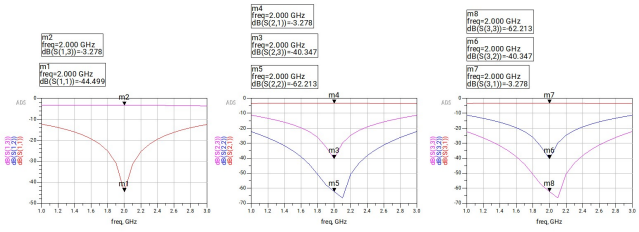

Fig. 3. Schematic Simulation output

similar to LTSpice. The simulation results confirm that S12 and S13 are equal, which is also consistent with S21 and S31, indicating that the S-parameters are matched and reciprocal. Additionally S11, S22 and S33 exhibit values below -15 dB, showing minimal return loss. The insertion losses are also near zero, confirming that the losses are within acceptable limits. With these satisfactory results, the design is ready to proceed to the layout and EM simulation phase.

C. Piecewise EM Simulation

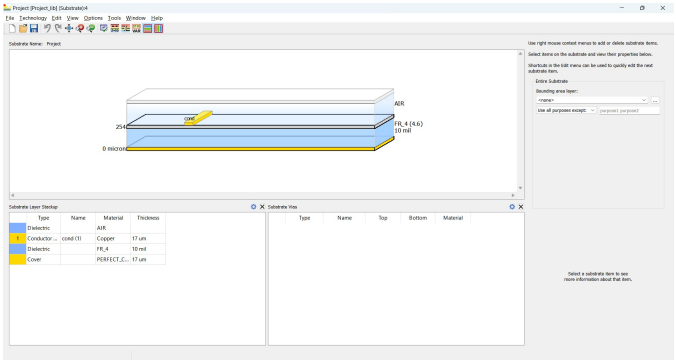

Fig. 4. Substrate

Before proceeding with the complete layout and EM simulation, a substrate was created (Fig. 4) and individual segments of the Wilkinson power divider were simulated separately to ensure accurate performance. Since the initial dimensions obtained from Linecalc may not be highly precise, CILD was used to validate and fine-tune the dimensions. The verified dimensions for the 50Ω and 70.7Ω transmission lines were then implemented in the layout.

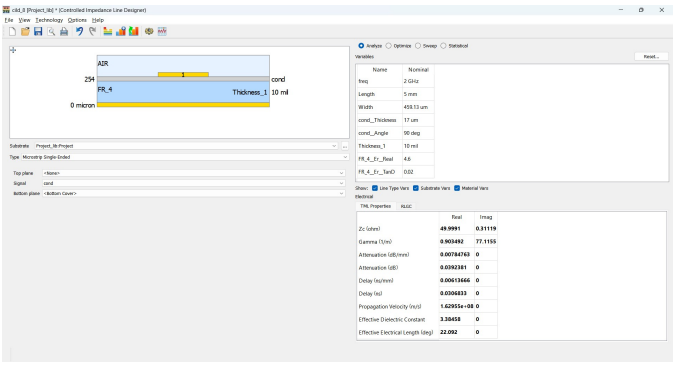

Fig. 5. 50Ω Transmission Line CILD

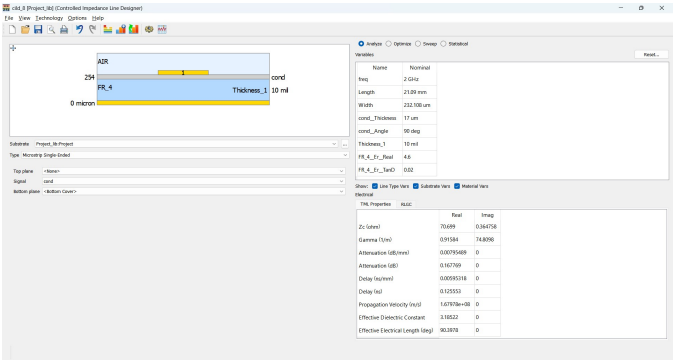

Fig. 6. 70.7Ω Transmission Line CILD

The 50Ω transmission line was modeled using the MLIN component. The dimensions derived from CILD were applied, and ports were placed at both ends for simulation. The resulting S-parameters confirmed that S11 and S22 were equal, with minimal insertion loss, indicating accurate impedance matching. The piecewise simulation results for the 50Ω line are shown in Fig. 7.

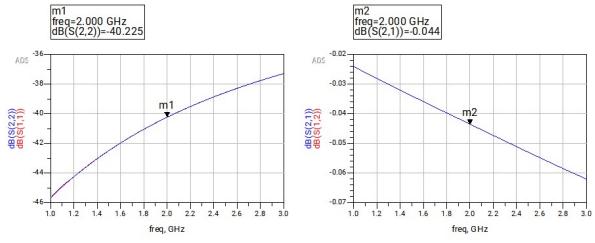

Fig. 7. 50Ω Transmission Line Piecewise Simulation Result

For the 70.7Ω transmission lines, the MCURVE component was used to create curved sections to prevent overlap and

minimize coupling effects. To achieve a 90° electrical length, the radius was calculated as

$$Radius = 21.09mm/\pi \approx 6.717 \quad (1)$$

Ports were added at the input and output, and the simulation results showed that S11 and S22 were closely matched, with negligible losses. The results of the 70.7Ω transmission line simulation are shown in Fig. 8.

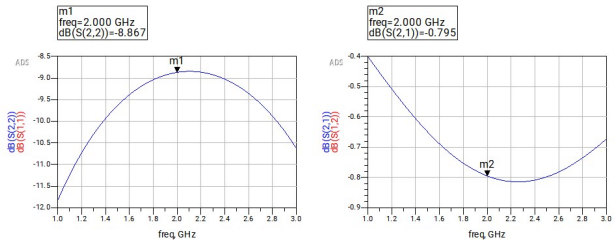

Fig. 8. 70.7Ω Transmission Line Piecewise Simulation Result

Simulating individual segments before performing a complete EM simulation ensures that each component meets design specifications, thereby minimizing errors in the final layout. The verified dimensions and simulation results provided confidence in proceeding to the complete EM simulation phase.

D. Total EM Simulation

The final layout connected the 50Ω transmission line to a microstrip-T junction (MTEE ADS) with dimensions matching the widths of the 50Ω and 70.7Ω lines. Curved transmission lines were placed on either side of the junction, and resistors were added using the R_PAD1 component, with dimensions according to provided specification.

Ports were placed at the ends of the input and output transmission lines. Since R_PAD1 does not impart resistance independently, ports were configured to contribute 100Ω of resistance. The EM simulation was performed with a frequency range of 1 GHz to 3 GHz. The realized layout is shown in Fig. 9.

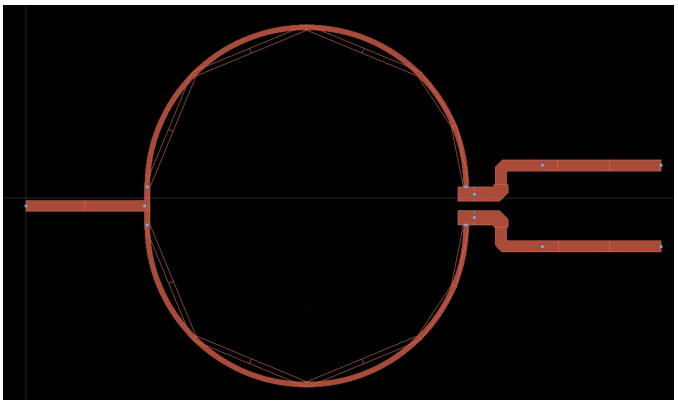

Fig. 9. Schematic Simulation output

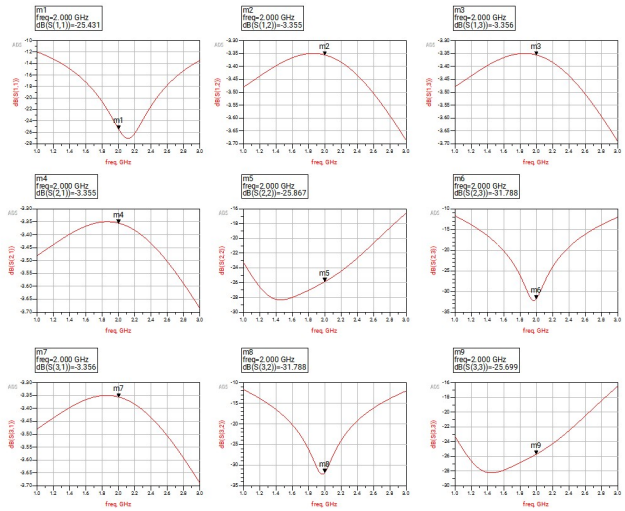

Fig. 10. 70.7Ω Transmission Line Piecewise Simulation Result

III. Result Analysis

A. S-Parameter Analysis

The S-parameter results (Fig. 10) provide insights into the performance of the Wilkinson divider in terms of return loss, insertion loss, and isolation between ports. Key observations include:

- **S11 (Return Loss):** Maintains a return loss below -20 dB at 2 GHz, indicating excellent impedance matching at the input port.
- **S21 and S31 (Insertion Loss):** Both output ports exhibit equal power division with an insertion loss close to -3 dB, as expected from a Wilkinson divider.
- **S23 (Isolation):** High isolation between output ports is achieved, with isolation values below -20 dB.

IV. Conclusion

The successful design and simulation of a 2 GHz, 50Ω Wilkinson divider was achieved using Keysight ADS. The design process involved accurate impedance line modeling, S-parameter simulations, and electromagnetic simulations to verify performance. The final design exhibits excellent return loss, minimal insertion loss, and high isolation between the output ports. The resulting design meets the required specifications.

References

[1] D. M. Pozar, Microwave Engineering, 4th ed., Wiley, 2011.

[2] Keysight Technologies, “Advanced Design System (ADS) User Manual,” 2024

[3] I. S. Jacobs and C. P. Bean, “Fine particles, thin films and exchange anisotropy,” in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.

[4] Keysight Technologies, “Advanced Design System (ADS) Distributed Components,” February 2011