High-Performance Low Noise Amplifier for Medical Applications: A Gain-Adjustable Solution

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***Abstract*— The paper presents the design of a high-gain wideband low-noise amplifier (LNA) operating above 6 GHz, targeting applications in medical systems that require significant amplification of low-intensity signals. The LNA is designed using 90 nm CMOS, and consists of a combined common-source and common-gate topology. The LNA exhibits a power gain of 29 dB over a bandwidth range of 1.7 GHz (6.6–8.3 GHz), with an average noise figure below 3 dB. Excellent impedance matching is achieved, with S_{11} < - 18.14 dB and S_{22} < - 20.23 dB respectively. Furthermore, the value of the third-order input intercept point (IIP3) is 21.1537 dBm, and the design consumes 83 mW of power at a 1.2 V supplied voltage. A gain control mechanism is introduced by integrating an input-side attenuator, enabling tunable gain without compromising other performance metrics.**

***Index Terms*— Attenuator, CMOS technology, IIP3, Power consumption, Wideband LNA.**

I. INTRODUCTION

LNAs have attracted significant attention as a vital component in circuit design in the field of communication and medical systems owing to their ability to amplify weak input signals while minimizing external noise. LNA enhances the performance and efficacy of medical systems by improving signal quality and sensitivity. Recent progress has aimed at better performance of gain, bandwidth and noise to meet the demands of modern diagnostic applications. This paper presents a wideband LNA circuit, designed in 90 nm Cadence Technology using common gate common source cascaded circuit, operating at a low supply voltage (about 1.2 V).

Designing LNAs with various topologies faces challenges in limiting their use in low-power or high-performance applications like narrowband impedance matching, selective gain, high supply voltage needs, and poor noise performance[1][2]. Achieving all features simultaneously is a major challenge as conventional techniques often limit the ability to meet all specifications at a once [3][4]. Although existing designs such as resistive shunt-feedback LNAs, and UWB LNAs address noise and bandwidth issues, many multi-stage designs consume high power and occupy more area [5][6]. Traditional LNA architectures, particularly limits the bandwidth. In contrast, CMOS-based approaches offer improved linearity, better frequency response, low power consumption, and high integration potential, effectively addressing challenges in noise suppression and bandwidth optimization. So, UWB LNA could be highly linear, comparing its performance with advanced CMOS designs. [7][8][9][10]. The scalability of CMOS technology further makes it suitable for wideband applications, and RF circuit design. CMOS-based LNA strategies are explored in RF circuit principles for LNA development. Together, these insights highlight significant advancements in LNA performance, efficiency, and integration [11][12]. For example, the need for low-power, high-performance CMOS RF circuits in wireless communication is emphasized in [13][14], highlighting the importance of the LNA in amplifying weak signals with minimal noise. The challenges in designing reconfigurable multiband LNAs, such as impedance matching and maintaining low noise, are discussed. The development of an effective LNA is crucial for multi-standard receivers. The design of a two-stage UWB LNA in [15] tackles challenges like noise and impedance matching, and bandwidth improvement, showing the strong performance with low noise, high power gain, and good power efficiency and provides a clear explanation of its design, operation, and performance. The resonance frequency can limit bandwidth, emphasizing the trade-off between usable bandwidth and noise figures in MPI systems [16]. A multi-stage (4stage) optimized LNA provides efficient amplification with good isolation and low noise levels [17]. Additionally the optimized biasing technique reduces input noise and power consumption, showing strong potential for biomedical applications [18].

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In LNA design the common gate topology is preferred in the input stage due to its ease of impedance matching, excellent noise characteristics, and widened capabilities which makes it suitable for 50Ω source matching. Again a common source topology can be used as amplification stage in LNA,

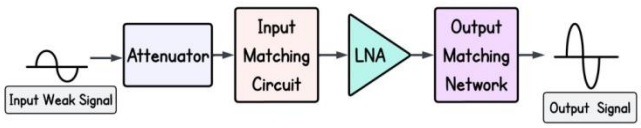


Fig. 1: Block Diagram of the proposed design

due to its high voltage gain for amplifying weak signals. Its high input impedance makes it appropriate for high-impedance sources and allows for easy gain control, providing flexibility in design. Additionally, the simple design and good isolation between the input and output enhance the stability of the CS stage, making it a reliable choice for amplification. Compared to prior works this design offers broader applicability, low noise, and tunable gain—ideal for dynamic medical applications [19][20].

In this work, we proposed a two-stage LNA using a common gate followed by a common-source topology with an input-side attenuator for improved input matching and noise performance, as shown in Fig. 1. Designed in 90 nm tech., the CG-CS cascade achieves high gain and bandwidth, targeting 7.616 GHz with a 1.7 GHz bandwidth, making it ideal for wideband biomedical application. A buffer circuit enhances output noise immunity. The main challenge was balancing power while maintaining stable high gain, as lower supply voltages reduce gain margin and increase noise sensitivity. To address this, the input-side attenuator offers a gain-adjustable solution for medical application. Circuit-level simulations show improved performance over previous work in Cadence Virtuoso. Section II details the design methodology, Section III covers performance analysis, Section IV presents results, and Section V concludes. The design is compact and efficient promising significant improvements in medical applications.

II. METHODOLOGY

A. *Proposed LNA:*

The design of wideband LNA becomes extremely challenging when analog and RF circuits operating in the sub-threshold zone display increased thermal noise, poorer bandwidth, and poor linearity, even while sub-threshold biasing gives better $\frac{gm}{I_d}$ compared to strong inversion. Our suggested LNA provides high linearity, a broad bandwidth, a modest gain, and a reasonable noise figure. To guarantee optimum performance, a number of crucial elements (such as frequency range, gain, noise figure, input/output impedance, and power consumption) must be taken into account when constructing a Low Noise Amplifier (LNA). We have first established the operational frequency range of 6.6 GHz to 8.3 GHz. A common gate (CG) stage and a common source (CS) stage with a gain-boosted, source follower buffer circuit are both included in the proposed LNA. In Fig. 2 the schematic of the proposed wideband LNA is shown. The component values of LN are summarized in Table I. The common gate amplifier circuit is utilized as a first stage because it offers superior input matching due to its low input impedance, low noise performance, and enhanced linearity. The load on the CG stage is inductive(L_1) which offers better noise performance. C_1 , the coupling capacitor blocks the dc and passes the ac signal. A LC tank is formed by L_2 *and* C_{gs_1}. The CG-CS cascaded stage is included to maintain low noise levels, supply the required gain, and permit design modifications to satisfy particular operational needs. By resonating with M_2's total capacitance at the drain, the CS stage load L_3 offers shunt peaking, improves the low-frequency gain which controls the peak at resonance, and expands the bandwidth. L_4 in the CS stage is used for obtaining better gain flatness. Two mirror circuits are used here as a biasing circuit. They are consist of a transistor (M_6, M_7), resistor (R_6, R_7) and V_{DD}. C_3 is connected between gate and the ground terminal to ensure a good AC grounding and to bypass the noise contributed by the biasing circuit. R_4 is used here to reverse isolation. To match and measure the output, a source follower buffer is introduced which isolate the output of the CS stage from the load impedance variation. After measurement, the buffer's influence must be eliminated to extract the LNA's performance alone from the entire circuit.

B. *Designing method:*

This study will be a simulation-based study using the Cadence Virtuoso 90 nm technology Software, with component values are (resistors, inductors, and capacitors) determined by a suitable matching network. An appropriate matching network will be used to estimate the values of the component. To get optimum power transmission, matching networks are utilized to match the impedance from gate to source and source to load. We may compute the input and output impedance values first using simulation tools. Subsequently, the suitable network topology will be chosen; RC networks, and L-networks are instances of common topology. The performance of the matching network is analyzed by simulation, with a special focus on bandwidth, gain, efficiency, and return loss. If the performance is not up to par, the design can be repeated numerous times by varying

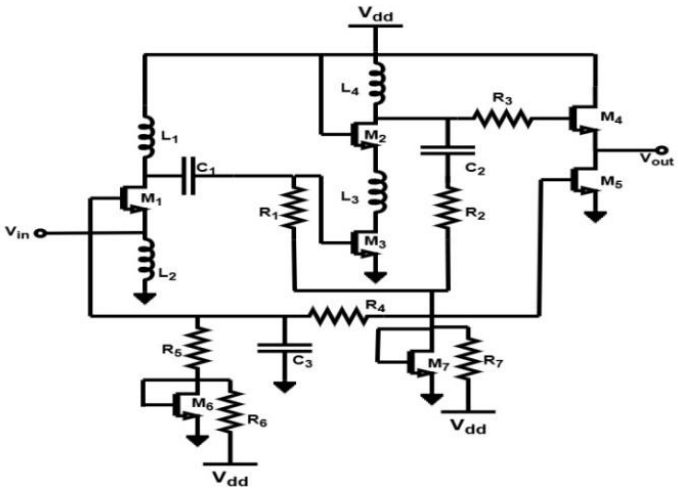


Fig. 2: Schematic of the proposed wideband low noise amplifier (with biasing circuit).

TABLE I
COMPONENTS VALUE

Aspects Ratio	**$(W/L)_1$**	**$(W/L)_2$**	**$(W/L)_3$**	**$(W/L)_4$**
	57u/100n	120u/100n	60u/100n	30u/100n
	$(W/L)_5$	**$(W/L)_6$**	**$(W/L)_7$**	
	60u/100n	60u/100n	60u/100n	
Inductor (nH)	**L_1**	**L_2**	**L_3**	**L_4**
	3.1	1	5.3	3.5
Capacitor (pF)	**C_1**	**C_2**	**C_3**	
	5	7	60	
Resistors (Ω)	**R_1**	**R_2**	**R_3**	**R_4**
	400	15e3	1e3	50
	R_5	**R_6**	**R_7**	
	500	50	40	

the component value or topology until the intended outcome is achieved.

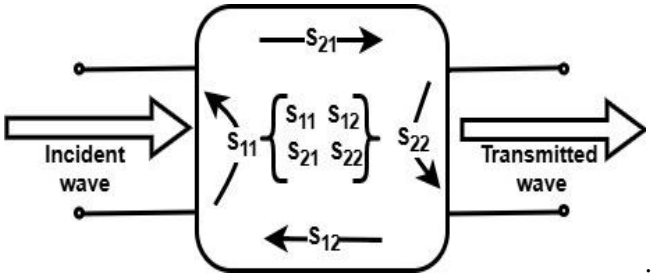
III. PERFORMANCE ANALYSIS

A. Input and output matching:

Characterizing the impedance and admittance of a two-port network operating at low frequencies often involves using the impedance matrix (Z parameters) and admittance matrix (Y parameters). However, these two approaches are insufficient for a network that operates at high frequencies. S-parameter analysis or scattering can be used instead. In this instance, the S-parameter matrix provides the link between the incident power waves that are reflected.

Let, a_1 and a_2 are incident waves; b_1 and b_2 are transmitted waves. Using a two-port network in s-parameter analysis,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$



The Equation Representation of the Matrix is as follows:

$b_1 = S_{11}a_1 + S_{12}a_2$, $\quad b_2 = S_{21}a_1 + S_{22}a_2$,

$S_{11} = \frac{b_1}{a_1}$ (when $a_2 = 0$), $\quad S_{12} = \frac{b_1}{a_2}$ (when $a_1 = 0$),

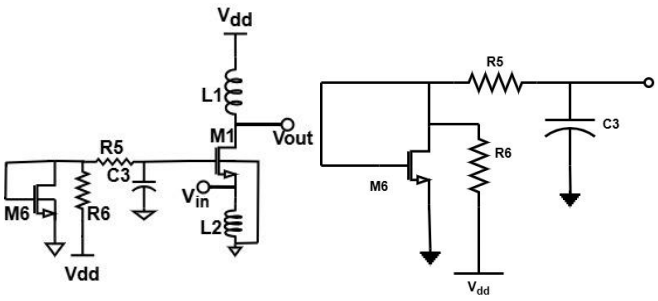
$S_{21} = \frac{b_2}{a_1}$ (when $a_2 = 0$), $\quad S_{22} = \frac{b_2}{a_2}$ (when $a_1 = 0$),

Where,

- S_{11} is the input port voltage reflection coefficient, ($S_{11} = |Z_{in} - Z_s| / |Z_{in} + Z_s|$)
- S_{12} is the reverse voltage gain
- S_{21} is the forward voltage gain
- S_{22} is the output port voltage reflection coefficient

Impedance matching can be done in various ways. A wideband CG-LNA's input matching is achieved by setting its trans-conductance to $g_m = 1/R_s$, where $R_s = 50\Omega$ represents the source impedance. To ensure that mismatching issues are kept to a minimum, the LNA's input must be matched to 50Ω. Finding the right methods is necessary to obtain 50Ω input impedance in Fig. 3. Additionally, since impedance is purely real, a 50Ω impedance match also permits a simultaneous conjugate power match, resulting in the best possible power transmission and meeting the system requirement.

Here, Z_d is the impedance of the load, Z_{in2} is the input impedance of the next stage, and g_{m1} is the trans-conductance of the MOS transistor in common-gate configuration.



(a) (b)

Fig. 3: (a) 1st stage of LNA (Common gate stage), (b) Biasing network for CG stage,

The small-signal equivalent circuit for the impedance calculation is shown in Fig. 4.

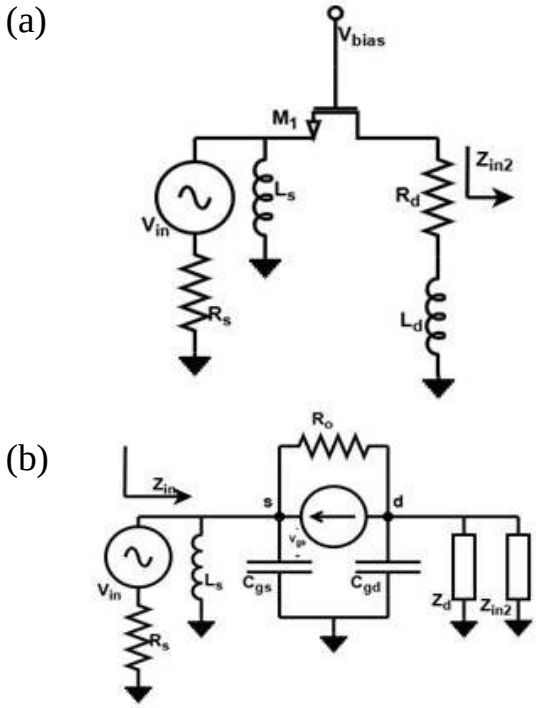


Fig. 4: (a) Configuration of a Common gate input stage, (b) Small signal in common gate

Now,

$$Z_{in} = \frac{1}{g_{m_1} + \frac{1}{Z_s} + (1 - g_{m_1}.Z_o)(R_o + Z_o)} \qquad (1)$$

Where,

$$Z_s = j\,\omega\,L_2 \parallel \frac{1}{j\omega C_{gs}} \quad \& \qquad (2)$$

$$Z_o = \frac{1}{j\omega\, c_{gd}} \parallel Z_d \parallel Z_{in2} \qquad (3)$$

Based on the aforementioned deductions, the following observations can be made: Due to the frequency-dependent Z_s dominating the imaginary component in the denominator the common-gate stage's unsatisfactory matching occurs throughout the band. The tank circuit should be designed to resonate near the center of the 6.6–8.3 GHz band to ensure good broadband matching and maintain real input impedance close to 50 Ω. The best input matching over the given bandwidth is found in MOS transistor with an aspect ratio of $\frac{57u}{100n}$ and L_2 = 1nH, according to simulations.

The value of S_{11} is -20.528 dB, suggesting better input matching in Fig. 5. Only small amount of power is reflected back at input side. Almost 1% of power is reflected back. Most of the power is entering into the amplifier rather than bouncing. Similarly the value of S_{22} in Fig. 6, indicates good

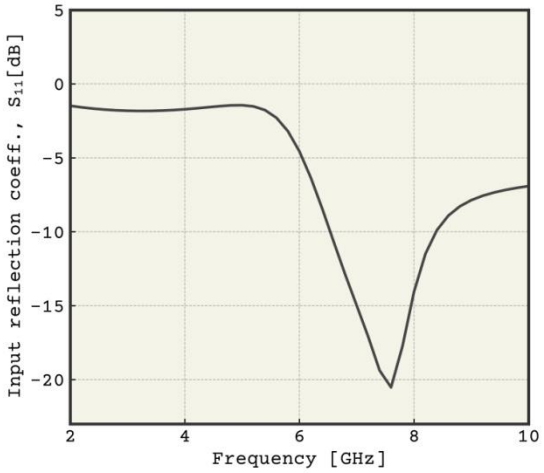


Fig. 5: Input return loss Vs Frequency

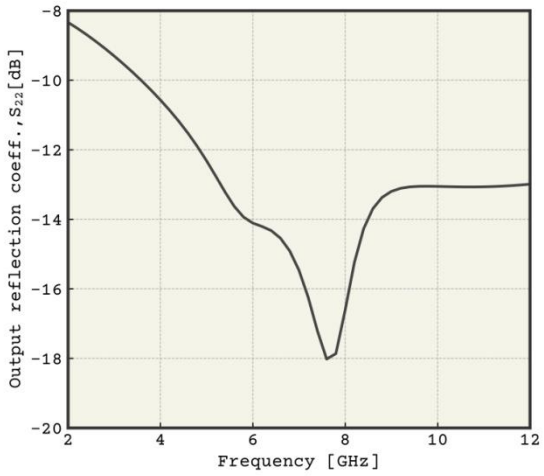


Fig. 6: Output return loss Vs Frequency

output matching. It means the most of the power is transmitted not reflecting.

B. Noise Analysis:

An LNA's noise performance is directly correlated with the matching of its input. Wide-band input matching, which cannot be tuned for a specific frequency, typically results in higher inherent noise compared to narrow-band matching. Therefore, it is important to carefully consider and make a decision regarding the strict trade-off between the wide-band input matching and the noise figure of the wideband LNA. It should be clear that the first stage amplifier's noise factor intuitively appealing that the source noise has already been gained up to that point. The noise factor is further degraded by a product of the total gain products up to that point when compared to the noise generated by the preceding system along with the already gained source noise.

The critical important data regarding a system's noise performance is contained in the Noise Figure (Noise Factor). Noise Factor (F) is another name for Noise Figure (NF). The partnership is as follows:

NF is equal to 10 *log10 (F).

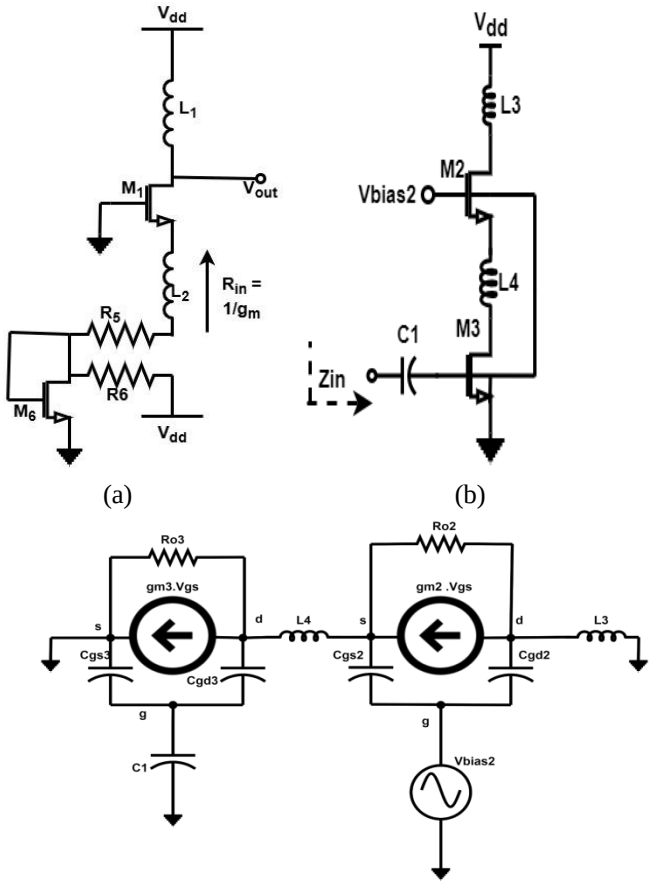


Fig. 7: (a) 1st stage of LNA (CG stage) with biasing network, (b) 2nd stage of LNA (CS stage) for noise analysis, (c) Small signal of a CS stage.

The noise factor due to termination is given by the following expression,

$$F = \frac{\text{Total power of output noise}}{\text{Total power of output noise due to source alone}}$$

$$F = 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R}; \quad (4)$$

Where, γ is the MOS transistor's coefficient of channel thermal noise and is defined as the ratio of the trans-conductance and the zero-bias drain conductance. γ is process-dependent and difficult to control, the noise performance can be optimized by increasing the trans-conductance of the MOS transistor, i.e., trading off the 50-input matching.
For first stage,

$$F = 2 + \frac{\gamma}{\alpha} + \frac{R_5 + R_{L2}}{R_{L1}}; \quad (5)$$

Where, R_{L1} is the parasitic resistance of the drain inductor L_1 and (R_5+R_{L2}) is the input source signal & R_{L2} is the parasitic resistance of the source inductor L_2.

As shown in Fig-7(b) inductively source-degraded common source topology is commonly used in wide-band LNA designs because it is a better option for concurrently achieving optimal noise and good input matching.

$$Z_{in} = \frac{g_{m_3}}{C_1 + C_{gs_3} + 2C_{gd}} L_4 + j\left[(\omega_H L_4) - \frac{1}{\omega_H (C_1 + C_{gd} + C_{gs_3})}\right] \quad (6)$$

Where, C_{gs3} represents the gate to source capacitance of M_3. By adjusting C_1, L_4, C_{gd} and C_{gs3} so that, at the input frequency, the imaginary term equals zero. It is possible to obtain a real term of 50 Ω without the need for a resistor. Moreover, it offers simultaneous power matching. It is most common to use this type of arrangement when developing narrow-band LNAs.

$$\left[(\omega_H L_4) - \frac{1}{\omega_H (C_1 + C_{gd} + C_{gs_3})}\right] = 0,$$

$$\text{So, } \omega_H = \frac{1}{\sqrt{L_4 (C_{gs_3} + C_{gd} + C_1)}}$$

$$\& \; Z_{in} = \frac{g_{m_3}}{C_1 + C_{gs_3} + 2C_{gd} L_4} = 50$$

Where,

$$C_{gs3} = \left(\frac{2}{3}\right) C_{ox} W_{opt} L_4, \quad g_{m_3} = \frac{2I_d}{V_{ov}} \; \& \; W_{opt} = \frac{1}{3\omega_H L_4 C_{ox} R_s}$$

This configuration's noise factor is determined by the following formula,

$$F = 1 + \gamma . g_m . R_s . \left(\frac{\omega_0}{\omega_T}\right)^2 \quad (7)$$

The minimum noise figure of this topology can be low.

- Transit or Cut off frequency, $\omega_T = \frac{g_{m_3}}{C_1 + C_{gs_3} + 2C_{gd}}$
- Trans-conductance g_m
- Total effective input capacitance,
  $C_T = (C_1 + C_{gs3} + 2C_{gd})$
- Drain current I_d

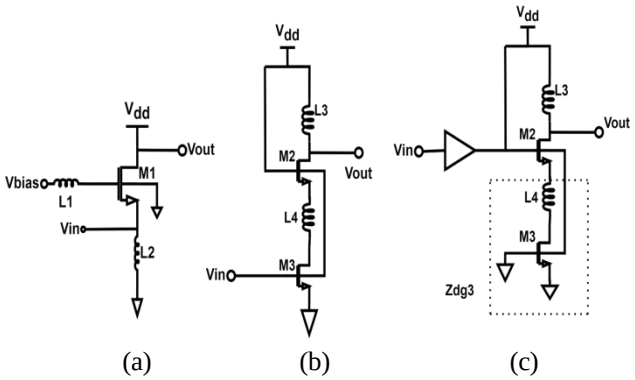
C. Gain Analysis:

The suggested wideband LNA includes a CS-CG cascaded gain-boosting stage. Decoupling the two steps, evaluating the

gain of each step separately, and then calculating the overall gain allows for the completion of the gain analysis.

The first stage gain can be calculated by using the formula,

$$A_{V1} = g_{m_1}(1-\alpha)\, Z_{L1} \quad (8)$$



(a) (b) (c)

Fig. 8: Gain analysis (a) CG stage-1, (b) CS stage-2, and (c) CG-CS cascaded stage.

Where,

$$\alpha = \frac{sC_{gs_1}p + sC_{gd_1}g_{m_1}}{pq + sC_{gd_1}(g_{m_1} - sC_{gd_1})}$$

$$Z_{L_1} = \frac{1}{s(C_{db_1} + C_{g_3})}$$

$$p = \left(\frac{1}{Z_{L_1}} + sC_{gd_1}\right)$$

$$Z_{G_1} = (sL_1 + R_{L_1}) \,||\left(\frac{1}{sC_{gb_1}}\right)$$

$$q = \left(\frac{1}{Z_{G_1}} + sC_{gs_1} + sC_{gd_1}\right)$$

We must apply the superposition concept in order to examine the second stage's gain. The CS-CG stage is depicted in Fig. 8(b) and 8(c), where the gain block A_{V_1} stands for the input CG-stage's gain. Let A_{V_2} and A_{V_3} represent the gain and the gain from the gate of M_2 and M_3 to the output, (9) and (10) provide A_{V_2} and A_{V_3}, respectively.

$$A_{V_2} = \frac{g_{m_2}Z_{L_3}}{1+g_{m_2}Z_{dg_3}} \quad (9)$$

Where,

$$Z_{dg_3} = \left(\frac{1}{sC_{sb_2}}\right) ||(sL_4 + \frac{1}{sC_{db_3} + sC_{gd_3} + \frac{1}{r_{03}}})$$

$$A_{V_3} = \left(\frac{g_{m_2}Z_{L_3}}{g_{m_2}+sC_{sb_2}+sC_{gs_2}}\right)\left(\frac{g_{m_3}}{1+sZ_3C_{db_3}}\right) \quad (10)$$

Where,

$$Z_3 = sL_4 + \frac{1}{(sC_{sb_2} + sC_{gs_2} + g_{m_2})}$$

$$Z_{L_3} = (R_{L_3} + sL_3) \,||\, (\frac{1}{sC_{db_2}})||\, Z_L$$

Z_L is the impedance of the load (mixer or variable gain amplifier (VGA)) connected to the LNA.

LNA's total gain,

$$A_V = A_{V_1}.A_{V_2} + A_{V_3} \quad (11)$$

Total forward power gain is shown in Fig. 9 indicated the larger gain, which means output power is more hundreds time larger than input power. And reverse power gain in Fig. 10. shows a value indicating good reverse isolation. A little signal is leaking backward. So this LNA is doing a great job of blocking reverse signal flow.

D. IIP3:

One crucial characteristic that shows the linearity of the amplifier is the input-referred third-order intercept point (IIP3) of an LNA. It stands for the fictitious input power level at which the basic signals' power and the power of the third-order inter-modulation products are identical. A higher IIP3 value denotes better linearity and less distortion, both of which are essential for preserving signal integrity when there are powerful interfering signals present. For many contemporary applications, particularly in cellular and wireless communications, an IIP3 of approximately +5 dBm or greater is generally preferred.

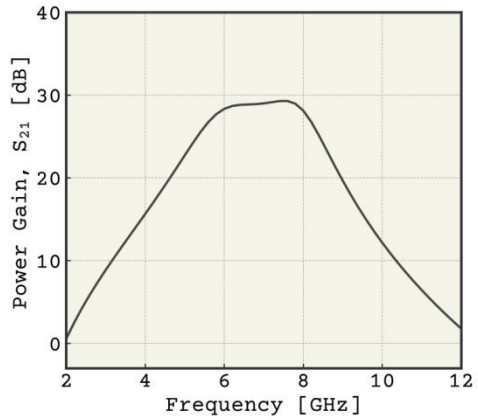


Fig. 9: Forward Gain Vs Frequency

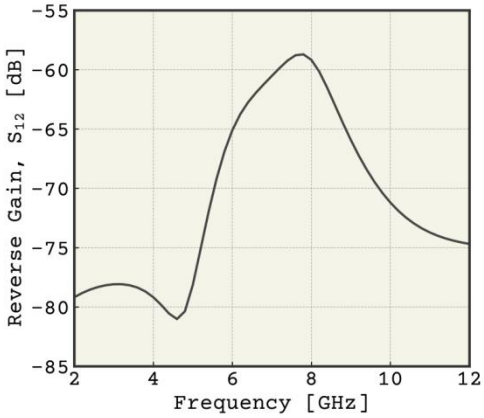


Fig. 10: Reverse gain Vs Frequency

The input referred third-order intercept point (IIP3), is shown in Fig-11. The value (One tone) is selected to test the IIP3 of the LNA. The IIP3 is found to be 21.1537 dBm in Fig. 11.

E. Stability Analysis:

Based on the input and output reflection coefficients, the stability factor—often denoted as K, or Rollet's stability factor—is used to determine whether an amplifier is unconditionally stable, conditionally stable, or perhaps unstable. To operate reliably, a larger stability factor denotes improved resilience to oscillations. The stability factor Kf can be calculated using the following formula:

$$Kf = \frac{(1-|S11|^2-|S22|^2)}{|S12\,.S21|} \quad (12)$$

As the value of Kf =10 > 1 and the B1f value > 0, shown in Fig.12 and Fig. 13 indicates the unconditionally stability which declares that the amplifier is stable within a specific range of impedances, necessitating careful design considerations.

F. Designed LNA with Attenuator:

A few traditional attenuators with series and shunt resistance adjustments use T, and bridged T topologies. By controlling the FET switches, the attenuator experiences the least amount of attenuation when the series resistance is minimal and the shunt resistances are big. In that scenario, the series switch's nonzero on-resistance is the only source of the loss at the lowest frequencies. The insertion loss resulting from the attenuator's minimum insertion decreases as this resistance decreases [31][39].

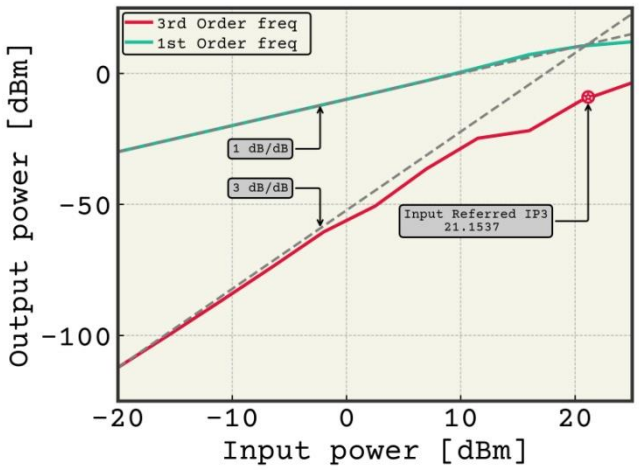


Fig. 11: Simulated IIP3

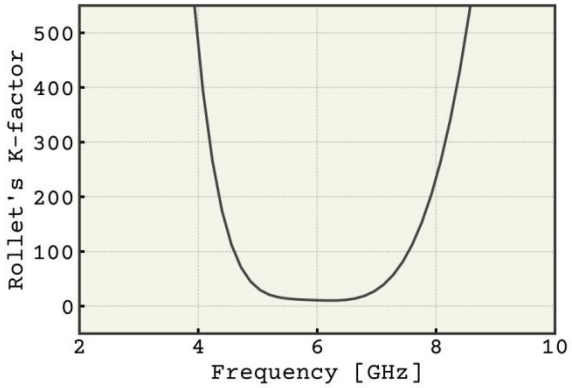


Fig. 12: Rollet's K factor Vs Frequency

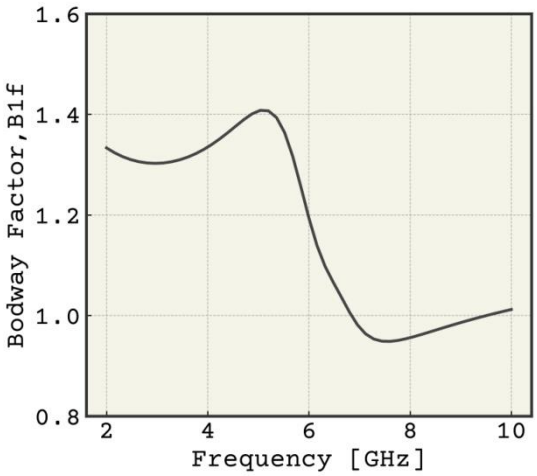


Fig. 13: Bodway factor Vs Frequency

The parasitic capacitors cause greater loss to ground at higher frequencies, hence reducing these capacitors lowers the insertion loss. Likewise, when the T-attenuator is set to minimal gain, the shunt component is off and the series components are fully on. In our analysis, π-topology displayed a wider frequency response when compared to T-topology. Furthermore, there is a trade-off between greater impedance matching and T-topology attenuator attenuation. Fig.14 displays the schematic of the suggested variable attenuator design. Five successive phases make up its single stage π -topology. Transistors ($M_{15,18}/M_{16,17}$) and resistors (3R/10R) are employed in two shunt branch pairs to enhance the attenuator's input/output impedance matching. We used S-parameter simulation to optimize the parameter; the gate width of each FET switch was set to 2 µm, and the resistance value R was set to 10 Ω [39].

TABLE II
COMPONENTS VALUE

Aspect ratio	**$(W/L)_8$~ $(W/L)_{19}$**
	2µ/100n
Inductor (nH)	**L_5**
	1

Capacitor (pF)	C_4	C_5	C_6	C_7		
	400	95	0.04	3		
Resistor (Ω)	R_8	R_9	R_{10}	R_{11}	R_{12}	R_{13}
	12	8	4	2	1	5

	R_{14}	R_{15}	R_{16}	R_{17}	R_{18}	R_{19}
	5	3	10	10	3	1.04e3

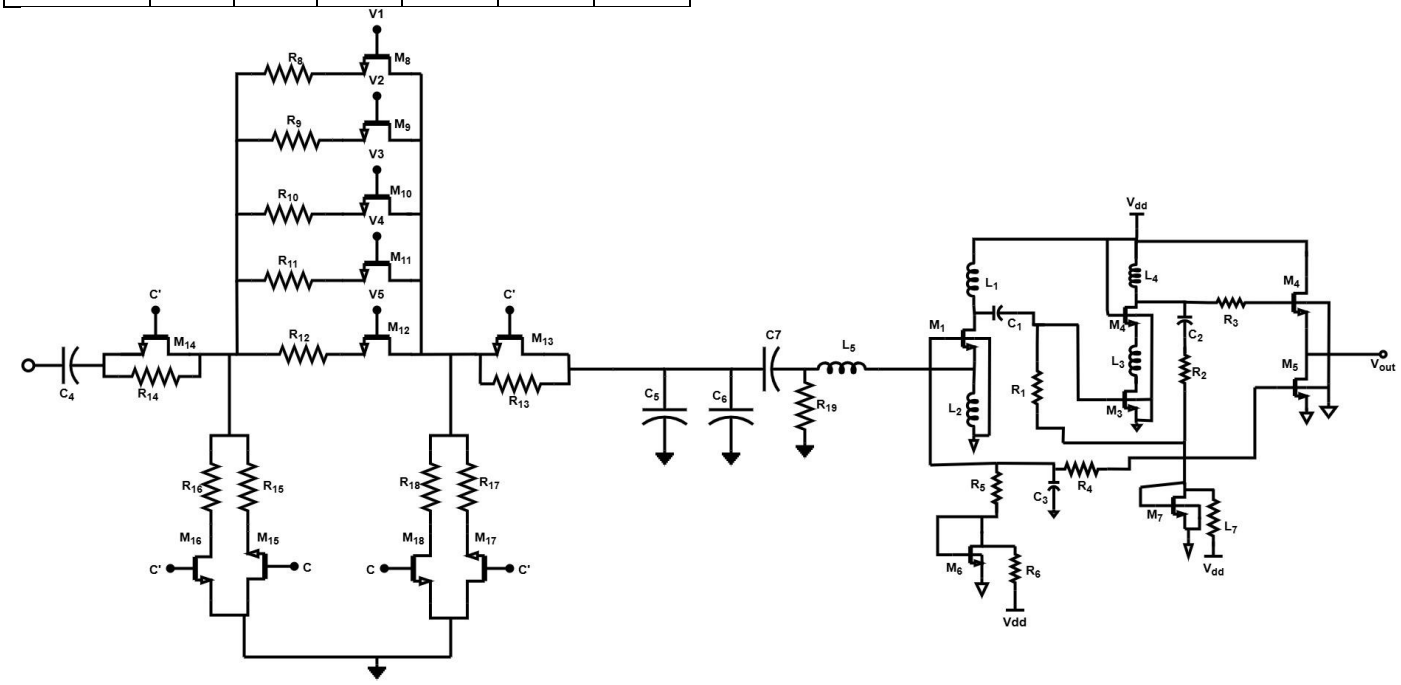


Fig. 14: Proposed LNA with 5 stages attenuator.

G. Gain Analysis of designed LNA with the attenuator:

With a straightforward shift register control bit V_c and V_c', where V_c' is the complementary of V_c , the designed attenuator offers attenuation ranging from 15.97 dB to 22.70 dB. The attenuation stages will reach a lesser attenuation state from 15.97 dB to 22.70 dB when the transistors M_{16} & M_{17} are turned on, that is when V_c is low and V_c' is high. Likewise, transistors of the five stages exhibit a higher attenuation condition from 16 dB to 22.52 dB when M_{15} to M_{18} are turned on (V_c is high and V_c' is low). Six digital control voltages are used in the suggested attenuator [39]. The digital control voltage combinations to choose the attenuation stat are displayed in Table III and the performance summaries of the proposed LNA and comparison to previously reported wideband LNAs are displayed in Table IV.

IV.SIMULATION RESULT AND DISCUSSION

The design simulations were performed using Spectre RF from the Cadence design suite. We examine the sp analysis, which mostly displays the circuit's performance in a selected position, to determine the performance analysis. S_{11}, S_{22}, S_{21}, and S_{12} represent the parameters of the SP analysis, from which we may determine the gain condition of the circuit.

Over a bandwidth of 6.6 – 8.3 GHz, there is high agreement between the simulated and measured values. The bottom band attains a noise figure of 3.4 dB, whereas the top band obtains a noise figure of 2.9 dB, according to the simulated plot in Fig. 20. A power increase of S_{21} 29.25dB is obtained at the operating frequency of 7.616 GHz with a 1.2 V power supply

TABLE III

THE GAIN OF LNA WITH THE ATTENUATOR

Control bias (H for high, L for Low)							S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)
V_1	V_2	V_3	V_4	V_5	V_c	V_c'				
H	L	L	L	L	H	L	16	-7.2	-18.4	-72

H	H	L	L	L	H	L	19.3	-9.6	-18.1	-68.4
H	H	H	L	L	H	L	20.97	-11.4	-18	-66.8
H	H	H	H	L	H	L	21.9	-12.8	-17.95	-65.9
H	H	H	H	H	H	L	22.5	-14.03	-17.9	-65.3
H	H	H	H	H	L	H	22.7	-13.5	-17.86	-65.2
H	H	H	H	L	L	H	22.2	-12.3	-17.91	-65.9
H	H	H	L	L	L	H	21.2	-11	-18	-66.8

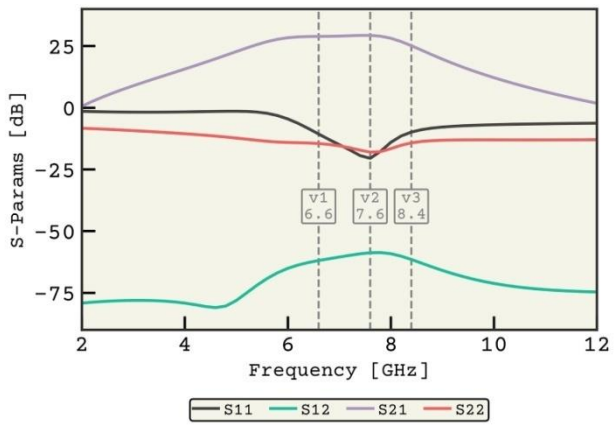


Fig. 15: Power gain (S_{21}), Input return loss (S_{11}), Output return loss (S_{22}) & Reverse gain (S_{12}) before adding attenuator.

in Fig. 16. At 7.616 GHz, the LNA's input return and output return losses (S_{11}, S_{22}) are −20.31dB and −18.01dB, respectively. The reverse isolation (S_{12}) is −58.78dB in Fig. 19, which can be attributed to the use of a cascaded structure.

The design displays that the gain may be varied from 28.85 dB at higher feet to 25.24 dB at lower feet, respectively, before using an attenuator on the input side. The nearly 2 dB bandwidth spans, respectively, and includes the lower (6.6 GHz) and higher (8.3 GHz) transit frequencies. Plots of the input return loss (S_{11}) and output return loss (S_{22}) for the upper and lower feet are shown in Fig.15, Fig.17 and Fig.18. S11 for both standards stayed well below -14 dB over the entire bandwidth. The simulated plots in Fig. 15 demonstrate that the higher ft design achieves a noise figure of 3 dB while the lower ft design reaches 2.59 dB.

Our developed circuit's gain can be easily verified from 15.97 dB to 22.7 dB over an acceptable range of bandwidth by adding an attenuator to the input side. Throughout the whole bandwidth, S_{11}'s value is also less than -17dB. Both S_{11} and S_{22} have values of -13.52 dB and -17.86 dB, respectively, at the cutoff frequency of 7.616 GHz. For the constructed circuit, the value of S_{12}, which primarily measures the reverse gain, was determined to be - 65.24 dB. Fig. 20 illustrates the suggested design's noise performance. A comparison is made between the noise values in the LNA arrangement with and without an attenuator simulation. With the gain shown in Fig. 20, the noise figure in the LNA configuration without attenuator simulation is maintained below 3 dB across the whole band. In the simulation of an LNA with an attenuator and a gain of 22.18 dB, the noise figure is less than 9.4 dB. The noise figure varies by around 0.3 dB at the low-frequency end and by 1.2 dB at the high-frequency end of the band when the gain falls to 15.98 dB. As a result, variable gain is obtained without a significant deterioration in the noise performance.

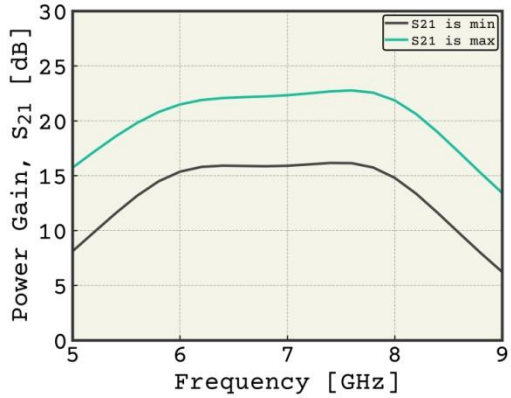


Fig. 16: Forward transmission coefficient Vs Frequency

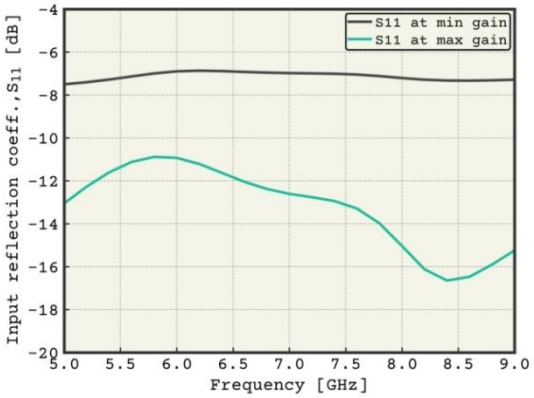


Fig. 17: Input return loss Vs Frequency

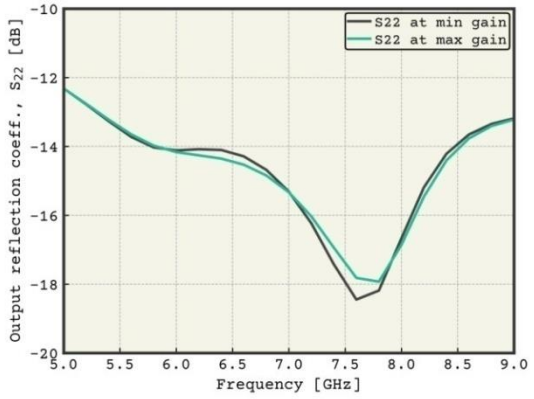


Fig. 18: Output return loss Vs Frequency

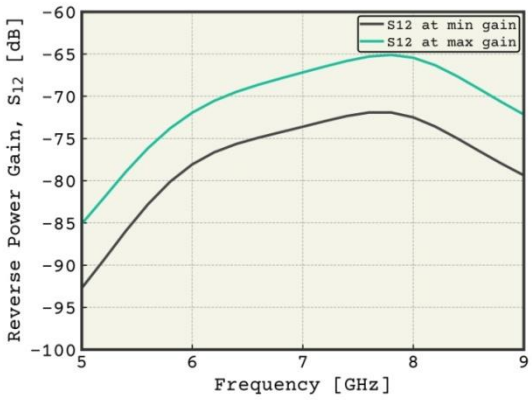


Fig. 19: Reverse Forward transmission coefficient Vs Frequency

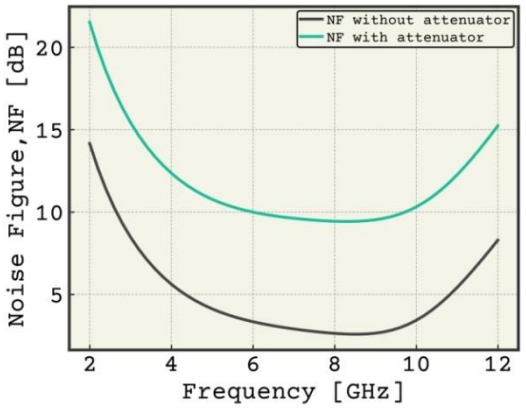


Fig. 20: Noise figure Vs Frequency

TABLE IV

PERFORMANCE SUMMARIES OF PROPOSED LNA AND COMPARISON TO PREVIOUSLY REPORTED WIDEBAND LNA

Ref.	**CMOS Tech. (nm)**	**V_{supply}**	**S21 (dB)**	**Freq. (GHz)**	**S11 (dB)**	**IIP3 (dBm)**
This Work (without attenuator)	90	1.2	29.25	7.62	-20.3	21.154
This Work (with attenuator)	90nm	1.2	15.97-22.7	7.616	–13.52 to -7.08	
[13]	180	1.8V	13	2 - 5	<-10	–9.5
[14]	90	1.2V	11.2-12.4	1.575-2.4	-25.26 to -21.4	-3.12 to -2.137
[5]	130	1.8V	17	0.05-0.83	<-8.9	-6.3
[7]	180	1.8	16.1	0.1 - 1.4	<-9	13-18.9
[39]	180	1.8V	6-24	DC-4	<-10	—

V. CONCLUSION

This paper presented a wideband LNA with integrated attenuator, designed in GPDK 90 nm CMOS technology based on CG-CS architecture which delivers maximum 22.7 dB gain and noise figure below 9.4 dB with dynamic gain control and body biasing. When the gain drops to 15.98 dB, the noise figure increases little bit. The design improves linearity, reduce noise, and enhance overall performance. Simulation in Cadence software makes the design more potential and significant for compact and tunable wideband application like the advancement of medical applications.

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