High-Performance Low Noise Amplifier for Medical Imaging: A Gain-Adjustable Solution./Gain-Tunable Low Noise Amplifier for Advanced Medical Imaging Systems./Advanced Low Noise Amplifier for Medical Imaging: A Gain-Adjustable Solution

Nishat Anjumane Salsabila
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology (CUET)
Chattogram, Bangladesh
salsabilpritu@gmail.com

Susmita Barua
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology (CUET)
Chattogram, Bangladesh
susmitarichi@gmail.com

Mohammad Mahmudul Hasan Tareq
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology (CUET)
Chattogram, Bangladesh
mmhtareq.eee@cuet.ac.bd

Quazi Delwar Hossain
Department of Electrical and Electronic Engineering
Chittagong University of Engineering and Technology (CUET)
Chattogram, Bangladesh
quazi@cuet.ac.bd

Abstract:

The purpose of this paper is to find a high gain for a wideband low noise amplifier above 6 GHz. A large gain is required by the LNA employed in this frequency range for medical imaging because it transforms low-intensity images into high-intensity images. A low noise amplifier designed with a common source and a common gate in 90nm technology is represented in this paper. With an average noise figure of < 3dB and a bandwidth of 1.7GHz from 6.6GHz to 8.3GHz, the proposed WideBand LNA achieves 29 dB power gain and extremely good impedance matching (S_{11}< -18.14dB and S_{22}< -20.23dB) at a supply voltage of 1.2V. By including an attenuator on the input side of the suggested design, a gain control mechanism is also included for the first time, all without affecting the other merits of the prior circuit.

I. INTRODUCTION

LNA is a component whose major purpose is to introduce as little noise as possible by increasing the strength of a weak signal. Low Noise Amplifiers, or LNAs, enhance the performance and efficacy of imaging systems in a number of ways, making them indispensable to the medical imaging sector. The current advancements in LNA technology make it more useful in this field. Recent advances in LNA technology have focused on improving performance metrics including gain, bandwidth, and noise figures. In conclusion, by fostering cutting-edge technologies and boosting signal quality and sensitivity, low-noise amplifiers have a large positive influence on medical imaging. Recent advances have continued to improve their performance, making them indispensable components of modern medical diagnostic and therapeutic approaches. This paper proposes a UWB LNA circuit for 90nm Cadence Technology where only one common source circuit will be used with a low supply voltage (about 1.2 V).

LNAs are crucial in the field of medical imaging because they enhance the pictures of diagnostic issues. This raises the demand for LNA circuits, thus optimization is crucial. In 90 nm technology, the design of a wideband LNA presents a significant challenge to designers since, in addition to having low power consumption, it must have flat power gain and strong linearity over the whole bandwidth [1]. Using the common gate at the initial stage of an LNA needs to meet a number of requirements over the whole bandwidth, including good linearity, low power consumption, low Noise Figure (NF), broadband input matching (S11), and flat power gain (S21) [2]. Achieving all of the above features simultaneously is a major challenge because the present techniques limit access to all of the above specifications. Common Gate (CG) is one of the input matching strategies [3][4], although the noise figure and gain are limited by the input matching condition.

A modified resistive shunt feedback LNA is suggested in [5] where it emphasizes the ability to cancel out distortion and noise. The design successfully handles problems with high 1/f noise. Ultra-wideband (UWB) LNAs, which need high data rates and low power consumption, are the main topic of [6]. Different LNA design topologies and associated difficulties are covered in the article. LNAs for RF applications are covered in [7] which makes use of a common CMOS procedure to improve circuit-level linearity. Using complementary nMOS and pMOS configurations[8] suggests a noise-cancelling CMOS LNA to improve linearity and a reduced noise figure and the result is a high third-order input intercept point. Using a gate inductor for bandwidth extension[9] discusses a resistive-feedback LNA for bandwidth extension that targets multiple wireless standards and applications and addresses challenges in traditional LNA architectures. The paper [10] presents a highly linear UWB LNA that compares performance with state-of-the-art CMOS LNAs.[11] provides insights for CMOS-based LNA design perspectives and [12] includes works on RF circuit design principles. [16] emphasizes how the resonance frequency between the receiver coil and amplifier input capacitance can restrict bandwidth, highlighting the trade-off between usable bandwidth and acceptable noise figures in MPI systems. It offers information on design factors to be taken into account for upcoming enhancements. A four-stage optimized Low Noise Amplifier (LNA) with a small configuration made possible by just two inductances in the input matching circuit is shown in [17]. It was constructed using the TSMC 0.18 μm CMOS technology. With a S_{12} parameter below -80 dB and a maximum gain of 17.5 dB, this LNA exhibits good isolation and efficient amplification of weak signals while preserving low noise levels. According to the paper, cascaded amplifiers have a high power consumption and may require greater space for the LNA design because of their numerous stages and parts. [18] concentrate on reducing input noise and power usage by optimizing bias currents using the EKV model, reducing flicker noise using PMOS input transistors, and reducing noise further without using more power by employing a switched biasing approach. With an average power consumption of 15.174 μW and a low input noise of 2.89 μVrms, demonstrating its suitability for sensitive biomedical applications. Though it highlights the effective noise reduction techniques but lacks discussion on their performance under varying environmental conditions or biomedical signals, limiting real-world applicability.

[19] details an LNA achieving a noise figure of 0.5-0.6 dB, gain > 20 dB at 63.87 MHz, and employs GaAs pHEMT for low noise and high linearity. A feedback network enhances stability contributing to improved MRI signal amplification and imaging quality for accurate diagnostics. The LNA is specifically designed

for a frequency of 63.87 MHz, which may limit its applicability to other MRI systems operating at different frequencies. [20]include optimized cascode structures, enhanced PSRR, and input impedance designs to reduce coil coupling and improve MRI sensitivity which presents CMOS LNAs with sub-1dB noise figures, achieving high gain and low noise at 437 MHz and 477 MHz for 10.3 T and 10.5 T MRI systems. It faces limitations in CMOS channel length constraints, modeling accuracy, inductor integration, and broader applicability beyond MRI systems. An optical preamplification is introduced in [22] for MR imaging but faces limitations like comparable yet suboptimal signal-to-noise ratio, narrow bandwidth, and excess noise. Though the bandwidth of the transduction is narrow compared to standard preamplifiers as a limited bandwidth can restrict the amount of data captured during imaging, potentially affecting the overall image quality and acquisition speed. [23] advances noise performance understanding for inductive sensors, presenting noise-matching techniques validated experimentally and applicable to biomedical imaging systems like MPI and low-field MRI. Even though the resistive load (R_L) may vary with frequency, especially with stranded litz wire, affecting noise-matching networks. Additionally, transformer-coupled networks achieve a maximum noise-matched bandwidth π times lower than the theoretical ideal, limiting real-world performance. [24] discusses various techniques for designing a wideband preamplifier that minimizes noise which includes considerations of bandwidth, averaging, and input stage topologies. Using N-channel JFETs in the input stage offers low noise and high gain but introduces high input capacitance, potentially lowering resonant frequencies and affecting performance. This paper explores Cascode amplifiers for low-noise MRI, achieving a noise figure of 0.45 dB, 11.6 dB gain at 32 MHz, and stability up to 6 GHz which presents a detailed design methodology focusing on DC biasing, stability, and linearity to enhance LNA reliability and performance.

In this paper, 90 nm technology is used to design an LNA circuit with the aim of getting high gain for the frequency above 5GHz. While designing there arise some problems about maintaining flat high gain and stability. As LNA made in 90nm technology often runs at lower supply voltages which reduces the gain margin and makes the circuit more noise sensitive. So the biggest challenge for us is to design a circuit with a stable high gain and balancing power consumption.

In this design, a CG-CS (Common Gate-Common Source) Cascode stage topology of LNA is used, as this topology offers higher gain and bandwidth compared to other topologies of LNA implementation. A buffer circuit is also included as output in the design as it gives better immunity against noise due to supply voltage variation [5]. In the simulation stage, the main focus is on optimizing LNA parameters like gain, bandwidth, center frequency, stability, etc. From circuit-level simulation, the gain is found to be around 29.28 dB with a center frequency of 7.6GHz with a bandwidth of around 2GHz. This output shows a better result than the previous paper. Besides the circuit has only one common source stage which makes the whole circuit lighter than the previous work. In a word, it can be said that this design promises to bring out a highly effective LNA system through the process of further development in the medical imaging sector. Since the low noise amplifier is a crucial component of the receiver chain, it is important to carefully select and analyze the appropriate metrics to accurately describe its performance. The general ideas covered in this part are crucial for the study and design of low-noise amplifiers.

Traditional variable gain amplifiers (VGAs) and variable FET attenuators are suitable options for accurate gain adjustment. In general, variable gain amplifiers (VGAs) are moved away from their ideal linearity bias point by their gain tuning mechanism, which calls for a change in the bias voltage or current. A CMOS VGA's linearity performance typically falls short of the necessary requirements unless it uses tens or even hundreds of milliwatts of power[6]. However, because their power consumption comes mostly from the control blocks and is largely independent of their linearity performance, attenuators are great choices for controlling huge signals[7][8]. As in medical imaging applications, we need a variable range of gain to control the quality of the image, a wideband variable attenuator is crucial for a low noise amplifier circuit.

This paper is organized as follows: At first, it describes the design of the proposed low-noise amplifier circuit and its analysis and for the next part it describes the design of an attenuator circuit in the input part of the previously designed LNA circuit and its performance.

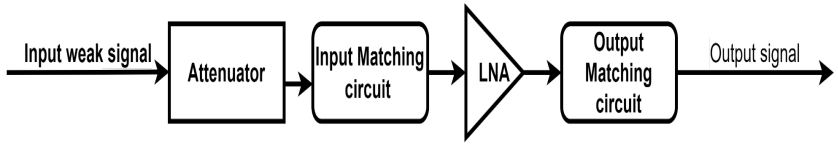


Fig-01: Block Diagram of the proposed design

II. METHODOLOGY

A. Proposed LNA design:

The design of wideband LNA becomes extremely challenging when analog and RF circuits operating in the subthreshold zone display increased thermal noise, poorer bandwidth, and poor linearity, even while subthreshold biasing gives better g_m/I_D compared to strong inversion. Our suggested LNA provides high linearity, a broad bandwidth, a modest gain, and a reasonable noise figure. To guarantee optimum performance, a number of crucial elements (such as frequency range, gain, noise figure, input/output impedance, and power consumption) must be taken into account when constructing a Low Noise Amplifier (LNA). We have first established the operational frequency range of 6.8 GHz to 8.3 GHz. A common gate (CG) stage and a CS-CG stage with a gain-boosted, source follower buffer circuit are both included in the proposed LNA. The component values are summarized in Table 1.

The common gate amplifier circuit is utilized as a first stage because it offers superior input matching, low noise performance, and enhanced linearity. The load on the CG stage is inductive (L_1). The CG-CS stage is included as the common source amplifier maintains low noise levels, supplies the required gain, and permits design modifications to satisfy particular operational needs. By resonating with M_2's total capacitance at the drain, the CS-CG stage load L_3 offers shunt peaking, improves the low-frequency gain which controls the peak at resonance, and expands the bandwidth. In order to match and measure the output, a source follower buffer is introduced. After measurement, the buffer's influence must be eliminated in order to extract the LNA's performance alone from the entire circuit.

B. Designing method:

This study will be a simulation-based study using the Cadence Virtuoso 90nm technology Software, with component values (resistors, inductors, and capacitors) determined by a suitable matching network. An appropriate matching network will be used to estimate the values of the component values, which include resistors, inductors, and capacitors. To get optimum power

transmission, matching networks are utilized to match the impedance from gate to source and source to load. We may compute the input and output impedance values first using simulation tools. Subsequently, the suitable network topology will be chosen; transformer-linked networks, π-networks, and L-networks are instances of common topologies. The performance of the matching network is analyzed by simulation, with a special focus on bandwidth, gain, efficiency, and return loss. If the performance is not up to par, the design can be repeated numerous times by varying the component value or topology until the intended outcome is achieved.

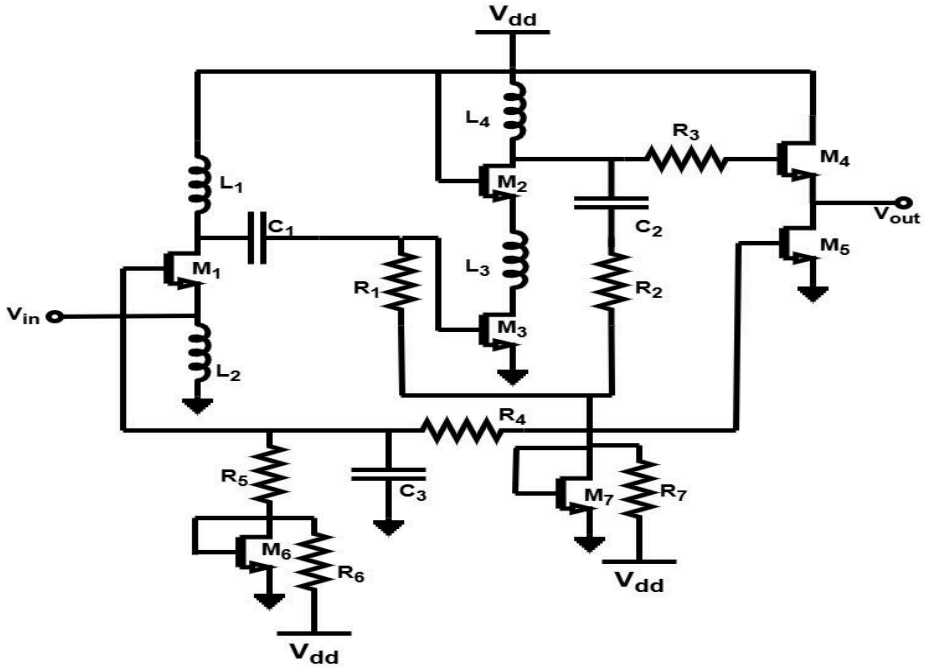


Fig-2: Schematic of the proposed wideband low noise amplifier (with biasing circuit).

TABLE - 1: Components values

i) Aspects Ratio:

$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$	$(W/L)_5$	$(W/L)_6$	$(W/L)_7$
$\frac{57u}{100n}$	$\frac{120u}{100n}$	$\frac{60u}{100n}$	$\frac{30u}{100n}$	$\frac{60u}{100n}$	$\frac{60u}{100n}$	$\frac{60u}{100n}$

ii) Inductors value:

L_1	L_2	L_3	L_4
3.1nH	1nH	5.3nH	3.5nH

iii) Capacitors value:

C_1	C_2	C_3
5pF	7pF	60pF

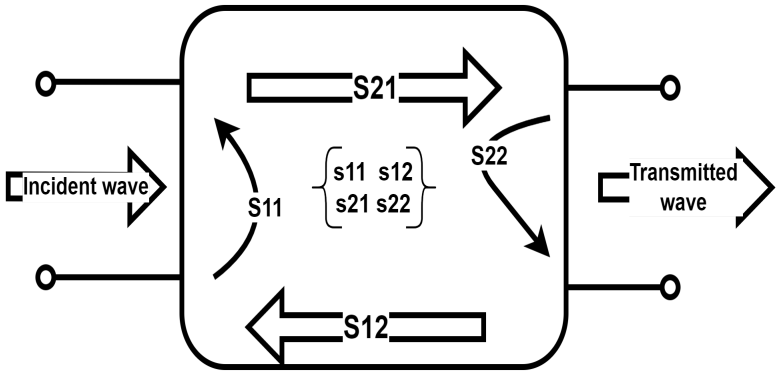
iv)Resistors value:

R_1	R_2	R_3	R_4	R_5	R_6	R_7
400Ω	**15KΩ**	**1KΩ**	**50Ω**	**500Ω**	**50Ω**	**40Ω**

III. PERFORMANCE ANALYSIS

1. Input matching: Characterizing the impedance and admittance of a two-port network operating at low frequencies often involves using the impedance matrix (Z parameters) and admittance matrix (Y parameters). However, these two approaches are insufficient for a network that operates at high frequencies. S-parameter analysis or scattering can be used instead. In this instance, the S-parameter

matrix provides the link between the incident power waves that are reflected and the S-parameter matrix[9].



Let, a_1 and a_2 are incident waves; b_1 and b_2 are transmitted waves. Using a two-port network in s-parameter analysis,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

The Equation Representation Of The Matrix is as follows:

$b_1 = S_{11}a_1 + S_{12}a_2$, $\quad b_2 = S_{21}a_1 + S_{22}a_2$,

$S_{11} = \frac{b_1}{a_1}$(when $a_2 = 0$), $\quad S_{12} = \frac{b_1}{a_2}$(when $a_1 = 0$),

$S_{21} = \frac{b_2}{a_1}$(when $a_2 = 0$), $\quad S_{11} = \frac{b_1}{a_1}$(when $a_2 = 0$),

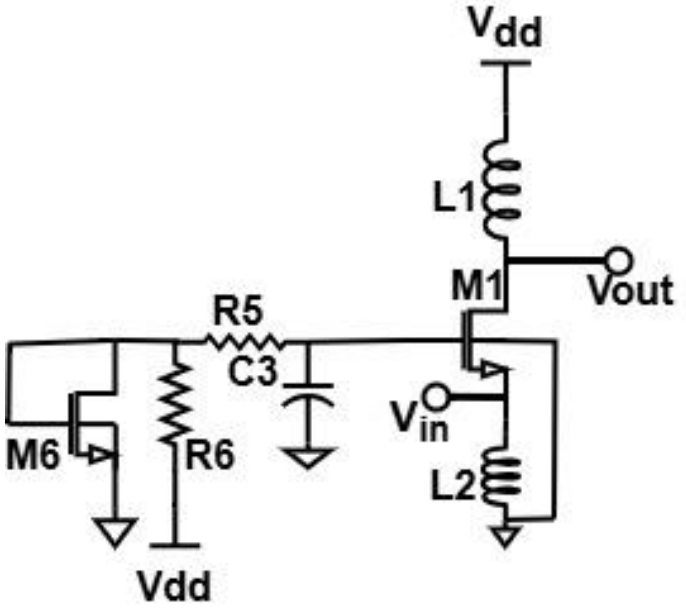
where,

- S_{11} is the input port voltage reflection coefficient, (S_{11}=$|Z_{in} - Z_s|/|Z_{in} + Z_s|$)
- S_{12} is the reverse voltage gain
- S_{21} is the forward voltage gain
- S_{22} is the output port voltage reflection coefficient

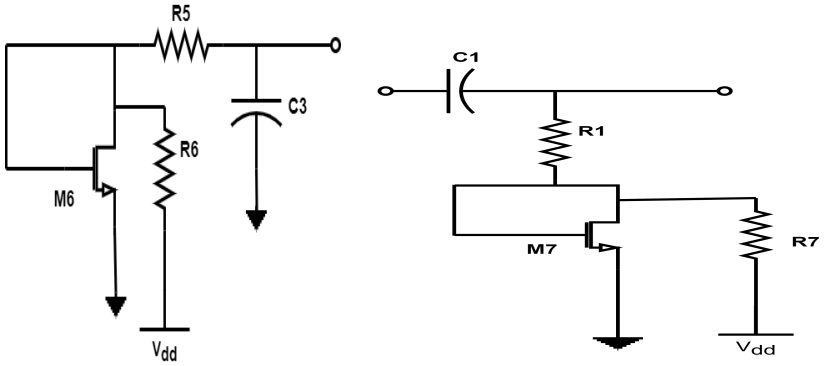
The ratio of the reflected signal to the incident signal is the reflection coefficient[14].

Impedance matching can be done in various ways.

A wideband CG-LNA's input matching is achieved by setting its transconductance to g_m=$1/R_s$, where R_s = 50Ω represents the source impedance. To ensure that mismatching issues are kept to a minimum, the LNA's input must be matched to 50Ω. Finding the right methods is necessary to obtain a 50Ω input impedance. Additionally, since impedance is purely real, a 50Ω impedance match also permits a simultaneous conjugate power match. resulting in the best possible power transmission and meeting the system requirements.



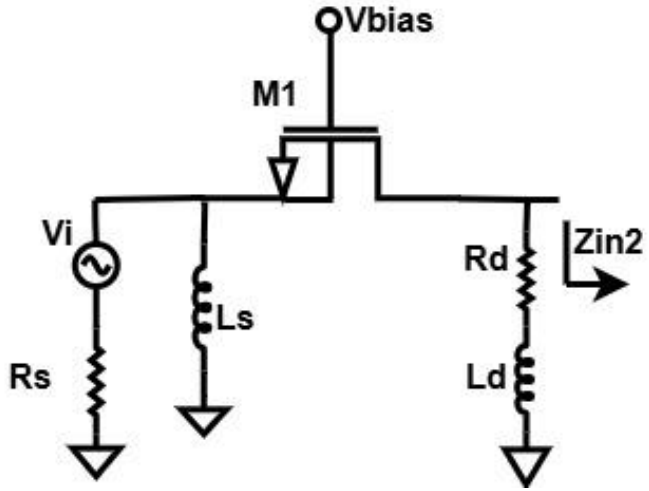
(a)



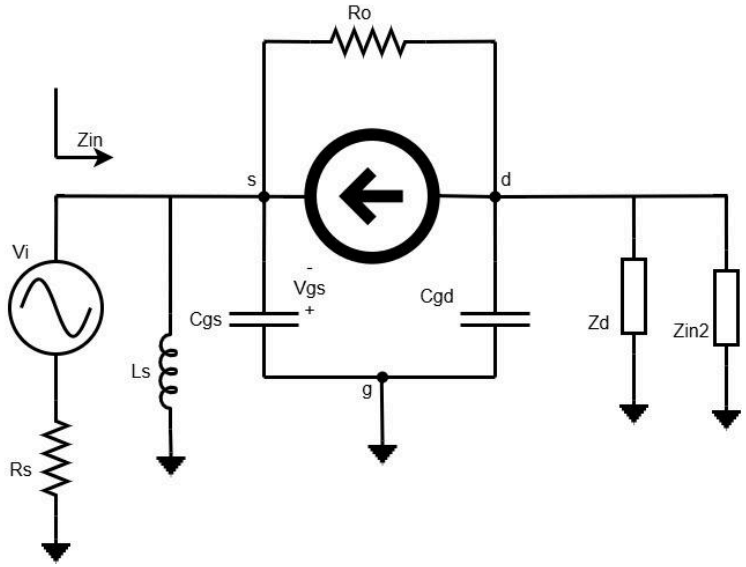
(b) (c)

Fig-3: (a) 1st stage of LNA(Common gate stage), (b) Biasing network for CG stage, (c) Intermatching network (RC network) between CG- stage and CS-stage.

The small-signal equivalent circuit for the impedance calculation,[15].



(a)



(b)

Fig-4: (a) Configuration of a Common gate input stage, (b)Small signal in common gate

Here, Z_d is the impedance of the load, Z_{in2} is the input impedance of the next stage, and g_{m1} is the transconductance of the MOS transistor in common-gate configuration[15].

Now,

$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Zs} + \frac{1-gm1.Zo}{Ro+Zo}} \quad \text{.....(1)}$$

where,

$$Z_s = j\omega L_s \;||\; \frac{1}{j\omega C_{gs}} \;\; \& \quad \text{.....(2)}$$

$$Z_o = \frac{1}{j\omega C_{gd}} \,||\, Z_d \,||\, Z_{in2} \;; \quad \text{.....(3)}$$

Based on the aforementioned deductions, the following observations can be made: Due to the frequency-dependent Z_s dominating the imaginary component in the denominator, or the

impedance of the LC tank created by L_s and C_{gs}, the common-gate stage's unsatisfactory matching occurs throughout the band. To provide a good matching throughout the broadband, L_s and C_{gs} should be selected so that they resonate close to the center of the 6.6–8.3 GHz band, leaving just a 50–real input impedance.

The best input matching over the given bandwidth is found in a MOS transistor with an aspect ratio of 57u/100n and L_s = 1nH, according to simulations.

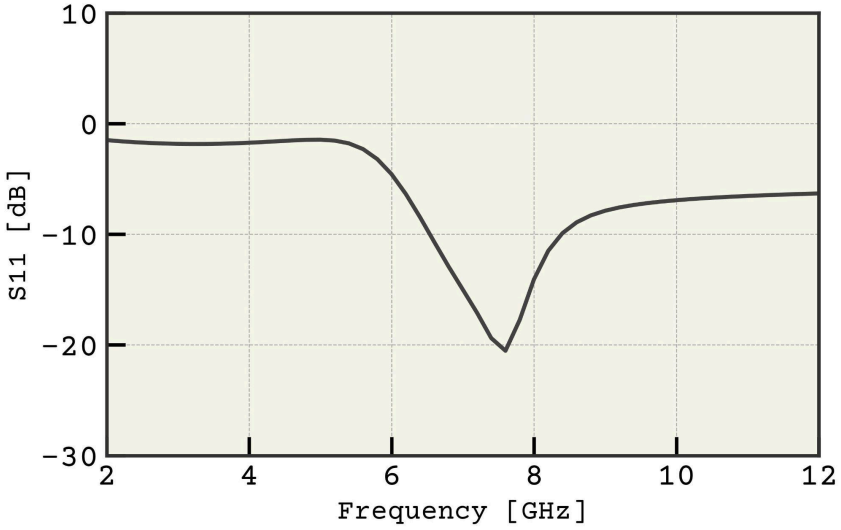


Fig-5: Input return loss vs Frequency

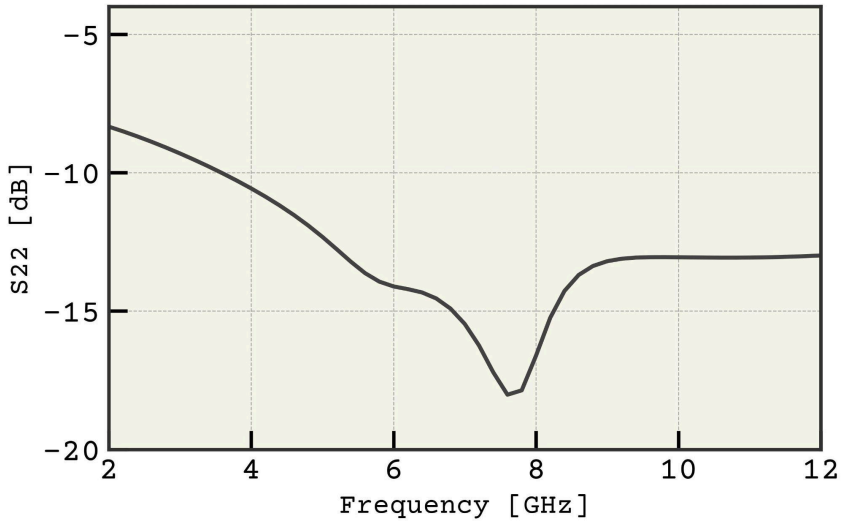


Fig-6:Output return loss vs Frequency

2. Noise Analysis:

An LNA's noise performance is directly correlated with the matching of its input. Since the noise performance of wide-band input matching cannot be tuned for a particular frequency, it is inherently noisier than its narrow-band cousin. Therefore, it is important to carefully consider and make a decision regarding the strict trade-off between the wide-band input matching and the noise figure of the wideband Low Noise Amplifier.

i)

It should be clear that the first stage amplifier's noise factor directly adds. However, in the later stages, it should be intuitively appealing that the source noise has already been gained up to that point. The noise factor is degraded by a factor of the total gain products up to that point when compared to the noise generated by the preceding system along with the already gained source noise.

The critical important data regarding a system's noise performance is contained in the Noise Figure (Noise Factor). Noise Factor (F) is another name for Noise Figure (NF). The partnership is as follows:

NF is equal to 10 $*log_{10}$ (F).

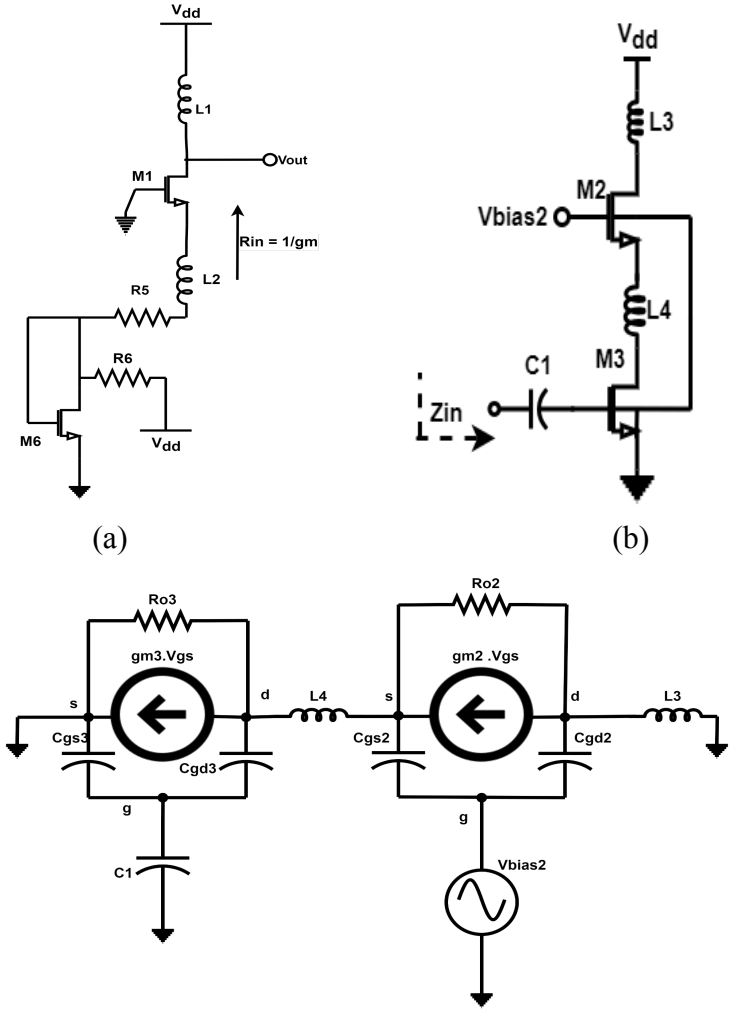


Fig-7: (a) 1st stage of LNA(Common gate stage) with biasing network,(b) 2nd stage of LNA(Common source stage) for noise analysis, (c) Small signal in common source.

The noise factor due to termination is given by the following expression,

$$F = \frac{Total\ power\ of\ output\ noise}{Total\ power\ of\ output\ noise\ \ due\ to\ source\ alone}$$

$$F = 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R}\ ; \qquad \text{.....(4)}$$

Where, γ is the MOS transistor's coefficient of channel thermal noise and α is defined as the ratio of the transconductance and the zero-bias drain conductance. γ is process-dependent and difficult to control, the noise performance can be optimized by increasing the transconductance of the MOS transistor, i.e., trading off the 50-input matching.

For first stage , $F = 1 + \frac{\gamma}{\alpha} + 4\frac{R_5 + R_{L2}}{R_{L1}}$; .....(5)

where, R_{L1} is the parasitic resistance of the drain inductor L_1 and ($R_5 + R_{L2}$) is the input source signal & R_{L2} is the parasitic resistance of the source inductor L_2.

ii)

As shown in Fig-7(b) inductively source-degraded common source topology is commonly used in narrow-band LNA designs because it is a better option for concurrently achieving optimal noise and good input matching.

$$Z_{in} = \frac{g_{m3}}{C_1 + C_{gs3} + 2C_{gd}} \times L_4 + j[(\omega_H L_4) - \frac{1}{\omega_H (C_1 + C_{gd} + C_{gs3})}] \text{ .....(6)}$$

where, C_{gs2} represents the gate to source capacitance of M_2. By adjusting C_1, L_4, C_{gd2} and C_{gs2} so that, at the input frequency, the imaginary term equals zero. It is possible to obtain a real term of 50 Ω without the need for a resistor. Moreover, it offers

simultaneous power matching. It is most common to use this type of arrangement when developing narrow-band LNAs.

$$[(\omega_H L_4) \; - \; \frac{1}{\omega_H(C_{gs3}+C_{gd}+C_1)}] = 0,$$

$$\text{so, } \omega_H = \frac{1}{\sqrt{L_4(C_{gs3}+C_{gd}+C_1)}}$$

$$\& \; Z_{in} = \frac{g_{m3}}{C_1+C_{gs3}+2C_{gd}} \times L_4 = 50\Omega \quad \text{where,}$$

$$C_{gs3} = \frac{2}{3} C_{ox} W_{opt} L_4, \quad g_{m3} = \frac{2I_d}{V_{ov}} \; \& \; W_{opt} = \frac{1}{3\omega_H L_4 C_{ox} R_s}$$

This configuration's noise factor is determined by the following formula,

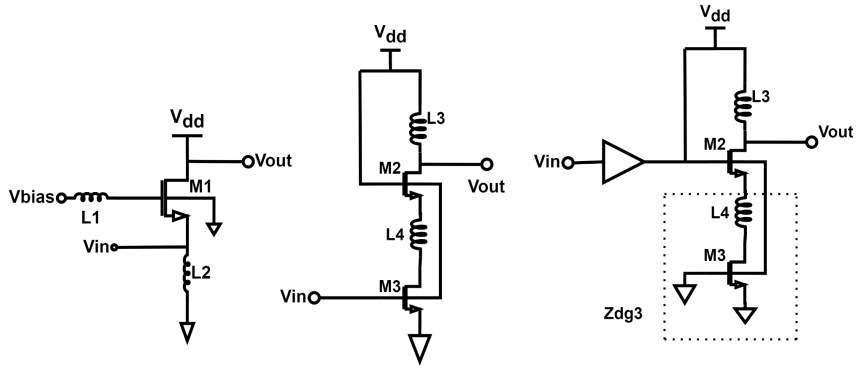
$$F = 1 + \gamma g_m R_s (\omega_o/\omega_T)^2 \qquad \text{.....(7)}$$

The minimum noise figure of this topology can be low.

- Transit or Cut off frequency, $\omega_T = \frac{g_{m3}}{C_1+C_{gs3}+2C_{gd}}$
- Transconductance g_m
- Total effective input capacitance, $C_T = (C_1 + C_{gs3} + 2C_{gd})$
- Drain current I_d

3. Gain Analysis:

The suggested wideband LNA includes a CG stage and a CS-CG current-reused gain-boosting stage. Decoupling the two steps, evaluating the gain of each step separately, and then calculating the overall gain allows for the completion of the gain analysis[13].



(a) (b) (c)

Fig-8: Gain analysis (a) CG stage-1, (b) CS stage-2, and (c) CG stage-2.

The first stage gain can be calculated by using the formula,

$$A_{V1} = g_{m1}(1-\alpha)Z_{L1} \qquad \text{.....(8)}$$

where,

$$\alpha = \frac{sCgs1p+sCgd1gm1}{p \cdot q+sCgd1(gm1-sCgd1)},$$

$$Z_{L1} = [s(C_{db1}+C_{g3})]^{-1}$$

$$p = (1/Z_{L1}+sC_{gd1}),$$

$$Z_{G1} = (sL_1+R_{L1}) \| (1/sC_{gb1})$$

$$q = (1/Z_{G1}+sC_{gs1}+sC_{gd1}),[15]$$

We must apply the superposition concept in order to examine the second stage's gain.

The CS-CG stage is depicted in Fig-8(b) and 8(c), where the gain block, A_{V1} stands for the input CG-stage's gain. Let A_{V2} and A_{V3} represent the gain and the gain from the gate of M_2 and M_3 to the output, equation (9) and (10) provide A_{V2} and A_{V3}, respectively.

$$A_{V2} = \frac{g_{m2} Z_{L3}}{1 + g_{m2} Z_{dg3}}; \quad \text{.....(9)}$$

where,

$$Z_{dg3} = (1/sC_{sb2}) \| (sL_4 + 1/(sC_{db3} + sC_{gd3} + 1/r_{03})).$$

$$A_{V3} = \left(\frac{g_{m2} Z_{L3}}{g_{m2} + sC_{sb2} + sC_{gs2}}\right) \left(\frac{g_{m3}}{1 + sZ_3 C_{db3}}\right); \quad \text{.....(10)}$$

where,

$$Z_3 = sL_4 + 1/(sC_{sb2} + sC_{gs2} + g_{m2}) \quad \&$$

$$Z_{L3} = (R_{L3} + sL_3) \| (1 / sC_{db2}) \| Z_L,$$

Z_L is the impedance of the load (mixer or variable gain amplifier (VGA))connected to the LNA.

LNA's total gain. $A_v = A_{V1} \cdot A_{V2} + A_{V3}$ .....(11)

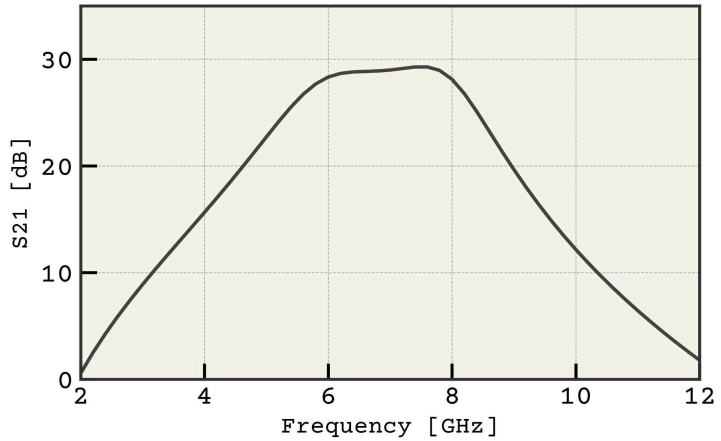


Fig-9:Insertion loss (attenuation gain) vs Frequency

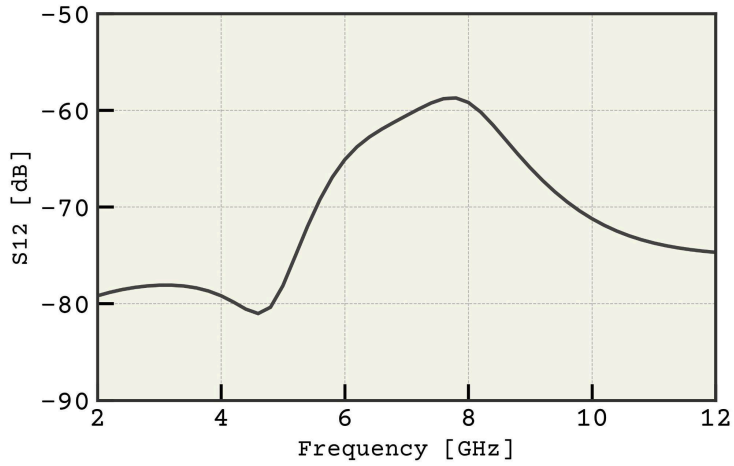


Fig-10: Reverse gain vs Frequency

4. IIP3:

One crucial characteristic that shows the linearity of the amplifier is the input-referred third-order intercept point (IIP3) of an LNA. It stands for the fictitious input power level at which the basic signals' power and the power of the third-order intermodulation products are identical. A higher IIP3 value in RF and communication systems denotes better linearity and less distortion, both of which are essential for preserving signal integrity when there are powerful interfering signals present. For many contemporary applications, particularly in cellular and wireless communications, an IIP3 of approximately +5 dBm or greater is generally preferred.

The input referred third-order intercept point (IIP3), is shown in Fig-11. The value (One tone 2 GHz) is selected to test the IIP3 of the LNA. The IIP3 is found to be 21.1537 dBm.

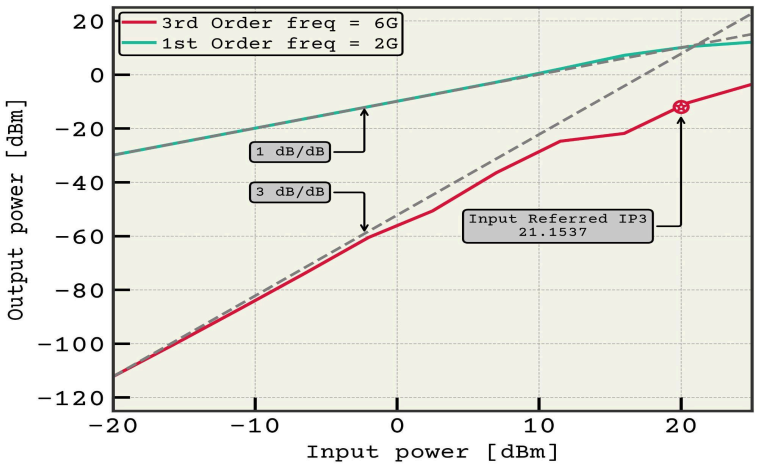


Fig-11: Simulated IIP3

5. Stability Analysis:

Based on the input and output reflection coefficients, the stability factor—often denoted as K, or Rollet's stability factor—is used to determine whether an amplifier is unconditionally stable, conditionally stable, or perhaps unstable. For RF applications to operate reliably, a larger stability factor denotes improved resilience to oscillations. The stability factor K_f can be calculated using the following formula:

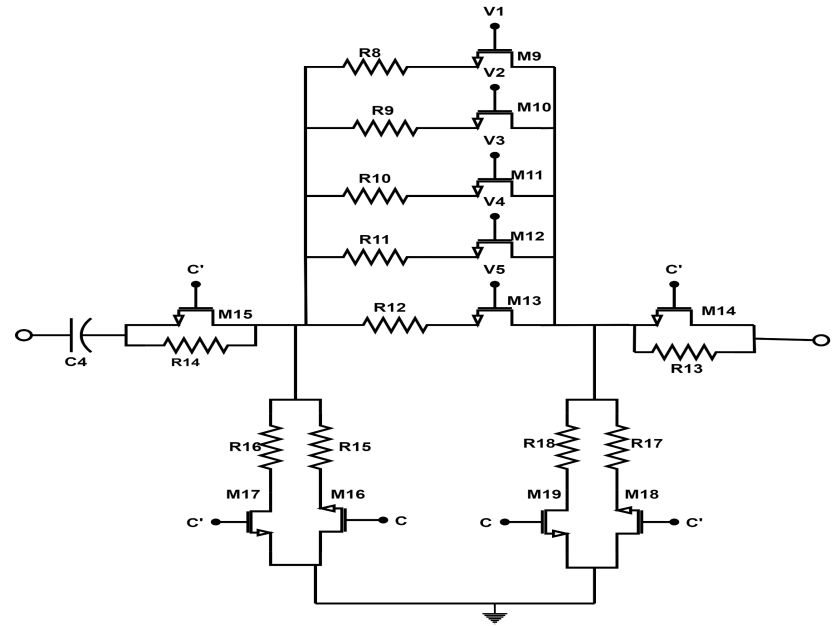
$$K_f = \frac{(1 - |S_{11}|^2 - |S_{22}|^2)}{|S_{12} . S_{21}|} \quad \text{.....(12)}$$

As the value of $K_f < 1$, so conditionally stable which declares that the amplifier may only be stable within a specific range of impedances, necessitating careful design considerations.

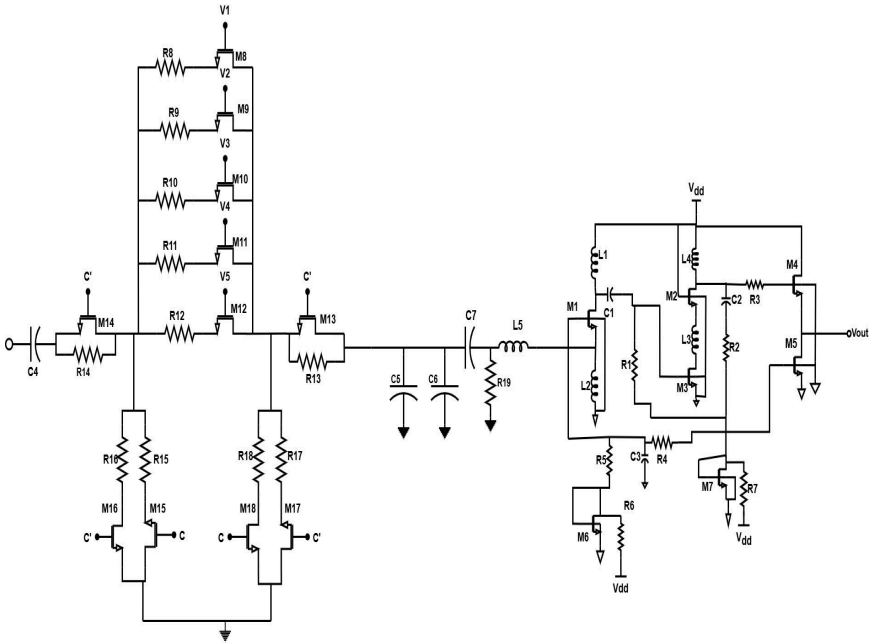
C. Designed LNA with Attenuator:

A few traditional attenuators with series and shunt resistance adjustments use T,Π and bridged T topologies. By controlling the FET switches, the attenuator experiences the least amount of attenuation when the series resistance is minimal and the shunt resistances are big. In that scenario, the series switch's nonzero on-resistance is the only source of the loss at the lowest frequencies. The insertion loss resulting from the attenuator's minimum insertion decreases as this resistance decreases[31][39].

The parasitic capacitors cause greater loss to ground at higher frequencies, hence reducing these capacitors lowers the insertion loss. Likewise, when the T-attenuator is set to minimal gain, the shunt component is off and the series components are fully on. In our analysis, Π-topology displayed a wider frequency response when compared to T-topology. Furthermore, there is a trade-off between greater impedance matching and T-topology attenuator attenuation. Therefore, we decided on the topology. Fig-1(a) displays the schematic of the suggested variable attenuator design. Five successive phases make up its single stage Π-topology. Transistors ($M_{15,18}/M_{16,17}$) and resistors (3R/10R) are employed in two shunt branch pairs to enhance the attenuator's input/output impedance matching. We used S-parameter simulation to optimize the parameter; the gate width of each FET switch was set to 2 μm, and the resistance value R was set to 10 Ω [39].



(a)



(b)

Fig-12: (a) Attenuator with 5 stages, added with proposed LNA; (b) Proposed LNA with attenuator.

i) Aspects Ratio:

$(W/L)_8 \sim (W/L)_{19}$
$\frac{2u}{100n}$

ii)Inductors value:

L_5
1nH

iii) Capacitors value:

C_4	C_5	C_6	C_7
400pF	95pF	40fF	3pF

iv)Resistors value:

R_8	R_9	R_{10}	R_{11}	R_{12}	R_{13}
12Ω	**8 Ω**	**4Ω**	**2Ω**	**1Ω**	**5Ω**
R_{14}	R_{15}	R_{16}	R_{17}	R_{18}	R_{19}
5Ω	**3Ω**	**10Ω**	**10Ω**	**3Ω**	**1.04K Ω**

Gain Analysis of designed LNA with the attenuator:

With a straightforward shift register control bit V_c and V_c', where V_c' is the complementary of V_c, the designed attenuator offers attenuation ranging from 15.97 dB to 22.70 dB. The attenuation stages will reach a lesser attenuation state from 15.97 dB to 22.70 dB when the transistors M_{16} & M_{19} are turned off, that is when V_c is low and V_c' is high. Likewise, transistors of the five stages exhibit a higher attenuation condition from 16 dB to 22.52 dB when M_{17} to M_{18} are turned 0ff (V_c is high and V_c' is low). Six digital control voltages are used in the suggested attenuator[39]. The digital control voltage combinations to choose the attenuation stat are displayed in Table 2 and the performance summaries of the proposed LNA and comparison to previously reported wideband LNAs are displayed in Table 3.

TABLE - 2: The gain of LNA with the attenuator

Control bias							Attenuation S21 (dB)	S11 (dB)	S22 (dB)	S12 (dB)
V_1	V_2	V_3	V_4	V_5	V_c	V_c'				
High	Low	Low	Low	Low	High	Low	16	-7.19	-18.43	-72
High	High	Low	Low	Low	High	Low	19.34	-9.58	-18.1	-68.44
High	High	High	Low	Low	High	Low	20.97	-11.39	-18	-66.8
High	High	High	High	Low	High	Low	21.91	-12.83	-17.95	-65.87
High	High	High	High	High	High	Low	22.52	-14.03	-17.9	-65.26
High	High	High	High	High	Low	High	22.70	-13.52	-17.86	-65.24
High	High	High	High	Low	Low	High	22.15	-12.31	-17.91	-65.88
High	High	High	Low	Low	Low	High	21.23	-10.99	-18	-66.79
High	High	Low	Low	Low	Low	High	19.63	-9.30	-18.16	-68.39
High	Low	Low	Low	Low	Low	High	15.97	-7.08	-18.34	-71.93

TABLE-3: Performance summaries of the proposed LNA and comparison to previously reported wideband LNAs.

Reference	CMOS Tech. (nm)	Supply Voltage	Gain (dB)	Frequency (GHz)	S_{11} (dB)	S_{12} (dB)	S_{22} (dB)	IIP3 (dBm)
This Work (without attenuator)	90	1.2V	29.25	7.616	-20.31	-58.78	-18.01	21.1537
This Work (with attenuator)	90nm	1.2V	15.97 -22.7	7.616	–13.52 to -7.08	-71.93 to -65.24	-18.34 to -17.86	
[13]	180	1.8V	13	2 - 5	<-10	—-	—--	−9.5
[14]	90	1.2V	11.2-12.4	1.575-2.4	-25.26 to -21.4	—---	—---	-3.12 to -2.137
[5]	130	1.8V	17	0.05-0.83	<-8.9	—--	<-8.5	-6.3
[7]	180	1.8	16.1	0.1 - 1.4	<-9	—---	—---	13-18.9
[39]	180	1.8V	6-24	DC-4	<-10	—	—--	—----

Simulation Results And Discussions

The design simulations were performed using Spectre RF from the Cadence design suite.

We examine the sp analysis, which mostly displays the circuit's performance in a selected position, to determine the performance

analysis. S_{11}, S_{22}, S_{21}, and S_{12} represent the parameters of the SP analysis, from which we may determine the gain condition and the stability factor of the circuit.

Over a bandwidth of 6.6 – 8.3 GHz, there is high agreement between the simulated and measured values. The bottom band attains a noise figure of 3.4 dB, whereas the top band obtains a noise figure of 2.9 dB, according to the simulated plot in Figure 6. A power increase of S_{21} 29.25dB is obtained at the operating frequency of 7.616 GHz with a 1.2 V power supply. At 7.616 GHz, the LNA's input return and output return losses (S_{11}, S_{22}) are −20.31dB and −18.01dB, respectively. The reverse isolation(S_{12}) is −58.78dB, which can be attributed to the use of a cascaded structure.

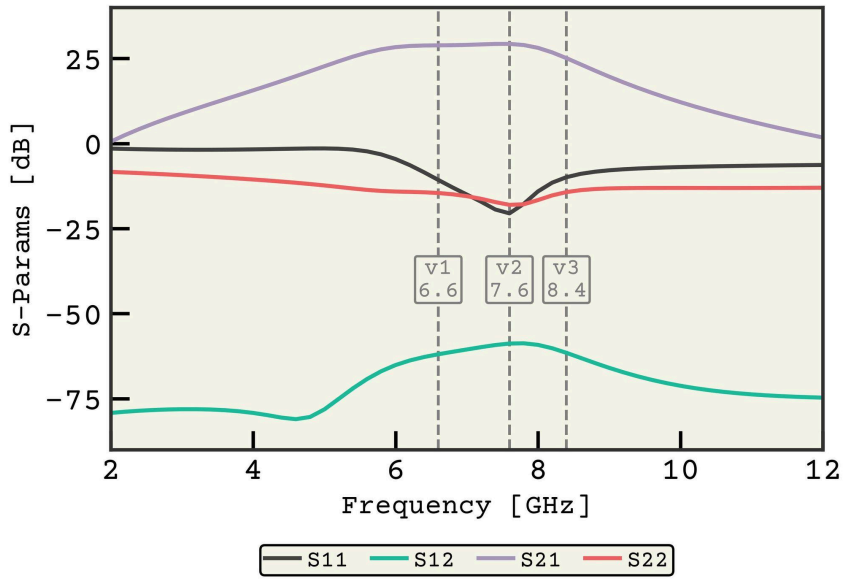


Fig- 13: Insertion loss(Attenuation Gain)(S21), Input return loss(S11),Output return loss(S22) & Reverse gain(S12) before adding attenuator.

The design displays that the gain may be varied from 28.85 dB at higher feet to 25.24 dB at lower feet, respectively, before using an attenuator on the input side. The nearly 2 dB bandwidth spans, respectively, and includes the lower (6.6 GHz) and higher (8.3 GHz) transit frequencies. Plots of the input return loss (S_{11}) and output return loss (S_{22}) for the upper and lower feet are shown in Figure 6. S_{11} for both standards stayed well below -14 dB over the entire bandwidth. The simulated plots in Figure-6 demonstrate that the higher ft design achieves a noise figure of 3 dB while the lower ft design reaches 2.59 dB.

Our developed circuit's gain can be easily verified from 15.97 dB to 22.7 dB over an acceptable range of bandwidth by adding an attenuator to the input side. Throughout the whole bandwidth, S_{11}'s value is also less than -17dB. Both S_{11} and S_{22} have values of -13.52 dB and -17.86 dB, respectively, at the cutoff frequency of 7.616 GHz. For the constructed circuit, the value of S_{12}, which primarily measures the reverse gain, was determined to be - 65.24 dB.

Figure 11 illustrates the suggested design's noise performance. A comparison is made between the noise values in the LNA arrangement with and without an attenuator simulation. With the gain shown in Figure 11, the noise figure in the LNA configuration without attenuator simulation is maintained below 3 dB across the whole band. In the simulation of an LNA with an attenuator and a gain of 22.18 dB, the noise figure is less than 9.4 dB. The noise figure varies by around 0.3 dB at the low-frequency end and by 1.2 dB at the high-frequency end of the band when the gain falls to 15.98 dB. As a result, variable gain is obtained without a significant deterioration in the noise performance.

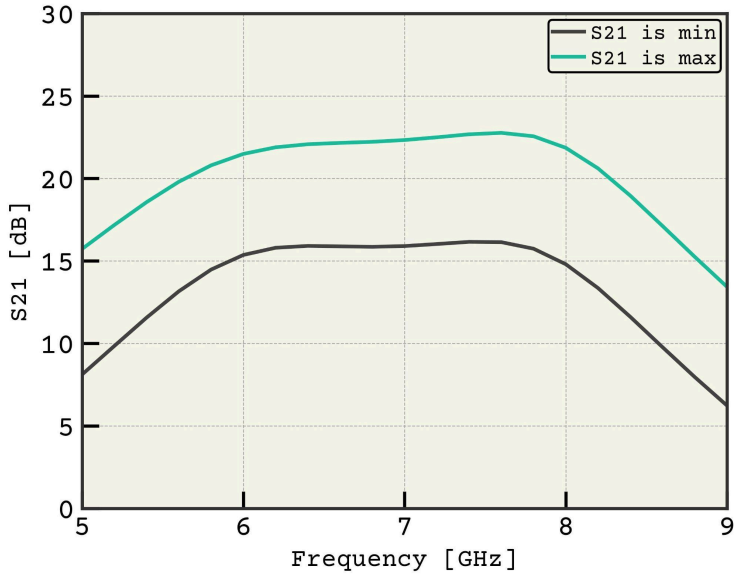


Fig-14: Insertion loss (attenuation gain) vs Frequency

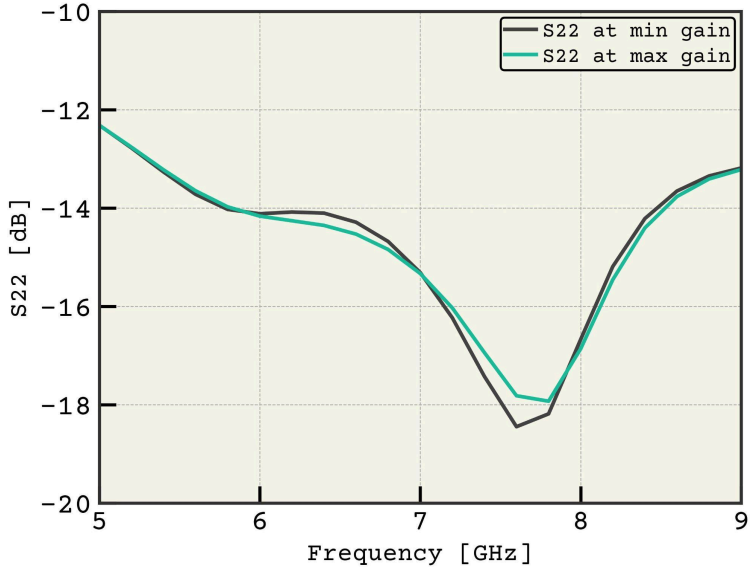


Fig-15: Input return loss vs Frequency

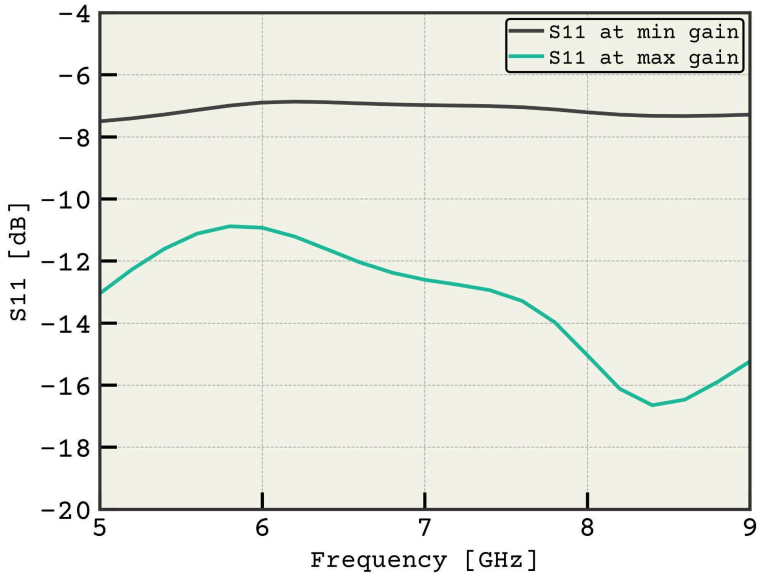


Fig-16: Output return loss vs Frequency

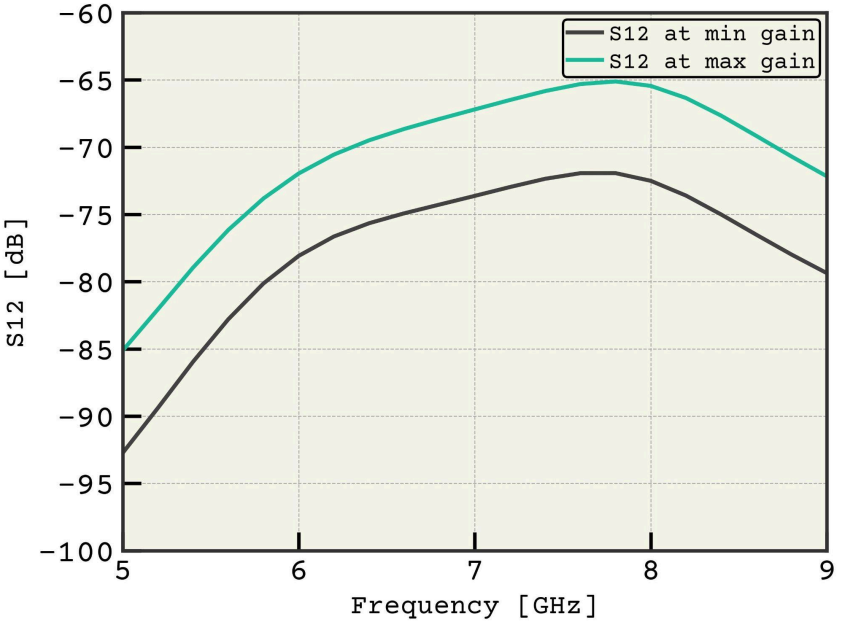


Fig-17: Reverse gain vs Frequency

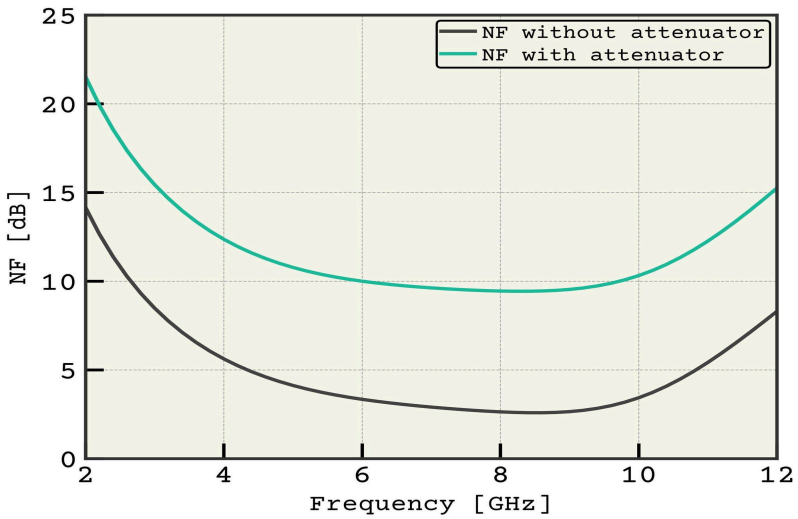


Fig-18: Noise factor/figure vs Frequency

IV. CONCLUSION

In this paper, a low-noise amplifier (LNA) is designed integrated with an attenuator to regulate the circuit's linearity and gain over a wide frequency range. The attenuator provides variable gain, enhancing noise immunity, optimizing stability, and supporting a broad operational bandwidth. The proposed LNA incorporates an attenuator and a single common-gate common-source (CG-CS) stage, which collectively contribute to adjusting the stability and achieving high gain while maintaining excellent noise performance and wide bandwidth.

Body biasing is utilized to enhance S-parameter values, while the elimination of passive L-C components improves both gain and output noise performance. The design is thoroughly analyzed mathematically and simulated using Cadence Virtuoso with GPDK 90nm CMOS technology.

The proposed LNA operates at a supply voltage of 1.2 V with a center frequency of 7.6 GHZ, achieving a power gain of 22.7 dB without an attenuator. The noise figure is less than 9.4 dB while using an attenuator with a gain of 22.7 dB. When the gain drops to 15.98 dB, the noise figure changes by around 0.3 dB at the low-frequency end of the band and by 1.2 dB at the high-frequency end. Considering the performance achieved, the proposed technique is suitable for the implementation of wideband LNAs in medical imaging sectors. As the attenuator is placed into the LNA, the performance characteristics are also adjusted within a reasonable range which makes the proposed LNA circuit unique. In the near future, the bandwidth may be further expanded by performing circuit modifications.

REFERENCES

[1] "Linearity improvement of gm-boosted common gate LNA: analysis to design," Ali Sahafi, Jafar Sobhi, Ziaddin Daei Koozehkanani, *Microelectronics Journal*, pp.156-162, vol.56, October 1, 2016.

[2] "A linear, low power, 2.5-dB NF LNA for UWB application in a 0.18 μm CMOS." Ismail Mohammadi, Ali Sahafi, Jafar Sobhi, and Ziaddin Daei Koozehkanan, *Microelectronics Journal*, pp. 1398-1408, vol.46, no.12, December 1, 2015.

[3] "A low power and high gain CMOS LNA for UWB applications in a 90 nm CMOS process." Sunil Pandey, Jawar Singh. *Microelectronics Journal, pp.*390-397, *vol.* 46, no. 5, May 1, 2015.

[4] "Noise suppression in a common-gate UWB LNA with an inductor resonating at the source node." Hossein Sahoolizadeh, Abumoslem Jannesari, Massoud Dousti,

AEU-International Journal of Electronics and Communications, pp.144-153, vol. 96, November 1, 2018.

[5] "50–830 MHz noise and distortion canceling CMOS low noise amplifier," Sana Arshada∗, Rashad Ramzanb, Qamar-ul Wahabc, Integration, pp.63-73 vol. 60, January 1, 2018.

[6] "Design of UWB low noise amplifier using noise-canceling and current-reused techniques," Mohsen Hayati, Sajad Cheraghaliei and Sepehr Zarghami, Integration, pp.232-239, vol. 60, January 1, 2018.

[7] "A 0.1–1.4 GHz inductorless low-noise amplifier with 13 dBm IIP3 and 24 dBm IIP2 in 180 nm CMOS," Benqing Guo, Jun Chen, Hongpeng Chen and Xuebing Wang, Modern Physics Letters B, pp.1850009, vol. 32, no 2, January 20, 2018.

[8] "A wideband noise-canceling CMOS LNA with enhanced linearity by using complementary nMOS and pMOS configurations," Benqing Guo, Jun Chen, Lei Li, Haiyan Jin, and Guoning Yang, IEEE Journal of Solid-State Circuits, pp. 1331-1344, vol. 52, no. 5, February 17, 2017.

[9] "A resistive-feedback LNA in 65 nm CMOS with a gate inductor for bandwidth extension," Huang, Dong, Shengxi Diao, Weiqiang Qian, and Fujiang Lin, Microelectronics Journal, pp' 103-110, vol. 46, no. 1, January 1, 2015.

[10] "A linear ultra wide band low noise amplifier using predistortion technique," Roya Jafarnejad, Abumoslem Jannesari, and Jafar Sobhi, AEU-International Journal of Electronics and Communications, pp. 172-183, vol. 79, September 1, 2017.

[11] "CMOS low-noise amplifier design optimization techniques," Trung-Kien Nguyen, Chung-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang and Sang-Gug Lee, IEEE Transactions on Microwave Theory and Techniques, pp.1433-1442, vol. 52, no. 5, May 2004.

[12] "Design challenges and performance parameters of low noise amplifiers," Gore, S. S., and G. M. Phade, International Journal of Innovations in Engineering and Technology (IJIET), pp. 204-209, vol. 3, no. 1, October 2013.

[13] "A wideband 2–5 GHz noise canceling subthreshold low noise amplifier," A. R. Aravinth Kumar, Bibhu Datta Sahoo, and Ashudeb Dutta, IEEE Transactions on Circuits and Systems II: Express Briefs, pp. 834-838, vol. 65, no. 7, June 26, 2017.

[14] "A Reconfigurable SPICE-Based CMOS LNA Design in 90 nm Technology Using ADS RFIC Dynamic Link," Arja, Pushpak Vasanth Rayudu, 2015.

[15] "A novel CMOS low-noise amplifier design for 3.1-to 10.6-GHz ultra-wide-band wireless receivers," Yang Lu, Kiat Seng Yeo, Alper Cabuk, Jianguo Ma, Manh Anh Do, and Zhenghao Lu, IEEE Transactions on Circuits and Systems I: Regular Papers, pp.1683 - 1692, vol.53, issue.8, August 21, 2006.

[16] "A custom low-noise preamplifier for Magnetic Particle Imaging," Wencong Zhang, Bo Zheng, Patrick Goodwill, Steven Conolly, in *2015 5th International Workshop on Magnetic Particle Imaging (IWMPI)*, pp. 1-1. IEEE, March 26, 2015.

[17] "A low noise cascaded amplifier for the ultra-wideband receiver in the biosensor," Maissa Daoud, Mohamed Ghorbel, and Hassene Mnif, *Scientific Reports,* pp. 22592, *vol.* 11, no. 1, November 19, 2021.

[18] "A Low Power Low Noise Amplifier for Biomedical Applications," Deepansh Dubey, Anu Gupta, In *2015 IEEE* International Conference on Electrical*, Computer and* Communication Technologies (ICECCT), pp. 1-6. IEEE, March 5, 2015.

[19] "Design and Implementation of Low noise Amplifier for MRI Scanner," Shailesh H., Yadav, Kishor G. Sawarkar, Ta pas Bhuiya, In *2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, pp. 744-747. IEEE, May 20-21, 2016.

[20] "Design and optimization of a sub - 1dB noise figure low noise amplifier for magnetic resonance applications using CMOS technology." Bal, Ayşe Rana, PhD diss., December 2024.

[21] "Fast quantitative low-field magnetic resonance imaging with OPTIMUM—optimized magnetic resonance fingerprinting using a stationary steady-state cartesian approach and accelerated acquisition schedules," Mathieu Sarracanie *Investigative radiology*, pp. 263-271, vol. 57, no. 4, April 1, 2022.

[22] "Magnetic resonance imaging with optical preamplification and detection," Anders Simonsen, J. D. Sánchez-Heredia, Sampo Antero Saarinen, Jan Henrik Ardenkjær-Larsen, Albert Schliesser, and Eugene Simon Polzik *Scientific reports, vol* 9, no. 1, December 3, 2019.

[23] "Optimal road noise matching to inductive sensors: Application to magnetic particle imaging," Bo Zheng, Patrick W. Goodwill, Neerav Dixit, Di Xiao, Wencong Zhang, Beliz Gunel, Kuan Lu, Greig C. Scott and Steven M. Conolly, pp.1041-1052, vol. 11, no.5, July 20, 2017.

[24] "Ultra low noise preamplifier design for magnetic particle imaging." Quincy Huynh, PhD diss., PhD Thesis, 2018.

[25] "Ultra-Low noise Amplifier Design for Magnetic Resonance Imaging systems." Mustafa A. Kabel, *arXiv preprint arXiv:1706.03507*, June 12, 2017

[26] "A comparative overview of high power handling CMOS switches and their recent applications in RF front ends," J. Rascher, A. Zohny, S. Glock, G. Fischer, R. Weigel, and T. Ussmueller, in Proc. IEEE Wireless Microw. Technol. Conf. (WAMICON), pp. 1–5, April 2013.

[27] "Highly integrated 4–32-GHz two-port vector network analyzers for instrumentation and biomedical applications," J. Nehring et al., IEEE Trans. Microw. Theory Techn., vol. 65, no. 1, pp. 229–244, January 2017.

[28] "A wideband analog-controlled variable-gain amplifier with dB-linear characteristic for high-frequency applications," H. Liu et al., IEEE Trans. Microw. Theory Techn., vol. 64, no. 2, pp. 533–540, February 2016.

[29] “Broadband compact InGaAs pin 5-bit digital attenuator using π-type resistive network,” J. G. Yang and K. Yang, Electron. Lett., vol. 48, no. 12, pp. 702–704, June 2012.

[30] “A 1.8-GHz 33-dBm P0.1 dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated wall structure,” M. Ahn, H. W. Kim, C. H. Lee, and J. Laskar,IEEETrans.Microw.TheoryTech., vol. 57, no. 11, pp. 2661–2670, Nov. 2009.

[31] "Design and analysis of a low loss, wideband digital step attenuator with minimized amplitude and phase variations," Ickhyun Song, Moon-Kyu Cho, and John D. Cressler, IEEE Journal of Solid-State Circuits, pp. 2202-2213, vol. 53, no. 8, May 4, 2018.

[32] “A wideband analog-controlled variable-gain amplifier with dB-linear characteristic for high-frequency applications,”H. Liu et al., IEEE Trans. Microw. Theory Techn., vol. 64, no. 2, pp. 533–540, Feb. 2016.

[33] "Design of a 1-V 90-nm CMOS adaptive LNA for multi-standard wireless receivers," E.C. Becerra–Álvarez[a], F. Sandoval–Ibarra[b], and J.M. de la Rosa, Revista Mexicana de física, pp. 322-328, vol. 54, no. 4, 2008.

[34] "Design and Simulation of Low Noise Amplifiers at 180nm and 90nm Technologies," Fathima Janisha, Lekha Pankaj, Int. Journal of Engineering Research and Application, ISSN : pp. 43-47,2248-9622, vol. 6, no. 11, (Part-1), November 2016.

[35] "Design & Simulation of LNA in 90nm CMOS Technology for Radio Receiver using the Cadence Simulation Tool," Nayak, Dhananjay, International Journals Digital Communication and Analog Signals, pp.1-9, vol. 8, no. 1, June 29, 2022.

[36] "Design of a high linear and ultra-wideband LNA using post distortion star feedback method," Siamak Veisi, Mostafa Yargholi, Microelectronics Journal, November 23, 2020.

[37] "Design of an Ultra Wideband Low Noise Amplifier(LNA) Circuit with High Center Frequency and Low Power Consumption, " Md. Asif Mahmood Chowdhury, Prasenjit Chowdhury, Conference Publishing Service,2013.

[38] "Design of 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current reuse technique," Qiuzhen Wan, Chunhua Wang, International Journal of Electronics and Communications (AEÜ), 20 March 2011.

[39] "Wideband RF CMOS Variable Attenuator Using Single Stage ΠΙ-Topology, " Nusrat Jahan, , I. L. Abdalla, Ramesh K. Pokharel, and Takana Kaho. pp.5, vol. 4.

[40] “Analysis and reduction of phase variations of variable gain amplifiers verified by CMOS implementation at C-band,” U. Mayer, F. Ellinger, and R. Eickhoff, IET Circuits, Devices Syst., vol. 4, no. 5, pp. 433–439, September 2010.