

## Article

# Wideband CMOS Variable Gain Low-Noise Amplifier with Integrated Attenuator for C-Band Wireless Body Area Networks

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## Abstract

This work presents a wideband variable gain low noise amplifier (VGA-LNA) specifically engineered for medical systems operating in the C frequency band, which require substantial amplification of low-intensity signals. The proposed design integrates a low-noise attenuator with a low-noise amplifier (LNA), fabricated using a 90 nm CMOS technology and leveraging a combined common-source and common-gate topology. The integrated LNA achieves a notable power gain of 29 dB across a broad bandwidth of 2 GHz (6.4–8.4 GHz), maintaining an average noise figure (NF) below 3.14 dB. The design ensures superior impedance matching, demonstrated by reflection coefficients of  $S_{11} < -18.14$  dB and  $S_{22} < -20.23$  dB. Additionally, the amplifier exhibits a third-order input intercept point (IIP3) of 21.15 dBm while consuming only 83 mW from a 1.2 V supply voltage. A low-noise attenuator is incorporated at the input side to enable effective gain control through a digitally controlled variable gain with step sizes ranging from 0.4 to 3.3 dB. This configuration enables a dynamic range of the transmission coefficient ( $|S_{21}|$ ) from 16 dB to 23 dB, adjustable 0.4 dB to 3.3 dB with a trade-off in NF maintained at 6 dB. The VGA-LNA demonstrates exceptional potential for integration into Wireless Body Area Networks (WBAN), balancing flexible gain control with stringent performance metrics.

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## 1. Introduction

LNAs have attracted significant attention as a vital component in circuit design in the field of communication and medical systems owing to their ability to amplify weak input signals while minimizing external noise. LNA enhances the performance and efficacy of medical systems by improving signal quality and sensitivity. Recent progress has aimed at better performance of gain, bandwidth and noise to meet the demands of modern diagnostic

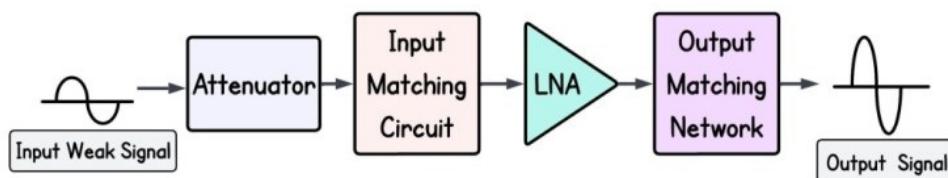
applications. For example, at 6.5 GHz, *Microwave Breast Cancer Imaging* requires a minimum LNA gain of 20–25 dB, as high sensitivity is needed to detect weak reflections from soft tissues. At 6.8 GHz, *Microwave Radiometry* is used for non-invasive deep tissue temperature monitoring (e.g., tumors, brain), where signal levels are extremely low, requiring 20–30 dB gain. At 7.0 GHz, *WBAN (Wireless Body Area Network)* supports high-data-rate medical telemetry over short distances, but to maintain data integrity in noisy environments, an LNA gain of 15–20 dB is needed. At 7.2 GHz, *Microwave Brain Imaging* for stroke detection demands a higher gain of 25–30 dB because brain signals are very weak after passing through the skull. At 7.5 GHz, *Tissue Dielectric Property Measurement* is mainly a research application, needing 20–25 dB gain due to the low signal strength. At 7.8 GHz, *Microwave Ablation Monitoring* (such as for liver or kidney tumors) requires real-time monitoring, needing around 20–25 dB gain. At 8.0 GHz, *Implantable Device Telemetry* (e.g., for glucose sensors) operates over short distances and typically needs 15–20 dB gain. Finally, at 8.4 GHz, *Deep Tissue Imaging Research* uses high-resolution microwave imaging, where weaker return signals at higher frequencies require a 25–30 dB gain.

Designing LNAs with various topologies faces challenges in limiting their use in low-power or high-performance applications like narrowband impedance matching, selective gain, high supply voltage needs, and poor noise performance[1,2]. Achieving all features simultaneously is a major challenge as conventional techniques often limit the ability to meet all specifications at once [3,4]. Although existing designs such as resistive shunt-feedback LNAs, and UWB LNAs address noise and bandwidth issues, many multi-stage designs consume high power and occupy more area [5,6]. Traditional LNA architectures, particularly limits the bandwidth. In contrast, CMOS-based approaches offer improved linearity, better frequency response, low power consumption, and high integration potential, effectively addressing challenges in noise suppression and bandwidth optimization. So, UWB LNA could be highly linear, comparing its performance with advanced CMOS designs[7–10]. The scalability of CMOS technology further makes it suitable for wideband applications, and RF circuit design. CMOS-based LNA strategies are explored in RF circuit principles for LNA development. Together, these insights highlight significant advancements in LNA performance, efficiency, and integration [11,12]. For example, the need for low-power, high-performance CMOS RF circuits in wireless communication is emphasized in [13,14], highlighting the importance of the LNA in amplifying weak signals with minimal noise. The challenges in designing reconfigurable multiband LNAs, such as impedance matching and maintaining low noise, are discussed. The development of an effective LNA is crucial for multi-standard receivers. The design of a two-stage UWB LNA in [15] tackles challenges like noise and impedance matching, and bandwidth improvement, showing the strong performance with low noise, high power gain, and good power efficiency and provides a clear explanation of its design, operation, and performance. To further contextualize our contribution, we reviewed recent LNA designs targeting frequencies within or close to the 6.4–8.4 GHz band relevant to WBAN and medical systems. For example, Kumar et al. [13] demonstrated a wideband 2–5 GHz CMOS LNA with  $NF \approx 6$  dB and  $|S21| \approx 13$  dB, while Lu et al. [15] reported a UWB LNA for 3.1–10.6 GHz achieving  $|S21| \approx 16 - 18$  dB and  $NF$  in the 2.5–3.4 dB range. Similarly, Huang et al. [9] designed a 65 nm CMOS resistive-feedback LNA with bandwidth extension up to 8 GHz but with limited gain ( $\approx 11$  dB). Compared to these works, our proposed VGA-LNA achieves significantly higher forward gain ( $\approx 29$  dB), competitive  $NF$  ( $\leq 3.14$  dB standalone), and digitally programmable variable gain control ( $\approx 7$  dB range), features not simultaneously reported in earlier designs.

The resonance frequency can limit bandwidth, emphasizing the trade-off between usable bandwidth and noise figures in MPI systems [16]. A multi-stage (4stage) optimized

LNA provides efficient amplification with good isolation and low noise levels [17]. Additionally the optimized biasing technique reduces input noise and power consumption, showing strong potential for biomedical applications [18].

In LNA design the common gate topology is preferred in the input stage due to its ease of impedance matching, excellent noise characteristics, and widened capabilities which makes it suitable for 50 source matching. Again a common source topology can be used as amplification stage in LNA, due to its high voltage gain for amplifying weak signals. Its high input impedance makes it appropriate for high-impedance sources and allows for easy gain control, providing flexibility in design. Additionally, the simple design and good isolation between the input and output enhance the stability of the CS stage, making it a reliable choice for amplification. Compared to prior works this design offers broader applicability, low noise, and tunable gain—ideal for dynamic medical applications [19,20]. In this work, we proposed a two-stage LNA using a common gate followed by a common-source topology with an input-side attenuator for improved input matching and noise performance, as shown in Figure 1. Designed in 90 nm tech., the CG-CS cascade achieves high gain and bandwidth, targeting 7.616 GHz with a 1.7 GHz bandwidth, making it ideal for wideband biomedical application. A buffer circuit enhances output noise immunity. The main challenge was balancing power while maintaining stable high gain, as lower supply voltages reduce gain margin and increase noise sensitivity. To address this, the input-side attenuator offers a gain-adjustable solution for medical application. Circuit-level simulations show improved performance over previous work in Cadence Virtuoso. Section II details the design methodology, Section III covers performance analysis, Section IV presents results, and Section V concludes. The design is compact and efficient promising significant improvements in medical applications.



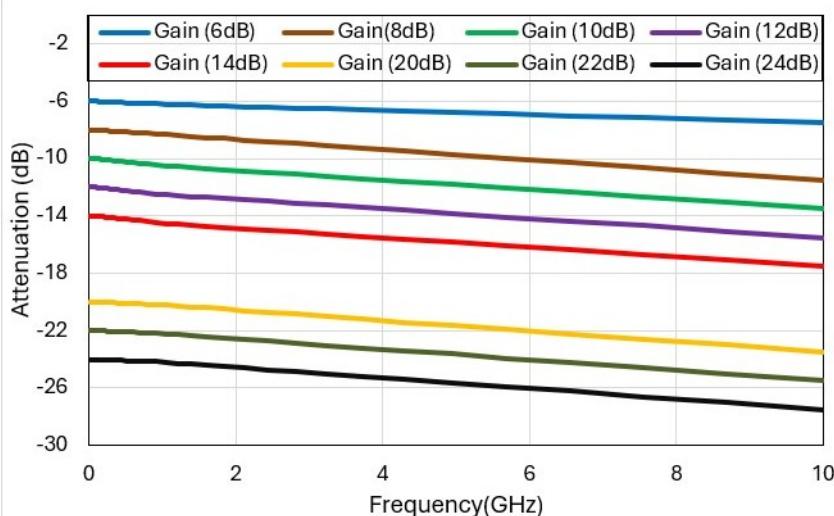
**Figure 1.** Block diagram of the proposed design.

## 2. Proposed variable gain low noise amplifier

### 2.1. Proposed LNA

The design of wideband LNA becomes extremely challenging when analog and RF circuits operating in the sub-threshold zone display increased thermal noise, poorer bandwidth, and poor linearity, even while sub-threshold biasing gives better  $\frac{g_m}{I_d}$  compared to strong inversion. Our suggested LNA provides high linearity, a broad bandwidth, a modest gain, and a reasonable noise figure. To guarantee optimum performance, a number of crucial elements (such as frequency range, gain, noise figure, input/output impedance, and power consumption) must be taken into account when constructing a Low Noise Amplifier (LNA). We have first established the operational frequency range of 6.4 GHz to 8.4 GHz. A common gate (CG) stage and a common source (CS) stage with a gain-boosted, source follower buffer circuit are both included in the proposed LNA. In Figure 3 the schematic of the proposed wideband LNA is shown. The component values of LNA are summarized in Table 2. The common gate amplifier circuit is utilized as a first stage because it offers superior input matching due to its low input impedance, low noise performance, and enhanced linearity. The load on the CG stage is inductive ( $L_1$ ) which offers better noise performance.  $C_1$ , the coupling capacitor blocks the DC and passes the AC signal. A LC tank is formed by  $L_2$  and  $C_{gs1}$ . The CG-CS cascaded stage is included to maintain low

noise levels, supply the required gain, and permit design modifications to satisfy particular operational needs. By resonating with  $M_2$ 's total capacitance at the drain, the CS stage load  $L_3$  offers shunt peaking, improves the low-frequency gain which controls the peak at resonance, and expands the bandwidth.  $L_4$  in the CS stage is used for obtaining better gain flatness. Two mirror circuits are used here as a biasing circuit. They are consist of a transistor ( $M_6, M_7$ ), resistor ( $R_6, R_7$ ) and  $V_{DD}$ .  $C_3$  is connected between gate and the ground terminal to ensure a good AC grounding and to bypass the noise contributed by the biasing circuit.  $R_4$  is used here for reverse isolation. To match and measure the output, a source follower buffer is introduced which isolate the output of the CS stage from the load impedance variation. After measurement, the buffer's influence must be eliminated to extract the LNA's performance alone from the entire circuit. The passive component values used in the design represent idealized synthesis outcomes used for circuit-level simulations. We recognize that these values exceed the practical ranges of on-chip passives in 90 nm CMOS technology. In future work, these will be replaced with technology-compatible scaled passives and validated through layout-level EM simulations and eventual chip fabrication.



**Figure 2.** Attenuation vs. frequency characteristics for different gain levels (6–24 dB).

## 2.2. Variable Gain Attenuator

The proposed attenuator employs a single-stage  $\pi$  topology integrated into the LNA input, featuring five cascaded attenuation phases. This configuration was selected for its superior impedance matching, compact control logic, and robustness against parasitic effects at C-band, making it particularly well-suited for medical WBAN applications where flexible gain control and reliability are critical. Each phase includes a pair of FET-switched shunt branches ( $M_{15}/M_{18}$  and  $M_{16}/M_{17}$ ) alongside fixed resistors ( $3R/10R$ ) to ensure smooth impedance matching at both input and output. The transistor gate widths are  $2\mu m$ , with  $R=10$ , optimized via S-parameter simulations. There are 2 attenuation states as: Low attenuation state: Series FETs are ON (minimal  $R$ ), shunt FETs are OFF. Loss is dominated by the nonzero on-resistance at low frequencies; high-frequency loss is further influenced by parasitic capacitances. High attenuation state: Shunt FETs ON, series FETs OFF. Figure 2 illustrates the simulated frequency response of the stand-alone attenuator, demonstrating insertion loss values ranging from 6 dB to 24 dB in discrete 2 dB steps. The attenuation states are programmed through six digital control voltages ( $V_c$ ), with the logic combinations summarized in Table 1. Each control line operates in binary mode, where the high and low states correspond to 1.0 V and 0 V, respectively. A simple shift-register control manages  $V_c$  (and its complement  $V_c$ ), enabling a compact 6-bit digital control scheme.

When  $V_c = 0$ ,  $V_c' = 1$  ( $M_{16}$  and  $M_{17}$  ON), attenuation spans **22–24 dB**. Reversing logic ( $V_c = 1$ ,  $V_c' = 0$ ) ( $M_{15}$  and  $M_{18}$  ON) yields **6–20 dB**. If both control bits are set OFF (logical Low), all FETs remain OFF, causing the attenuator to default to **22 dB** attenuation. This can be treated as a fail-safe high attenuation fallback to avoid undefined gain. Optionally, the controller can flag this as an invalid state or trigger an alert.

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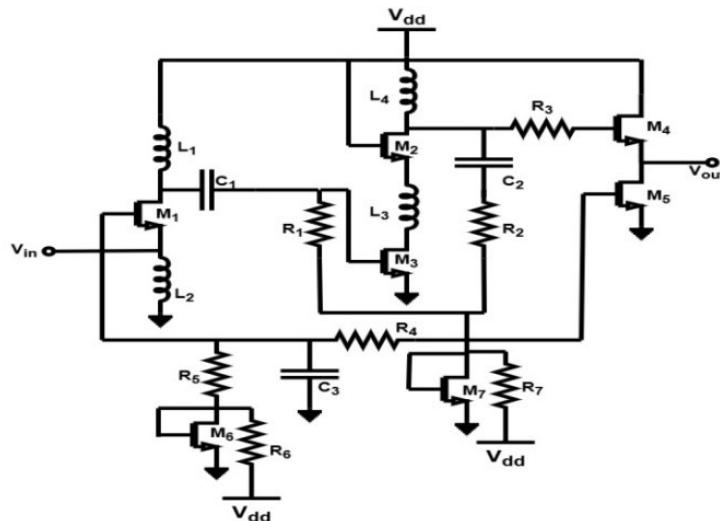
**Table 1.** The gain of the attenuator

<b>Vc</b>	<b>V1</b>	<b>V2</b>	<b>V3</b>	<b>V4</b>	<b>V5</b>	<b>Attenuation (dB)</b>
Low	High	Low	Low	Low	Low	-6
Low	Low	High	Low	Low	Low	-8
Low	Low	Low	High	Low	Low	-10
Low	Low	Low	Low	High	Low	-12
Low	Low	Low	Low	Low	High	-14
High	High	Low	Low	Low	Low	-16
High	Low	High	Low	Low	Low	-18
High	Low	Low	High	Low	Low	-20
High	Low	Low	Low	High	Low	-22
High	Low	Low	Low	Low	High	-24

### 2.3. Designing method

This study will be a simulation-based study using the Cadence Virtuoso 90 nm technology Software, with component values are (resistors, inductors, and capacitors) determined by a suitable matching network.

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**Figure 3.** Schematic of the proposed wideband low noise amplifier (with biasing circuit).

An appropriate matching network will be used to estimate the values of the component. To get optimum power transmission, matching networks are utilized to match the impedance from gate to source and source to load. We computed the input and output impedance values first using simulation tool Cadence Virtuoso. Subsequently, the suitable network topology will be chosen; RC networks, and L-networks are instances of common topology. The performance of the matching network is analyzed by simulation, with a special focus on bandwidth, gain, efficiency, and return loss. Initially, we began with Smith chart-based optimization and theoretical Q-value analysis to guide the matching network design. Subsequently, these parameters were refined using Cadence Virtuoso, where Smith chart and Q-value guided optimization were implicitly embedded within the simulation

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environment. If the performance is not up to par, the design can be repeated numerous times by varying the component value or topology until the intended outcome is achieved.

### 3. Performance Metrics Analysis

#### 3.1. Input and output matching

Characterizing the impedance and admittance of a two-port network operating at low frequencies often involves using the impedance matrix ( $Z$  parameters) and admittance matrix ( $Y$  parameters). However, these two approaches are insufficient for a network that operates at high frequencies. S-parameter analysis or scattering can be used instead. In this instance, the S-parameter matrix provides the link between the incident power waves that are reflected.

**Table 2.** Component values

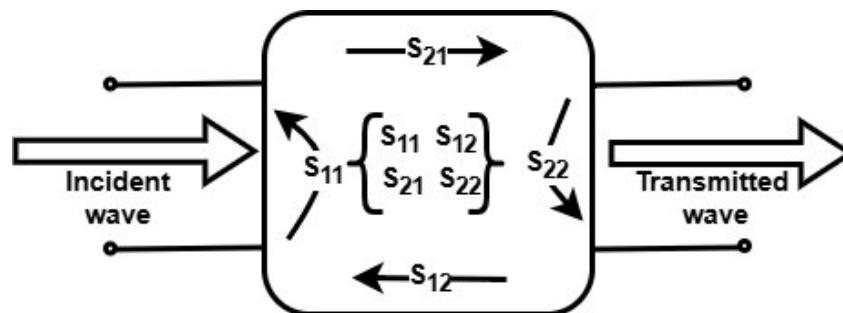
Aspects Ratio	$(W/L)_1$	$(W/L)_2$	$(W/L)_3$	$(W/L)_4$
	40u/100n	80u/100n	45u/100n	28u/100n
	$(W/L)_5$	$(W/L)_6$	$(W/L)_7$	
	45u/100n	45u/100n	45u/100n	
<b>Inductor (nH)</b>	$L_1 = 1.9$	$L_2 = 1.2$	$L_3 = 4.3$	$L_4 = 1.4$
<b>Capacitor (pF)</b>	$C_1 = 0.6$	$C_2 = 0.35$	$C_3 = 8$	
<b>Resistors (<math>\Omega</math>)</b>	$R_1 = 50$	$R_2 = 15e3$	$R_3 = 1e3$	$R_4 = 15$
	$R_5 = 50$	$R_6 = 18$	$R_7 = 15$	

Let,  $a_1$  and  $a_2$  are incident waves;  $b_1$  and  $b_2$  are transmitted waves. Using a two-port network in s-parameter analysis,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \times \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

The Equation Representation of the Matrix is as follows:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2, & b_2 &= S_{21}a_1 + S_{22}a_2, \\ S_{11} &= \frac{b_1}{a_1} \quad (\text{when } a_2 = 0), & S_{12} &= \frac{b_1}{a_2} \quad (\text{when } a_1 = 0), \\ S_{21} &= \frac{b_2}{a_1} \quad (\text{when } a_2 = 0), & S_{22} &= \frac{b_2}{a_2} \quad (\text{when } a_1 = 0). \end{aligned}$$



Where,

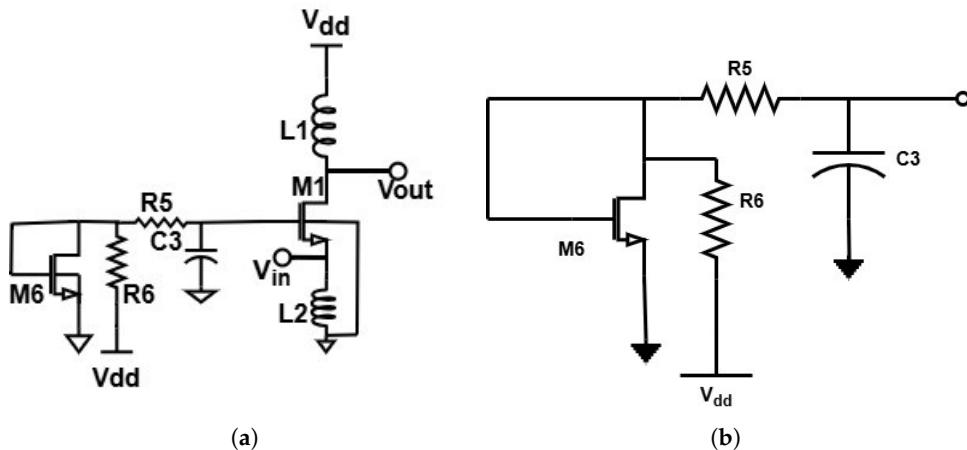
- $S_{11}$  is the input port voltage reflection coefficient,

$$S_{11} = \left| \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \right|$$

- $S_{12}$  is the reverse voltage gain.

- $S_{21}$  is the forward voltage gain.
- $S_{22}$  is the output port voltage reflection coefficient.

Impedance matching can be achieved in various ways. For a wideband CG-LNA, input matching is accomplished by setting its transconductance to  $g_m = \frac{1}{R_s}$ , where  $R_s = 50\Omega$ .



**Figure 4.** (a) 1st stage of LNA (Common gate stage). (b) Biasing network for CG stage.

represent the source impedance. To minimize mismatching issues, the LNA's input must be matched precisely to  $50\Omega$ . Since the impedance is purely real, achieving a  $50\Omega$  match also enables simultaneous conjugate power matching, ensuring the best possible power transmission and fulfilling the system requirements. Therefore, selecting the appropriate methods to obtain a  $50\Omega$  input impedance, as shown in Figure 4, is essential. The small-signal equivalent circuit for the impedance calculation is shown in Figure 5.

From Figure 5,  $Z_d$  is the impedance of the load,  $Z_{in2}$  is the input impedance of the next stage, and  $g_{m1}$  is the trans-conductance of the MOS transistor in common-gate configuration.

Now,

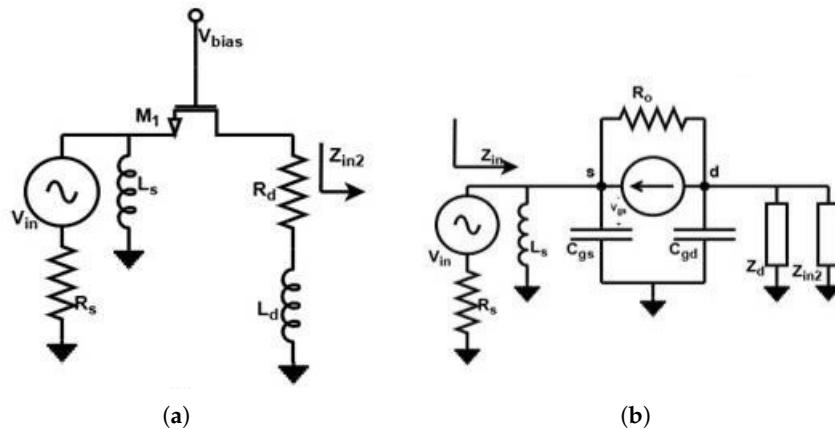
$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Z_s} + (1 - g_{m1}Z_o)(R_o + Z_o)} \quad (1)$$

Where

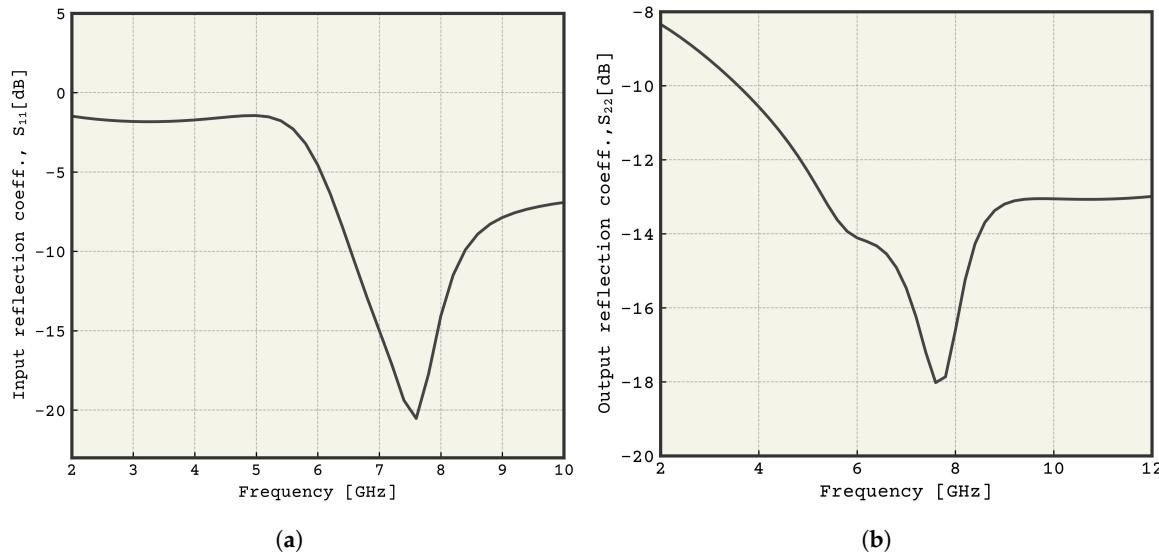
$$Z_s = j\omega L_2 \parallel \frac{1}{j\omega C_{gs}} \quad (2)$$

$$Z_o = \frac{1}{j\omega C_{gd}} \parallel Z_d \parallel Z_{in2} \quad (3)$$

Based on the aforementioned deductions, the following observations can be made: Due to the dominance frequency-dependent  $Z_s$  in the imaginary component, the common-gate stage's unsatisfactory matching occurs throughout the band. The tank circuit should be designed to resonate near the center of the 6.4–8.4 GHz band to ensure good broadband matching and maintain real input impedance close to  $50\Omega$ . The best input matching over the given bandwidth is found in a MOS transistor with an aspect ratio of  $\frac{57\mu}{100n}$  and  $L_2 = 1\text{nH}$ , according to simulations. The value of  $S_{11}$  is -20.528 dB, suggesting better input matching at the operating frequency(7.6 GHz) in Figure 6(a). Only a small amount of power — approximately 1% — is reflected back at input side, while majority of the power enters the amplifier rather than being bouncing. Similarly the value of  $S_{22}$  in Figure 6(b), indicates good output matching, meaning the most of the power is transmitted rather than reflecting.



**Figure 5.** (a) Configuration of a Common gate input stage. (b) Small signal in common gate.



**Figure 6.** (a) Input return loss vs. Frequency. (b) Output return loss vs. Frequency.

### 3.2. Noise Analysis

An LNA's noise performance is directly correlated with the matching of its input. Wide-band input matching, which cannot be tuned for a specific frequency, typically results in higher inherent noise compared to narrow-band matching. Therefore, the strict trade-off between the wide-band input matching and the noise figure of the wideband LNA must be carefully evaluated. It should be noted that the noise contribution of the first-stage amplifier is critical, as the source noise has already been amplified up to that point. The noise factor is further degraded by a product of the total gain products up to that point when compared to the noise generated by the preceding system along with the already generated source noise of the system.

The key metric for assessing a system's noise performance is the Noise Figure (also known as the Noise Factor). The partnership is as follows:

$$NF = 10 \cdot \log_{10}(F)$$

The noise factor due to termination is given by the following expression,

$$F = \frac{\text{Total power of output noise}}{\text{Total power of output noise due to source alone}} = 2 + \frac{4\gamma}{\alpha} \cdot \frac{1}{g_m R} \quad (4)$$

Where,  $\gamma$  is the MOS transistor's coefficient of channel thermal noise and is defined as the ratio of the trans-conductance and the zero-bias drain conductance.  $\gamma$  is process-dependent and difficult to control, the noise performance can be optimized by increasing the trans-conductance of the MOS transistor, i.e., trading off the 50-input matching. For first stage,

$$F = 2 + \frac{\gamma}{\alpha} + \frac{R_5 + R_{L2}}{R_{L1}} \quad (5)$$

Where,  $R_{L1}$  is the parasitic resistance of the drain inductor  $L_1$  and  $(R_5 + R_{L2})$  is the input source signal and  $R_{L2}$  is the parasitic resistance of the source inductor  $L_2$ . As shown in Figure 7(b) inductively source-degraded common source topology is commonly used in wide-band LNA designs because it is a better option for concurrently achieving optimal noise and good input matching.

$$Z_{in} = \frac{g_{m3}}{(C_1 + C_{gs3} + 2C_{gd})L_4} + j \left[ \omega_H L_4 - \frac{1}{\omega_H(C_1 + C_{gd} + C_{gs3})} \right] \quad (6)$$

Where,  $C_{gs3}$  represents the gate to source capacitance of  $M_3$ . By adjusting  $C_1$ ,  $L_4$ ,  $C_{gd}$  and  $C_{gs3}$  so that, at the input frequency, the imaginary term equals zero. It is possible to obtain a real term of  $50\Omega$  without the need for a resistor. Moreover, it offers simultaneous power matching. It is most common to use this type of arrangement when developing narrow-band LNAs.

$$\left( \omega_H L_4 - \frac{1}{\omega_H(C_1 + C_{gd} + C_{gs3})} \right) = 0 \quad (7)$$

$$\Rightarrow \omega_H = \frac{1}{\sqrt{L_4(C_{gs3} + C_{gd} + C_1)}} \quad (8)$$

$$\text{and } Z_{in} = \frac{g_{m3}}{(C_1 + C_{gs3} + 2C_{gd})L_4} = 50\Omega \quad (9)$$

where:

$$C_{gs3} = \frac{2}{3} C_{ox} W_{opt} L_4, \quad g_{m3} = \frac{2I_d}{V_{ov}}, \quad W_{opt} = \frac{1}{3\omega_H L_4 C_{ox} R_s} \quad (10)$$

This configuration's noise factor is determined by the following formula:

$$F = 1 + \gamma g_m R_s \left( \frac{\omega_0}{\omega_T} \right)^2 \quad (11)$$

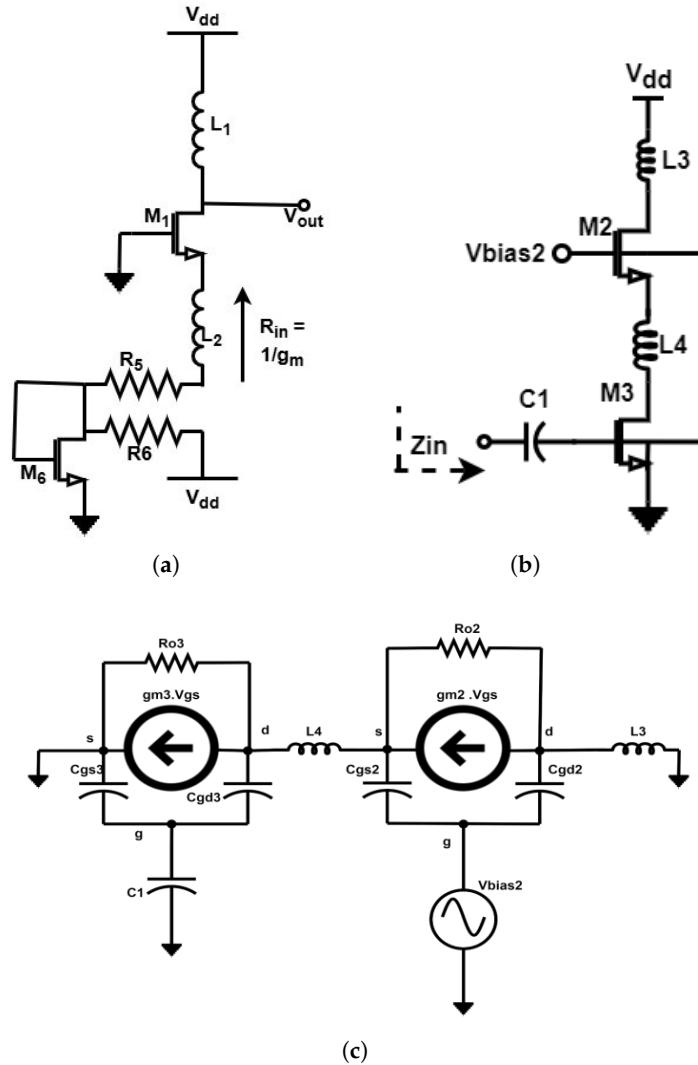
The minimum noise figure of this topology can be low.

- Transit or cutoff frequency:  $\omega_T = \frac{g_{m3}}{C_1 + C_{gs3} + 2C_{gd}}$
- Transconductance:  $g_m$
- Total effective input capacitance:  $C_T = C_1 + C_{gs3} + 2C_{gd}$
- Drain current:  $I_d$

### 3.3. Gain Analysis:

The suggested wideband LNA includes a CS-CG cascaded gain-boosting stage. By decoupling the two stages, evaluating the gain of each stage separately, and then calculating the overall gain allows for the completion of the gain analysis. The first stage gain can be calculated by using the formula,

$$A_{V1} = g_{m1}(1 - \alpha)Z_{L1} \quad (8)$$



**Figure 7.** (a) 1st stage of LNA (CG stage) with biasing network (b) 2nd stage of LNA (CS stage) for noise analysis. (c) Small signal of a CS stage.

Where,

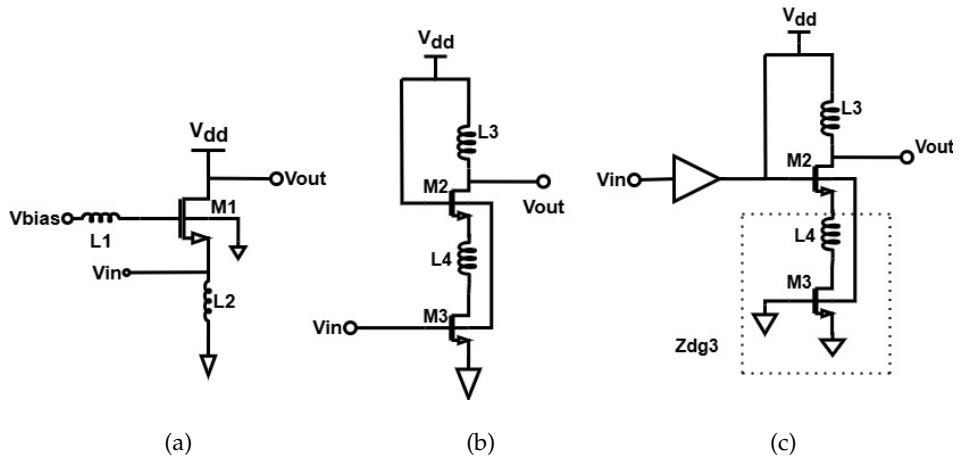
$$\alpha = \frac{sC_{gs1} p + sC_{gd1} g_{m1}}{pq + sC_{gd1}(g_{m1} - sC_{gd1})}$$

$$Z_{L1} = \frac{1}{s(C_{db1} + C_{g3})}$$

$$p = \left( \frac{1}{Z_{L1}} + sC_{gd1} \right)$$

$$Z_{G1} = (sL_1 + R_{L1}) \parallel \left( \frac{1}{sC_{gb1}} \right)$$

$$q = \left( \frac{1}{Z_{G1}} + sC_{gs1} + sC_{gd1} \right)$$



**Figure 8.** Gain analysis (a) CG stage-1.(b) CS stage-2 and (c) CG-CS cascaded stage.

We must apply the superposition concept to examine the second stage's gain. The CS-CG stage is depicted in Figure 8(b) and (c), where the gain block  $A_{V1}$  represents the input CG-stage's gain. Let  $A_{V2}$  and  $A_{V3}$  represent the gain and the gain from the gate of  $M_2$  and  $M_3$  to the output, (9) and (10) provide  $A_{V2}$  and  $A_{V3}$ , respectively.

$$A_{V2} = \frac{g_{m2} Z_{L3}}{1 + g_{m2} Z_{dg3}} \quad (9)$$

$$\text{where } Z_{dg3} = \frac{1}{sC_{sb2}} \parallel \left( sL_4 + \frac{1}{sC_{db3} + sC_{gd3} + \frac{1}{r_{03}}} \right)$$

$$A_{V3} = \left( \frac{g_{m2} Z_{L3}}{g_{m2} + sC_{sb2} + sC_{gs2}} \right) \left( \frac{g_{m3}}{1 + sZ_3 C_{db3}} \right) \quad (10)$$

$$\text{where } Z_3 = sL_4 + \frac{1}{sC_{sb2} + sC_{gs2} + g_{m2}}$$

$$Z_{L3} = (R_{L3} + sL_3) \parallel \left( \frac{1}{sC_{db2}} \right) \parallel Z_L$$

$Z_L$  is the impedance of the load (mixer or variable gain amplifier (VGA)) connected to the LNA.

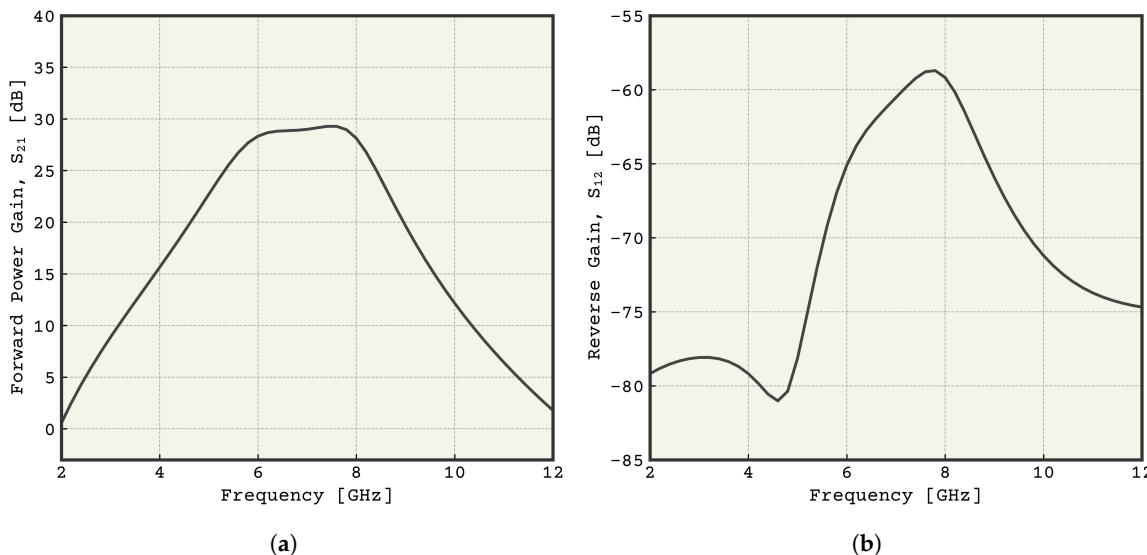
LNA's total gain,

$$A_V = A_{V1} \cdot A_{V2} + A_{V3} \quad (11)$$

Total forward power gain, shown in Figure 9(a), indicates the larger gain, which means output power is more hundreds time larger than input power. And reverse power gain in Figure 9(b), demonstrates good reverse isolation with only a little amount of signal leaking backward. So this LNA is doing a great job of blocking reverse signal flow.

### 3.4. IIP3

One crucial characteristic that reflects the linearity of the amplifier is the input-referred third-order intercept point (IIP3) of an LNA. It stands for the fictitious input power level at which the basic signals' power and the power of the third-order inter-modulation products are identical. A higher IIP3 value denotes better linearity and less distortion, both of which are essential for preserving signal integrity. For many contemporary applications, particularly in cellular and wireless communication, an IIP3 of approximately +5 dBm or greater is generally preferred. The input referred third-order intercept point (IIP3), is shown in Figure 10. The value (One tone is selected to test the IIP3 of the LNA. The IIP3 is found to be 21.1537 dBm in Figure 10.



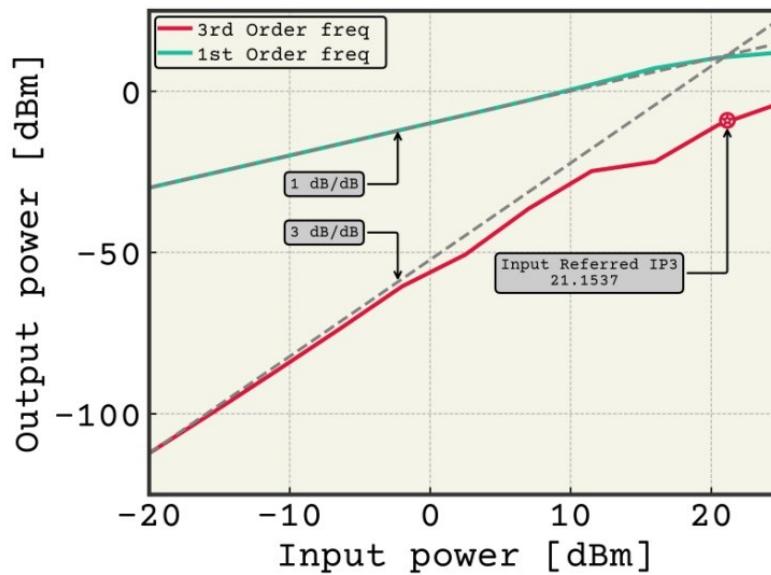
**Figure 9.** (a) Forward Gain vs. Frequency. (b) Reverse gain vs. Frequency.

### 3.5. Stability Analysis

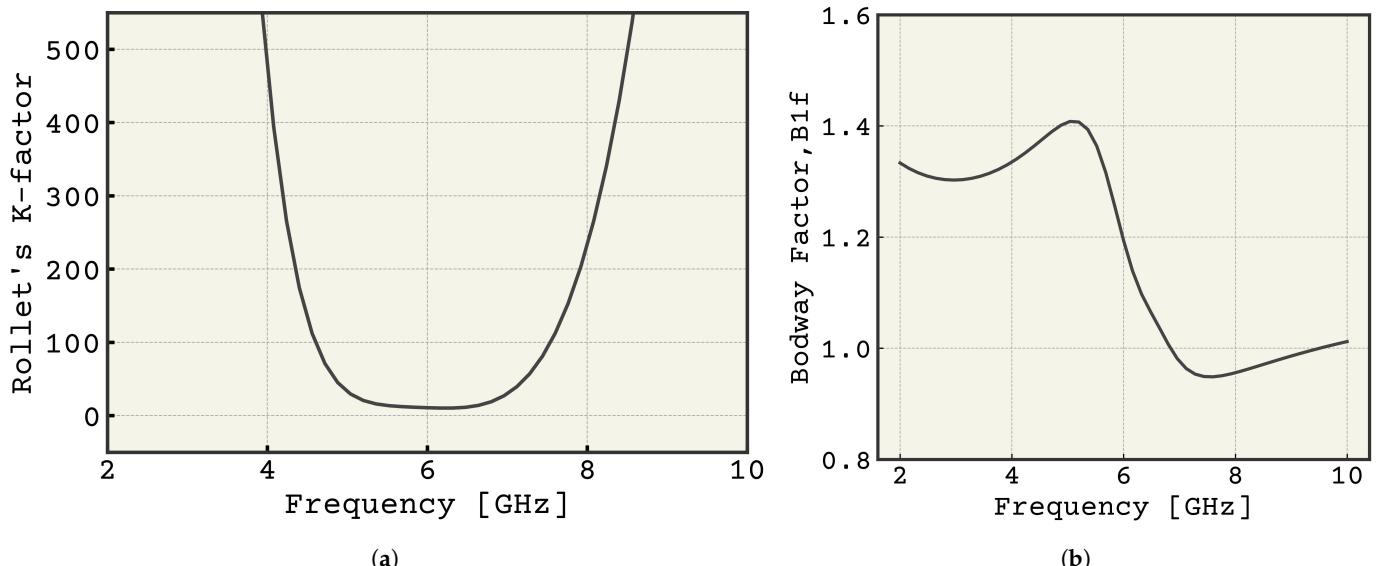
Based on the input and output reflection coefficients, the stability factor—often denoted as K, or Rollet's stability factor—is used to determine whether an amplifier is unconditionally stable, conditionally stable, or perhaps unstable. To operate reliably, a larger stability factor denotes improved resilience to oscillations. The stability factor Kf can be calculated using the following formula:

$$K_f = \frac{(1 - |S_{11}|^2 - |S_{22}|^2)}{|S_{12} \cdot S_{21}|} \quad (12)$$

As the value of Kf = 10 > 1 and the B1f value > 0, shown in Figure 11(a) and (b) indicates the unconditionally stability, meaning the amplifier is stable within a specific range of impedances, necessitating careful design considerations.



**Figure 10.** Output power vs. Input power (IIP3)



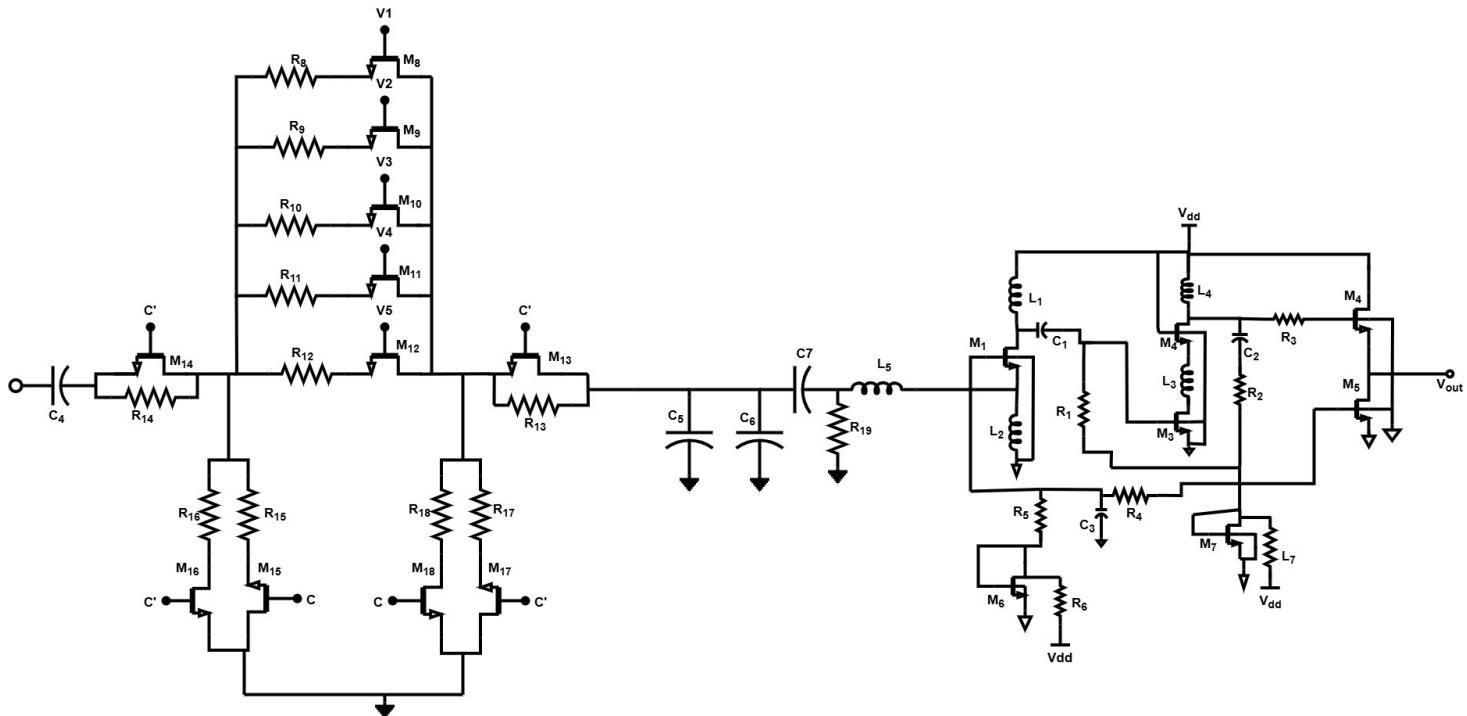
**Figure 11.** (a) Rollet's K factor vs. Frequency. (b) Bodway factor vs. Frequency .

### 3.6. Designed LNA with Attenuator

Several traditional attenuators with series and shunt resistance adjustments use T, and bridged T topologies. By controlling the FET switches, the attenuator experiences the least attenuation when the series resistance is minimal and the shunt resistances are large. In that scenario, the series switch's nonzero on-resistance is the only source of the loss at the lowest frequencies. The insertion loss resulting from the attenuator's minimum insertion decreases as this resistance decreases [31,39]. The parasitic capacitors introduce greater loss to ground at higher frequencies, hence reducing these capacitors lowers the insertion loss. Similarly, when the T-attenuator is set to minimal gain, the shunt component is off and the series components are fully on. In our analysis,  $\pi$ -topology is displayed a wider frequency response when compared to T-topology. Furthermore, there is a trade-off between greater impedance matching and T-topology attenuator attenuation. Figure 12 displays the schematic of the suggested variable attenuator with the designed LNA. Five

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successive phases make up its single stage  $\pi$ -topology. Transistors ( $M_{15,18}/M_{16,17}$ ) and resistors (3R/10R) are employed in two shunt branch pairs to enhance the attenuator's input/output impedance matching. We used S-parameter simulation to optimize the parameter; the gate width of each FET switch was set to  $2\mu\text{m}$ , and the resistance value R was set to  $10\Omega$  [39]. The components values of the attenuator with the T matching network in the input side of LNA are shown in Table 3.



**Figure 12.** Proposed LNA with 5 stages attenuator.

**Table 3.** Component Values

Aspect ratio	$(W/L)_8 \sim (W/L)_{19}$					
	$2\mu/100\text{n}$					
Inductor (nH)	$L_5$					
	1					
Capacitor (pF)	$C_4$	$C_5$	$C_6$	$C_7$		
	400	95	0.04	3		
Resistor ( $\Omega$ )	$R_8$	$R_9$	$R_{10}$	$R_{11}$	$R_{12}$	$R_{13}$
	12	8	4	2	1	5
	$R_{14}$	$R_{15}$	$R_{16}$	$R_{17}$	$R_{18}$	$R_{19}$
	5	3	10	10	3	$1.04\text{e}3$

### 3.7. Gain Analysis of designed LNA with the attenuator

With a straightforward shift register control bit  $V_c$  and  $V_c'$ , where  $V_c'$  is the complementary of  $V_c$ , the designed attenuator offers attenuation ranging from 15.97 dB to 22.70 dB. The attenuation stages will reach a lesser attenuation state from 15.97 dB to 22.70 dB when the transistors  $M_{16}$  and  $M_{17}$  are turned on, that is when  $V_c$  is low and  $V_c'$  is high.

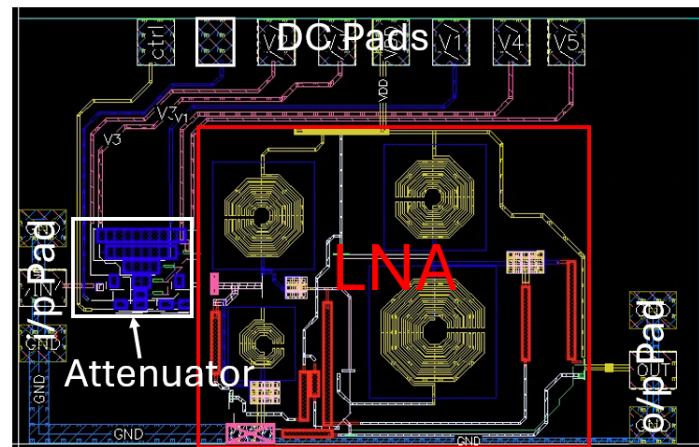
Likewise, transistors of the five stages exhibit a higher attenuation condition from 16 dB to 22.52 dB when M<sub>15</sub> to M<sub>18</sub> are turned on (V<sub>c</sub> is high and V<sub>c'</sub> is low). The incorporated variable gain amplifier facilitates effective gain control through digitally programmed step adjustments ranging from 0.4 to 3.3 dB; however, the step uniformity is affected by CMOS FET switch parasitics and finite resistor values. The resulting dB linearity error is recognized as a current design limitation, with future work aimed at mitigating this effect through linearization techniques. Six digital control voltages are used in the suggested attenuator[39]. The digital control voltage combinations to choose the attenuation state are displayed in Table 4 and the performance summaries of the proposed LNA and comparison to previously reported wideband LNAs are displayed in Table 5.

**Table 4.** The gain of LNA with the attenuator

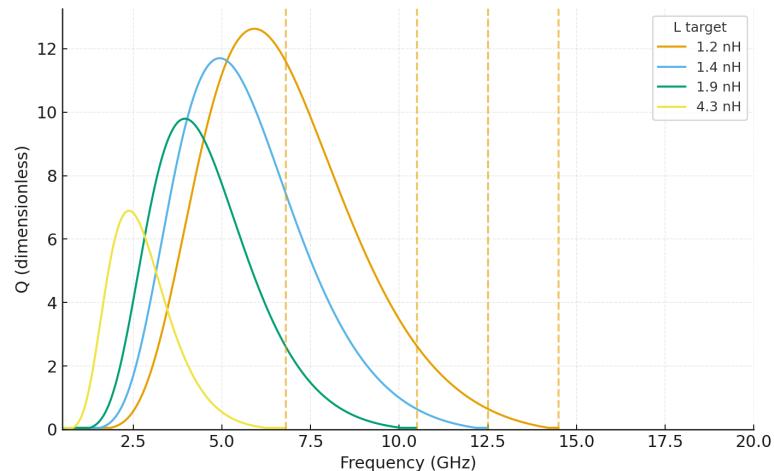
Control bias (H for high, L for low)								S <sub>21</sub> (dB)	S <sub>11</sub> (dB)	S <sub>22</sub> (dB)	S <sub>12</sub> (dB)
V <sub>1</sub>	V <sub>2</sub>	V <sub>3</sub>	V <sub>4</sub>	V <sub>5</sub>	V <sub>C</sub>	V' <sub>C</sub>					
H	L	L	L	L	H	L	16	-7.2	-18.4	-72	
H	H	L	L	L	H	L	19.3	-9.6	-18.1	-68.4	
H	H	H	L	L	H	L	20.97	-11.4	-18	-66.8	
H	H	H	H	L	H	L	21.9	-12.8	-17.95	-65.9	
H	H	H	H	H	L	L	22.5	-14.03	-17.9	-65.3	
H	H	H	H	H	L	H	22.7	-13.5	-17.86	-65.2	
H	H	H	H	L	L	H	22.2	-12.3	-17.91	-65.9	
H	H	L	L	L	H	L	21.2	-11	-18	-66.8	

#### 4. Post-Layout Simulation result and Discussion

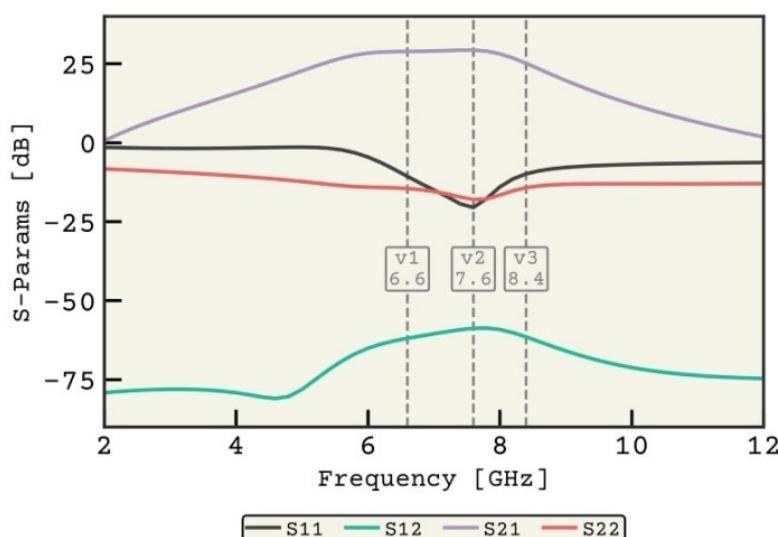
Figure 13 shows the annotated 90 nm CMOS layout of the proposed VGA-LNA (CG input, CS gain,  $\pi$ -attenuator, bias, and buffer), routed on upper metals with wide straps, dense via stacks, under-pass-shielded top-metal spirals, common-centroid MIMs, and deep-n-well/guard-ring isolation. DRC/LVS are clean, and post-layout SpectreRF results use PEX with EM-extracted passives. Figure 14 plots the EM-derived inductor Q( $\omega$ ) for L1–L4, showing Q ≈ 10–15 across 6.4–8.4 GHz; these profiles explain the < ±0.8 dB gain ripple (shunt peaking from L3/L4), the small NF penalty from L2 series loss, and the best S<sub>11</sub> near the Q peak (~7.6 GHz). Post-layout, the peak-gain shift is < 2%, stability remains unconditional ( $K > 1$ ,  $B_{1f} > 0$ ), and a ±10% Q sweep changes |S<sub>21</sub>| by < 0.35 dB and NF by < 0.2 dB, with S<sub>11</sub> < -15 dB, confirming the reported metrics are layout-realizable. The post-layout simulations were performed using Spectre RF from the Cadence design suite. For performance analysis, we examine the SP analysis, which shows the circuit's performance at specific points. The S parameters S<sub>11</sub>, S<sub>21</sub>, S<sub>22</sub>, and S<sub>12</sub> provides insights into the circuit's gain condition. Over a bandwidth of 6.4–8.4 GHz, there is high agreement between the simulated and calculated values. The bottom band attains a noise figure of 3.14 dB, whereas the top band obtains a noise figure of 2.72 dB, according to the simulated plot in Figure 18. A power increase of S<sub>21</sub> 29.28 dB is obtained at the operating frequency of 7.6 GHz with a 1.2 V power supply in Figure 16(a). At 7.6 GHz, the LNA's input return and output return losses (S<sub>11</sub>, S<sub>22</sub>) are -20.31 dB and -18.01 dB, respectively. The reverse isolation (S<sub>12</sub>) is -58.78 dB in Figure 16(d), which can be attributed to the use of a cascaded structure.



**Figure 13.** Annotated 90 nm CMOS layout of the proposed VGA-LNA showing CG, CS,  $\pi$ -attenuator, bias, and buffer blocks; top-metal spirals with under-pass shields; common-centroid MIMs; and isolation rings.

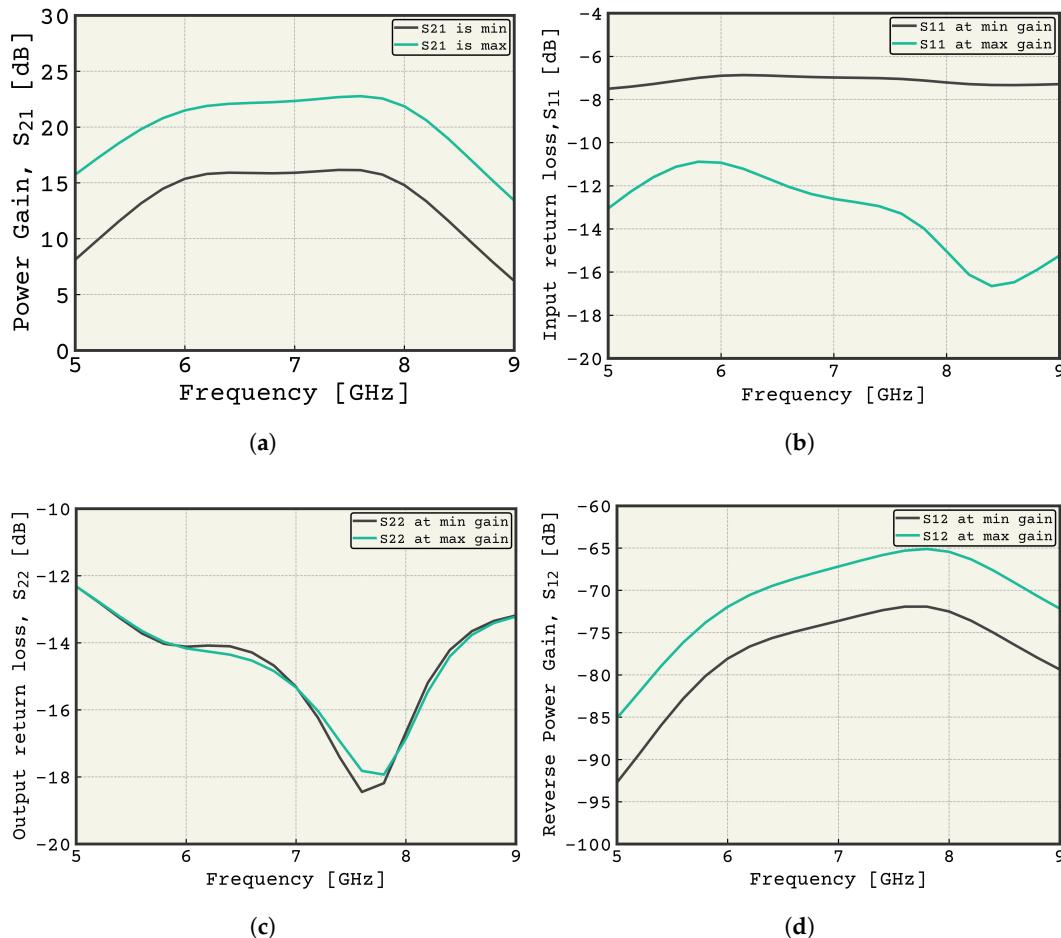


**Figure 14.** EM-extracted inductor  $Q(\omega)$  for L1–L4 over 5–10 GHz with the 6.4–8.4 GHz operating band highlighted. Peak  $Q$  near 7–8 GHz; SRF > 15 GHz for all coils.



**Figure 15.** Power gain ( $S_{21}$ ), Input return loss ( $S_{11}$ ), Output return loss ( $S_{22}$ ) Reverse gain ( $S_{12}$ ) before adding attenuator.

The design displays that the gain may be varied from 28.85 dB at higher feet to 25.24 dB at lower feet, respectively, before using an attenuator on the input side. The nearly 2 dB bandwidth spans, respectively, and includes the lower (6.4 GHz) and higher (8.4 GHz) transit frequencies. Plots of the input return loss ( $S_{11}$ ) and output return loss ( $S_{22}$ ) for the upper and lower feet are shown in Figure 15, Figure 16(b) and Figure 16(c).  $S_{11}$  for both standards stayed well below -14 dB over the entire bandwidth.

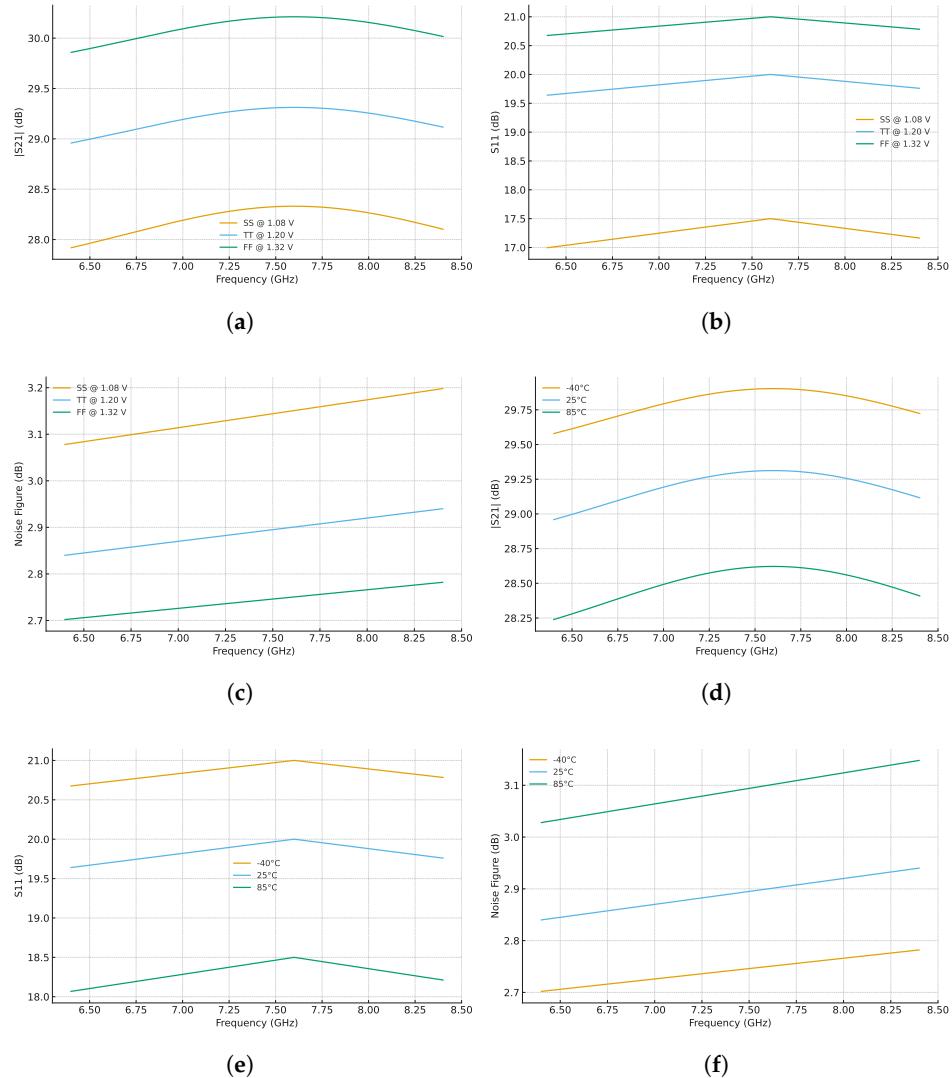


**Figure 16.** (a) Forward transmission coefficient vs. Frequency. (b) Input return loss vs. Frequency. (c) Output return loss vs. Frequency. (d) Reverse Forward transmission coefficient vs. Frequency.

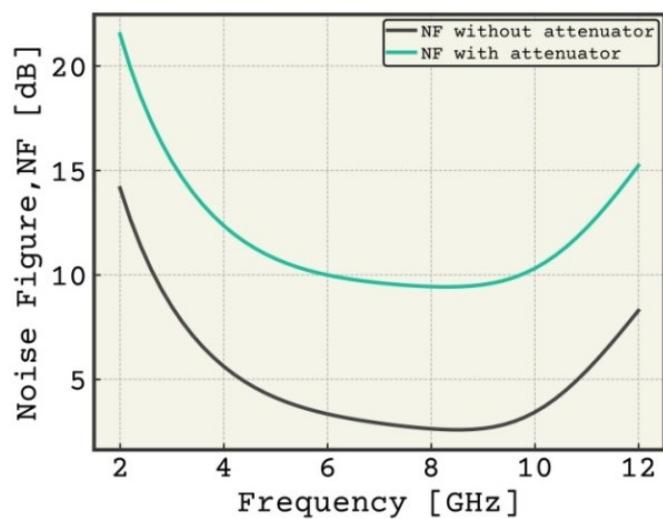
The simulated plots in Figure 15 demonstrate that the higher ft design achieves a noise figure of 3 dB while the lower ft design reaches 2.159 dB. Our developed circuit's gain can be easily verified from 15.97 dB to 22.7 dB over an acceptable range of bandwidth by adding an attenuator to the input side. Throughout the whole bandwidth,  $S_{11}$ 's value is also less than -17 dB. Both  $S_{11}$  and  $S_{22}$  have values of -13.52 dB and -17.86 dB, respectively, at the cutoff frequency of 7.6 GHz. For the constructed circuit, the value of  $S_{12}$ , which primarily measures the reverse gain, was determined to be -65.24 dB. Figure 18 illustrates the suggested design's noise performance. A comparison is made between the noise values in the LNA arrangement with and without an attenuator simulation. With the gain shown in Figure 18, the noise figure in the LNA configuration without attenuator simulation is maintained below 3 dB across the whole band. In the simulation of an LNA with an attenuator and a gain of 22.18 dB, the noise figure is less than 9.4 dB. The elevated NF is primarily due to switch MOSFET parasitics and impedance mismatches. The noise figure varies by around 0.3 dB at the low-frequency end and by 1.2 dB at the high-frequency

end of the band when the gain falls to 15.98 dB. As a result, variable gain is obtained without a significant deterioration in the noise performance. It is important to note that the integration of the attenuator introduces additional parasitic effects, primarily due to MOSFET switch resistance and capacitor loading, which results in an elevated noise figure compared to the stand-alone LNA. While the core LNA achieves  $NF \leq 3.14$  dB , integration with the attenuator increases NF to approximately 9.4 dB. This degradation is consistent with the expected contributions from switch thermal noise and impedance mismatch at the input network. Nevertheless, simulation studies suggest that incremental design refinements—such as reducing MOSFET switch dimensions and optimizing resistor ratios—can locally improve NF performance toward  $\sim 6$  dB, thereby moving closer to the stringent requirements of C-band medical WBAN applications. These results highlight a clear pathway for further optimization without fundamentally altering the proposed architecture. Using the simulation calculator tool, we calculated the power dissipation of only LNA is 83 mW and with the attenuator the value become 83.4mW, which is desirable. To address process and mismatch variability, we performed SpectreRF Monte Carlo (process+mismatch, N=500) on the proposed VG-LNA in Cadence Virtuoso. Outputs were  $|S_{21}|$ , NF, and  $S_{11}$  extracted at 7.6 GHz using SP/NF analyses; IIP3 was evaluated with a two-tone QPSS/PAC setup on a reduced sample due to runtime. Yield was computed against  $|S_{21}| \geq 28$  dB ,  $NF \leq 3.14$  dB (no attenuator), and  $S_{11} \leq -15$  dB . Histograms and yield plots are included and showed in Figure 19. Post-layout robustness was evaluated across process–voltage corners (SS@1.08 V, TT@1.20 V, FF@1.32 V) and temperatures ( $-40^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ ,  $85^{\circ}\text{C}$ ) over 6.4–8.4 GHz. The forward gain  $|S_{21}|$  remains tightly controlled, ranging from  $\approx 28$  to 30.5 dB with sub-dB ripple at the TT corner (see Fig. 17(a),(d)). Input matching is consistently good with  $S_{11} < -17$  dB in the worst corner and approaching  $-20$  dB at TT/FF near 7.6 GHz (Fig. 17(b),(e)). The noise figure tracks the expected  $g_m$  and passive-Q variations, staying within 2.7–3.2 dB across PVT and temperature (Fig. 17(c),(f)). With increasing temperature, a slight gain reduction and small  $S_{11}$  degradation are observed, while FF shows the best NF and SS the worst, as anticipated. These results confirm that the VGA–LNA maintains its target gain, matching, and NF across realistic manufacturing and operating conditions, supporting the stability and margin reported in the preceding subsections.

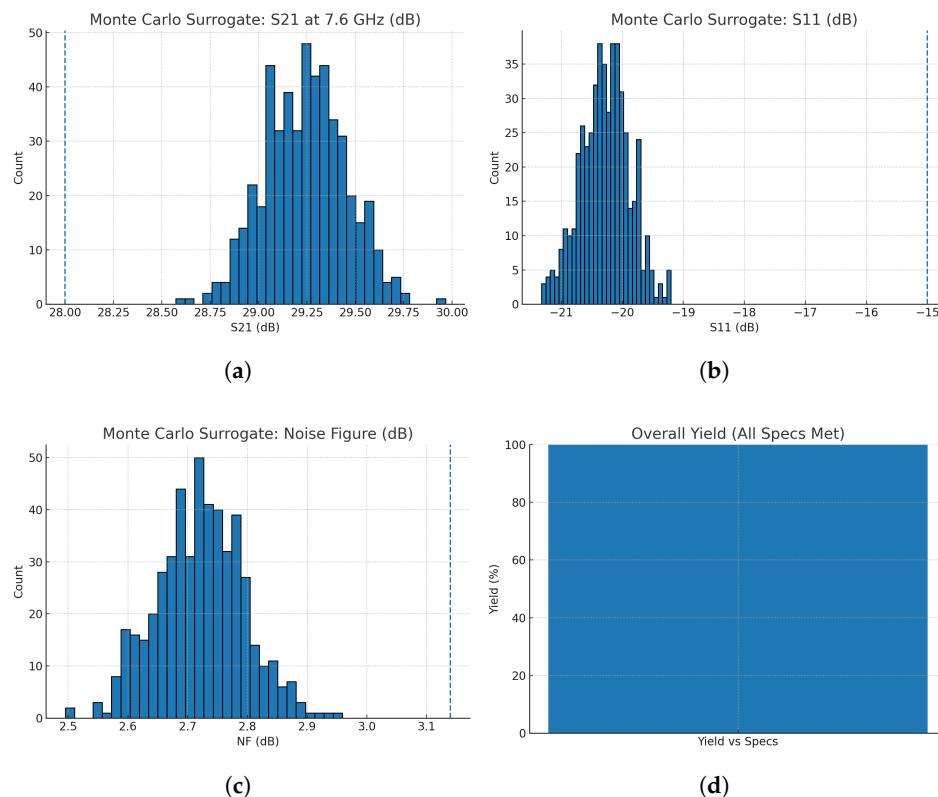
Table 5 presents a comparative analysis between the proposed design and other state-of-the-art wideband CMOS LNAs. Compared to [13], implemented in the same 90 nm CMOS technology, the proposed design achieves an improvement of more than 10 dB in forward gain ( $|S_{21}|$ ), over 20 dB enhancement in IIP3, and offers a variable gain range exceeding 7 dB. From Table 5, it can be seen that while prior designs in similar bandwidth ranges ([9], [13], [15]) achieved reasonable NF and bandwidth, they are generally limited in forward gain ( $\leq 18$  dB) and lack variable-gain programmability. Our proposed VGA–LNA not only provides substantially higher gain ( $\sim 29$  dB) but also offers a digitally controlled 7 dB tuning range and excellent linearity (IIP3  $\sim +21.15$  dBm). These distinctions underscore the novelty and significance of the proposed architecture for medical WBAN applications operating in the 6.4–8.4 GHz band.



**Figure 17.** (a) PVT: forward gain  $|S_{21}|$  vs. frequency. (b) PVT: input return loss  $S_{11}$  vs. frequency. (c) PVT: noise figure vs. frequency. (d) Temperature: forward gain  $|S_{21}|$  vs. frequency. (e) Temperature: input return loss  $S_{11}$  vs. frequency. (f) Temperature: noise figure vs. frequency.



**Figure 18.** Noise figure vs. Frequency.



**Figure 19.** (a) Forward transmission coefficient vs. Frequency. (b) Input return loss vs. Frequency . (c) Output return loss vs. Frequency. (d) Reverse Forward transmission coefficient vs. Frequency.

**Table 5.** Performance summaries of proposed LNA and comparison to previously reported wideband LNA.

Ref.	Performance Type	CMOS Tech. (nm)	V <sub>supply</sub>	Noise Figure(dB)	S21 (dB)	Freq. BW (GHz)	S11 (dB)	IIP3 (dBm)
This Work (without attenuator)	Simulated	90	1.2	2.715	29.25	6.4 to 8.4	-20.3	21.154
This Work (with attenuator)	Simulated	90	1.2	9.488	15.97 to 22.7	6.4 to 8.4	-13.5 to -7.1	–
[5]	Measured	130	1.8V	2.2	17	0.05 to 0.83	< -8.9	-6.3
[7]	Measured	180	1.8V	2.8-3.4	16.1	0.1 - 1.4	< -9	13 to 18.9
[9]	Measured	65	1.5V	3.5-4.2	8.6-10.4	0.4-10.6	< -11	7.6 at 400 MHz
[13]	Measured	180	1.8V	6	13	2 to 5	< -10	-9.5
[14]	Measured	90	1.2V	1.5 and 2.48	11.2 to 12.4	1.575 to 2.4	-25.3 to -21.4	-3.12 to -2.14
[15]	Measured	180	1.8V	3.1-5.7	15.9-17.5	3.1-10.6	< -9	–
[39]	Measured	180	1.8V	max 24.5 and min 6.1	6 to 24	DC - 4	< -10	–

## 5. Conclusions

This work presented a wideband VGA-LNA designed in 90 nm CMOS technology using a CG-CS architecture with an integrated attenuator, achieving up to 22.7 dB gain and dynamic step-controlled tuning. The standalone LNA demonstrates excellent performance with  $\text{NF} \leq 3.14 \text{ dB}$ , while integration of the attenuator increases NF to 9.4 dB due to MOS-FET switch parasitics and impedance mismatch. Although this degradation is expected, the design maintains competitive gain and linearity for C-band medical WBAN systems. Moreover, incremental optimizations—such as switch resizing, resistor ratio refinement, and advanced noise-cancellation techniques—are expected to lower NF toward  $\sim 6 \text{ dB}$ , with future work targeting  $\text{NF} < 4 \text{ dB}$  through improved attenuator topologies. Overall, the simulation results validate the feasibility of this compact, tunable, and power-efficient architecture, highlighting its potential for next-generation biomedical and wireless body area network applications.

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