PES UNIVERSITY

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100-ft Ring Road, Bengaluru – 560 085, Karnataka, India

Report on

‘Pulse Generator’

Submitted by

Nishchal A V (PES1UG21EC169)

L Sathya Suryanarayana Sharma (PES1UG21EC135)

Sudharshan M (PES1UG21EC140)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PES UNIVERSITY

BENGALURU - 560 085

FACULTY OF ENGINEERING

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1. Introduction

A **pulse generator** is an electronic circuit that generates a **series of electrical pulses**, with a specific **frequency and width**. The circuit can be designed with a variety of circuit topologies and technologies, depending on the application's need. Some can be done using astable multivibrators, monostable multivibrators, and pulse width modulators. And they can be fabricated using a variety of process technologies, such as CMOS, BiCMOS, etc.

Think of it like a machine that creates a regular "beep" sound, but instead of sound waves, it produces electrical pulses (**Short bursts of electrical energy**). This allows engineers to create and control precise electrical signals for various purposes.

Pulses can be customized to have a **specific property**, such as their **frequency** (how often they occur), **amplitude** (maximum voltage level of each pulse), **rise time and fall time** (how quickly the pulse voltage rises and falls), and **width** (how long they last). They can be found in many different types of electronics in daily life, from communication systems to scientific equipment to household components (TV for example).

The type of signals a pulse generator can produce depends on the specific design of the circuit, but typical used/generated signals are:

- Square waves (Alternates between two voltage levels)
    - Digital circuits as clock signals, testing purpose
- Pulse Train (Series of electrical pulses with a fixed duration and repetition rate)
    - Used in communication systems, triggering, and synchronization purposes.
- Sawtooth waves (Ramps up and down in voltage)
    - Display and imaging systems, as well as for testing and measurement purposes.
- Triangular waves (Ramps up and down in voltage)
    - Used in audio and video equipment, also for testing and measurement purposes.

- Sine waves (Smooth, oscillating waveform)
    - Audio and communications systems, testing, and measurement.

The pulse shape is determined by the **timing circuit** and the **output stage of the pulse generator.**

Advantages of using a pulse generator:

- Precise timing
- High-frequency operation
- Adjustable pulse width and frequency
- Compact size and portability
- Ease of use and versatile applications

Drawbacks / Disadvantages of using a pulse generator:

- Limited frequency range and limited pulse duration
    - These limit the usefulness of the pulse generator.
- Output signal distortion
    - Can be of concern when generating very short or very long pulses, or when working with high-frequency signals.
- Noise and interference with other circuits
    - Pulse generators can generate **electromagnetic interference (EMI)** that can affect other nearby circuits or devices. Hence, it is important to shield the pulse generator and use appropriate grounding and shielding techniques to minimize EMI.
- Power consumption
    - Can sometimes consume a significant amount of power and this can affect the devices which are battery-powered or portable devices.
- Timing errors
    - can be affected by several factors such as temperature, power supply noise, etc.

Applications of pulse generator:

- IR receiver: It is used to receive signals from the remote control. The receiver uses a pulse generator to generate a clock signal that is used to decode the modulated IR signal from the remote control
- Crystal Oscillator: A crystal oscillator is a type of oscillator that uses a quartz crystal resonator to generate a stable clock signal. (Used to synchronize various components in electronic devices)
- Pulse width modulator: A pulse width modulator (PWM) is used to generate control signals for controlling the brightness of the display backlight (in Television). The PWM generates a train of pulses with variable widths and repetition rates, which are used to control the amount of current flowing through the backlight.
- Audio and Video equipment: To generate various types of signals, such as sync signals for display devices, and audio signals for speakers and headphones.
- Medical Equipment: Equipment such as electrocardiographs (ECGs), to generate electrical signals for monitoring and diagnosing various medical conditions.
- Similarly, they can be found in many applications regarding telecommunications, measurement equipment, scientific research, control systems, power electronics, medical equipment, and audio and video equipment.

The specific types and configurations of pulse generators used can vary widely depending on the specific application and requirements.

While some potential issues can be seen when using pulse generators, these issues can be addressed through careful design and proper usage of pulse generators.

Overall, pulse generators play an important role in many electronic and scientific applications, and their **precise** and **accurate** pulse generation capabilities make them an essential tool for engineers, and scientists.

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2. Block Diagram

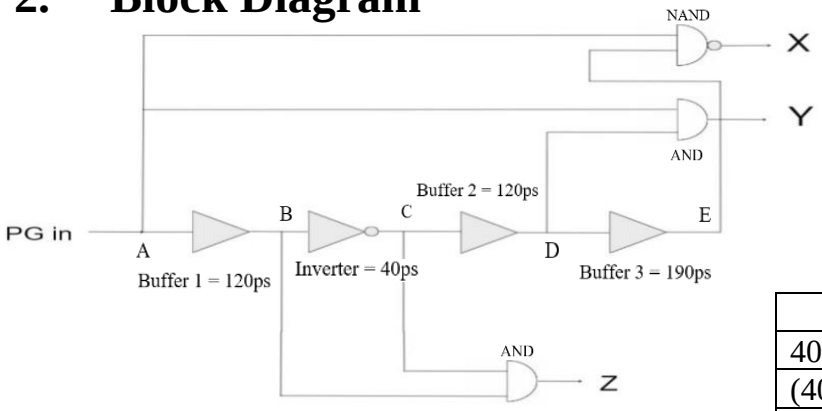

Fig.1 Block Diagram

Table.1 Expression

Expression
NAND = $\overline{AB}$
AND = AB

Table.2 Delay Relation

Delay relation
40ps
(40) × (3) = (120ps)
(120) + (70) = (190ps)

PGin: input received by the pulse generator block from other blocks in series with it.

X, Y, and Z are the output pins of NAND, AND, AND gates.

Table.3 Pulse generation

Node A	Node B	Node C	Node D	Node E	Logic Gate	Pulse(Y/N)
1	-	-	-	1	NAND (X)	Yes
1	-	-	1	-	AND (Y)	Yes
-	1	1	-	-	AND (Z)	Yes

Aim: Generate 3 different pulses of different pulse widths with their respective delays.

Observation:

- From ***Table.1*** we can see that NAND gate output is always high and it only falls when node A and node E are logic 1.
- Both the AND gate output is always low and only rises when nodes A, B, C, and D are logic 1. As we see, our circuit generates a **square pulse signal.**

Steps:

- Check the circuit output with only inverters and buffers. And verify the output.
- Add the NAND and AND gates to the circuit. (Note: They induce some percentage of delay to the overall circuit).
- Give width (w) value 'ranges' for pmos and nmos of buffers and inverter and check the output waveform along with the delays obtained.
- Start incrementing or decrementing width values concerning what delay you want. ***(Note: PMOS 'w' and NMOS 'w'*** $\propto \frac{1}{Resistance}$ **, which in-turn gives delay** ***)***
- By giving ranges we find the suitable width values, which give the required delay.

3. Schematic and Simulation Results

Circuit Designed using Tanner tool:

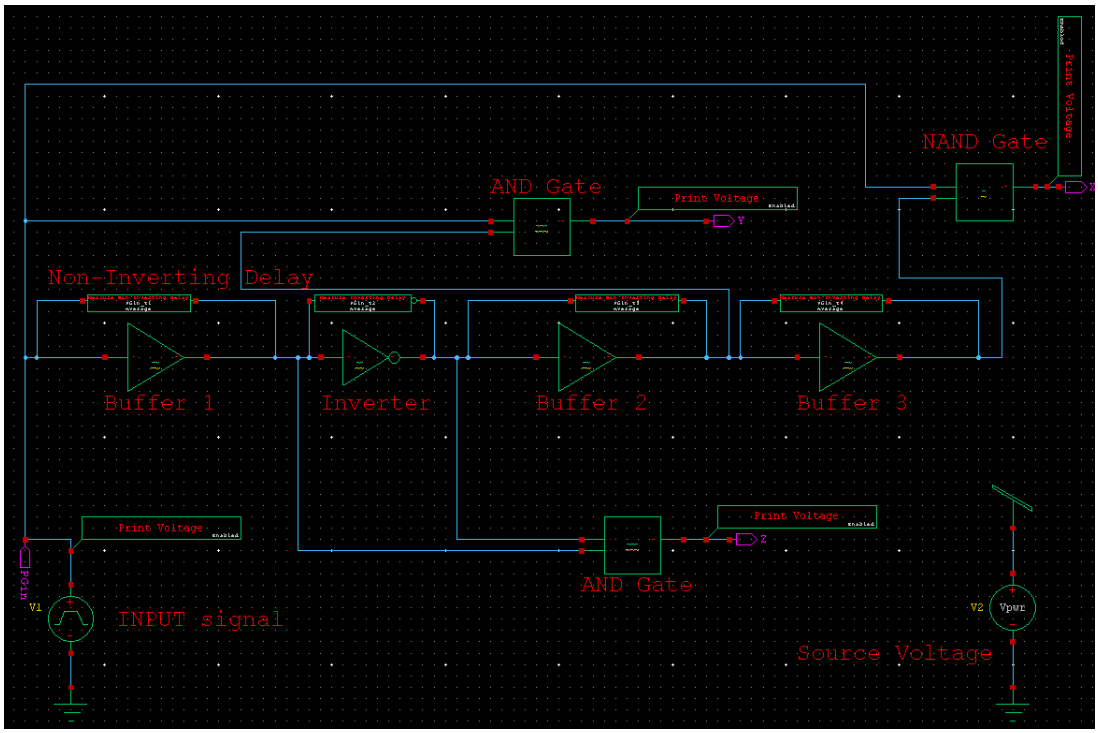

Fig.2 Pulse Generator Circuit design

Transient/Fourier Analysis	
Stop Time	100n
Maximum Time Step	0.01n
Print Start Time	0
Print Time Step	0.01n
Use Initial Conditions	False
Startup Mode	Op

Fig.3 Transient analysis parameters

Low Voltage	0
High Voltage	3.3
Period	50n
Rise Time	1p
Fall Time	1p
Time Delay	5n
Pulse Width	24.999n
Frequency	20M
Rounding Distance	0

Fig.4 V-Pulse Parameters

-Transient Analysis of Fig.1 when only inv and buffers are present:

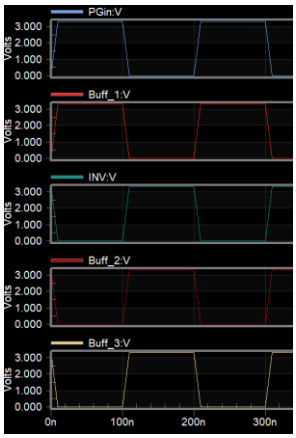

Fig.6 Output of inv and buff

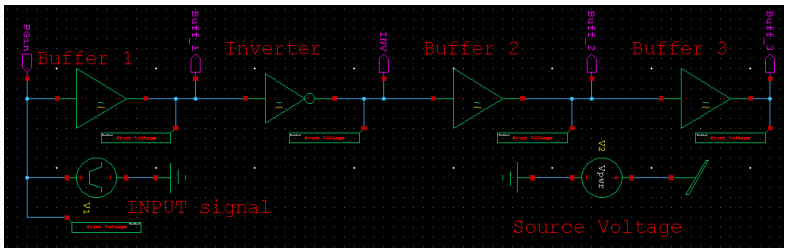

Fig.5 Circuit with only inv and buffer

-From ***Fig.6*** we can infer that Inverters and Buffers output is proper

Case 1: Generating the output with the desired delay results seen in the Question

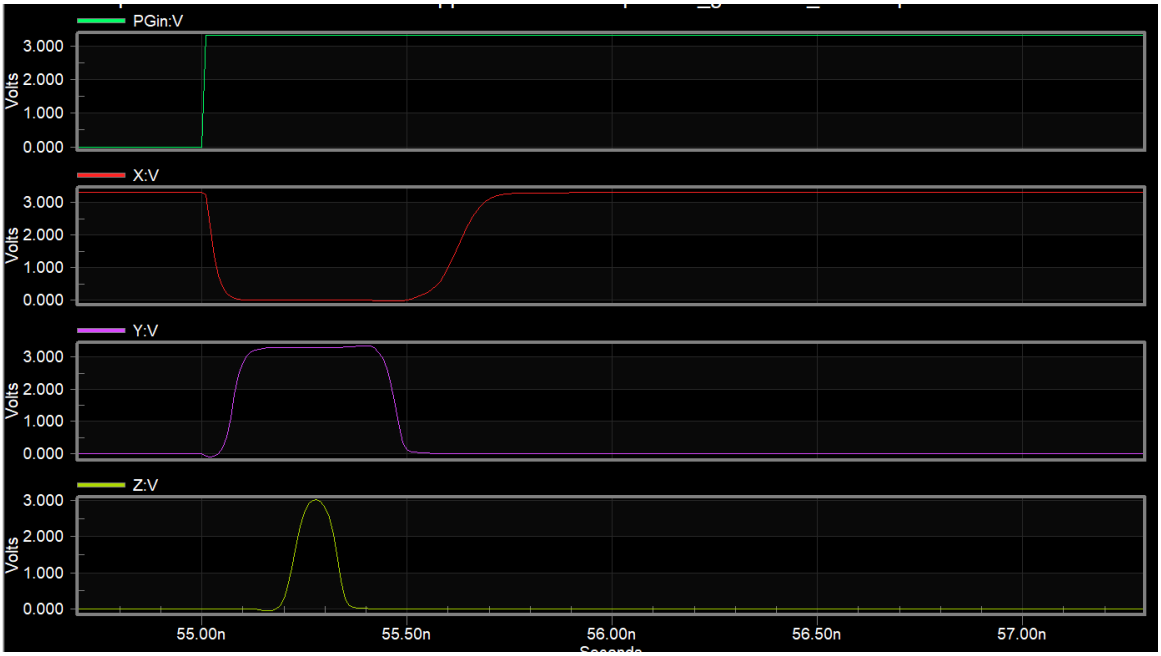

Fig.7 Transient analysis for Case 1

Table.4 Delay values

Component	Delay
Buffer 1	120.96ps
Inverter	85.36ps
Buffer 2	120.84ps
Buffer 3	190.49ps

Power dissipation of case 1 is shown in ***Fig.8***

```
vv2 from time 0 to 1e-07
Average power consumed -> 9.278848e-05 watts
Max power 3.527985e-01 at time 5.0005e-09
Min power 2.751745e-09 at time 3.36687e-09
```

Fig.8 Power Dissipation of source voltage (Case 1)

→**W = Width** values given to the components are shown in ***Table.5***

Table.5 Width values (Case 1)

Component	PMOS	NMOS
Buffer 1	6.8u	950n
Inverter	3u	600n
Buffer 2	6.4u	1.7u
Buffer 3	9u	450n

Case 2: Generating the output in terms of the delay relation seen in the Question

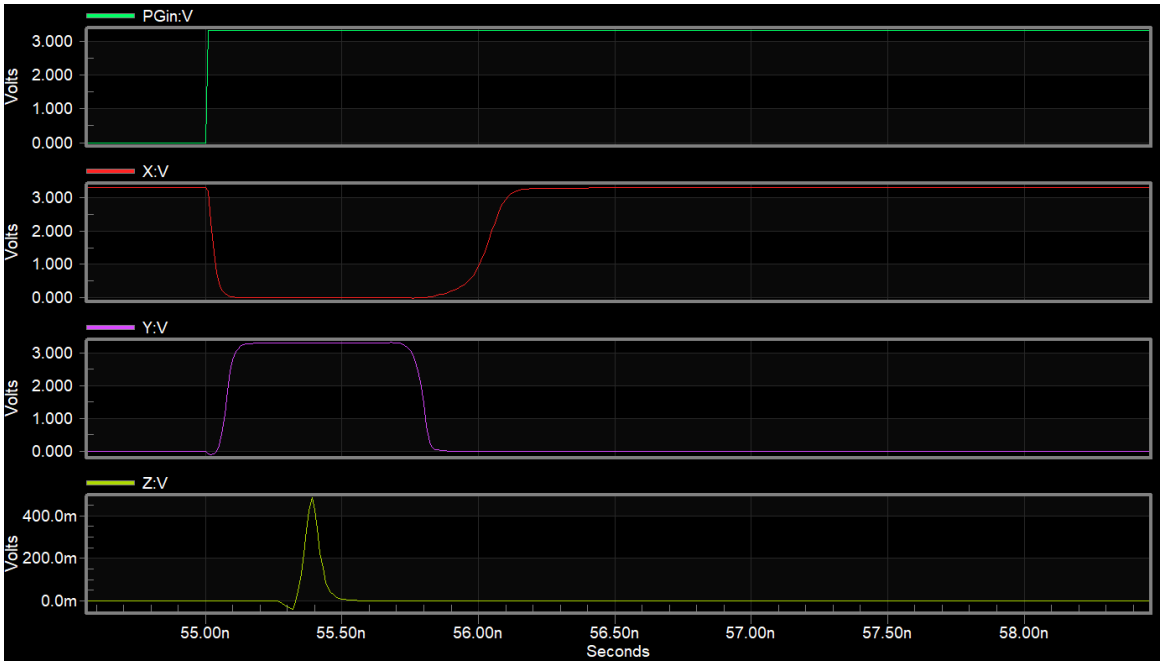

Fig.9 Transient analysis for Case 2

Table.6 Delay values

Component	Delay	Calculation (expected)
Buffer 1	255.77ps	(85) × (3) = (255ps)
Inverter	85.61ps	85ps
Buffer 2	225.82ps	(85) × (3) = (255ps)
Buffer 3	325.33ps	(225) + (70) = (325ps)

Power dissipation of case 2 is shown in ***Fig.10***

```
vv2 from time 0 to 1e-07
Average power consumed -> 1.919160e-04 watts
Max power 9.973558e-01 at time 5.50005e-08
Min power 4.986124e-09 at time 1.38687e-09
```

Fig.10 Power Dissipation of source voltage (Case 2)

→**W = Width** values given to the components are shown in ***Table.7***

Table.7 Width values (Case 2)

Component	PMOS	NMOS
Buffer 1	25.1u	1u
Inverter	6u	2.4u
Buffer 2	19.4u	1u
Buffer 3	18.7u	350n

Case 3: Better z pulse width and amplitude along with proper relations of delays

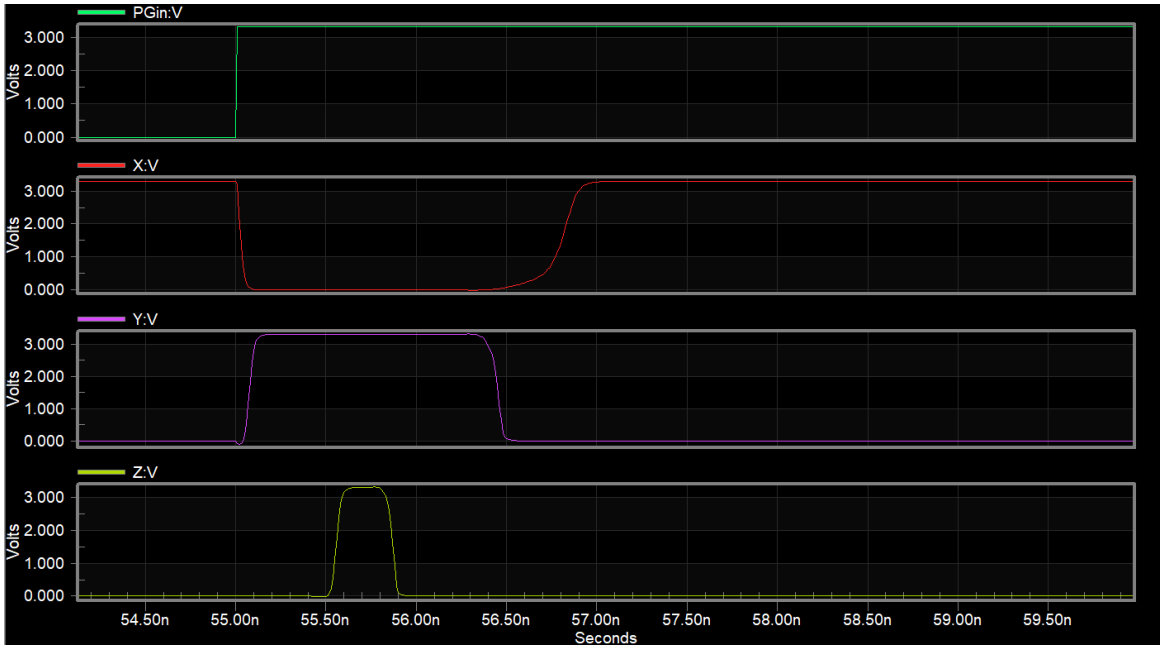

Fig.11 Transient analysis for Case 3

Table.8 Delay values

Component	Delay	Calculation (expected)
Buffer 1	450.78ps	(150) × (3) = (450ps)
Inverter	150.96ps	150ps
Buffer 2	450.36ps	(150) × (3) = (450ps)
Buffer 3	520.37ps	(450) + (70) = (520ps)

Power dissipation of case 3 is shown in ***Fig.12***

```
vv2 from time 0 to 1e-07
Average power consumed -> 3.405011e-04 watts
Max power 1.037077e+00 at time 5.50005e-08
Min power 7.350212e-09 at time 4.86875e-10
```

Fig.12 Power Dissipation of source voltage (Case 3)

→**W = Width** values given to the components are shown in ***Table.9***

Table.9 Width values (Case 3)

Component	PMOS	NMOS
Buffer 1	25.95u	500n
Inverter	12.5u	1.3u
Buffer 2	36.95u	1u
Buffer 3	48.85u	450n

Case 4: Reducing the x output rise time in Case 1

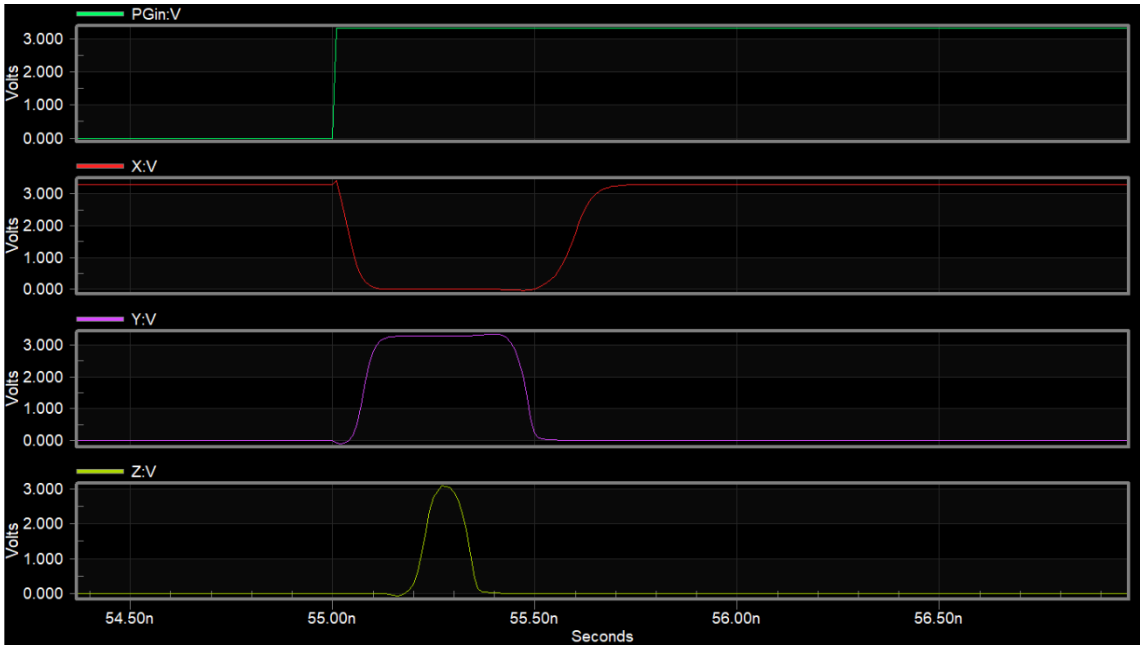

Fig.13 Transient analysis for Case 4

Table.10 Delay values

Component	Delay	Calculation (expected)
Buffer 1	120.46ps	(85) × (3) = (120ps)
Inverter	85.34ps	85ps
Buffer 2	121.50ps	(85) × (3) = (120ps)
Buffer 3	191.00ps	(120) + (70) = (190ps)

Power dissipation of case 4 is shown in ***Fig.14***

```
vv2 from time 0 to 1e-07
Average power consumed -> 8.978433e-05 watts
Max power 3.223671e-01 at time 5.50005e-08
Min power 3.078345e-09 at time 4.66875e-10
```

Fig.14 Power Dissipation of source voltage (Case 4)

→**W = Width** values given to the components are shown in ***Table.11***

Table.11 Width values (Case 4)

Component	PMOS	NMOS
Buffer 1	6.75u	950n
Inverter	3u	550n
Buffer 2	5.8u	1.7u
Buffer 3	10u	450n

NAND Gate width values (x output)	
PMOS	NMOS
800n	350n

4. Observation

→Case 1: We can infer from ***Table.4*** that we can get the required delays of Buffer 1, Buffer 2, and Buffer 3. But we see that we are not able to get the required Inverter delay. This is because of the constraint induced by the 250nm technology node that we are using. Going below 70ps for the inverter distorts the Z output (***Fig.7***) but cuts its peak voltage and gives some noise (due to the less delay of the inverter we observe a race condition). Hence, we have kept the inverter delay to be in 85ps. We also see that there is an increase in rise time for output X (***Fig.7***).

→Case 2: From ***Table.6*** we can see that we tried to get the delay relations which was shown in ***Table.4*** and we can notice from ***Fig.9*** that there is a dip in Z voltage to around 400nm, which is not desired. This is because the inverter delay is very less compared to other components' delay, hence we are not able to reach the peak voltage of 3.3V.

→Case 3: From ***Table.8,*** we increased the Inverter delay from 85ps to 150ps, and we can observe that we can reach the desired peak voltage of 3.3V of output Z in ***Fig11***. Also, we can see that we have maintained the respective delay relations seen in ***Table.2***.

→Case 4: This case deals with correcting Case 1 output X (***Fig.7***) rise time waveform. By changing the width values in the NAND gate (***Table.11***) we can correct the rise time. This in turn changes the delay of the overall circuit. (***Refer Table.11 and Fig.13***)

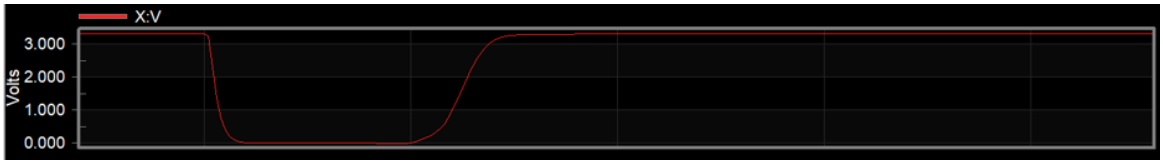

Fig.15 X-Output waveform (Case 1)

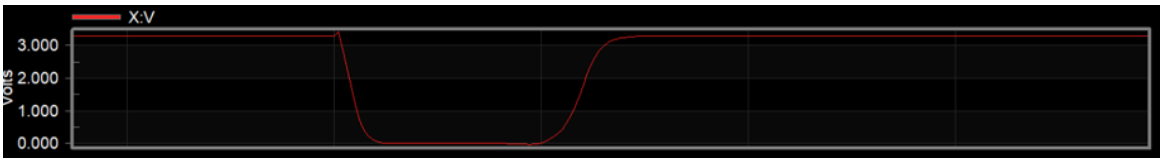

Fig.16 X-Output waveform (Case 4)

Comparing ***Fig.15*** and ***Fig.16*** we can say that Case 4 has the best waveform with satisfying delays. But before we conclude we need to do a bit more of an analysis.

Tabulating Data:

Table.12 Width values of all cases

Case	Transistor	Buffer 1	Inverter	Buffer 2	Buffer 3	NAND
1	PMOS	6.8u	3u	6.4u	9u	1.5u
	NMOS	950n	600n	1.7u	450n	1.5u
2	PMOS	25.1u	6u	19.4u	18.7u	1.5u
	NMOS	1u	2.4u	1u	350n	1.5u
3	PMOS	25.95u	12.5u	36.95u	48.95u	1.5u
	NMOS	500n	1.3u	1u	450n	1.5u
4	PMOS	6.75u	3u	5.8u	10u	800n
	NMOS	950n	550n	1.7u	450n	350n

Table.13 Delay values of all cases

Case	Buffer 1	Inverter	Buffer 2	Buffer 3	Total Delay
1	120.96ps	85.36ps	120.84ps	190.49ps	517.65ps
2	255.77ps	85.61ps	225.82ps	325.33ps	892.53ps
3	450.78ps	150.96ps	450.36ps	520.37ps	1.592ns
4	120.46ps	85.34ps	121.50ps	191.00ps	518.3ps

Table.14 Power Dissipation of all cases

Case	Power Dissipation
1	Avg: 9.27×10^{-5} W Max: 3.52×10^{-1} W @ 5×10^{-9} sec Min: 2.75×10^{-9} W @ 3.36×10^{-9} sec
2	Avg: 1.91×10^{-4} W Max: 9.97×10^{-1} W @ 5.5×10^{-8} sec Min: 4.48×10^{-9} W @ 1.38×10^{-9} sec
3	Avg: 3.405×10^{-4} W Max: 1.037 W @ 5.5×10^{-8} sec Min: 7.35×10^{-9} W @ 4.86×10^{-10} sec
4	Avg: 8.97×10^{-5} W Max: 3.22×10^{-1} W @ 5.5×10^{-8} sec Min: 3.07×10^{-9} W @ 4.66×10^{-10} sec

5. Conclusion

- To get the desired delays we must keep the width value of pmos 2-3 times more than nmos width. (***Mobility of holes and electrons depend on Resistance == produce delay)***
- Increasing the width value in pmos *reduces the resistance* and decreasing the width value in nmos *increases the resistance*. Controlling the resistance gives delays.
- To get a visible output and not some noise we give small transient time (***Fig.3***), this also enables us to get a zoomed-in waveform. And by keeping the period less we can generate more pulses given that the transient was made less.
- By changing the rise time and fall time parameters in the V-Pulse (***Fig.4)*** we can estimate the cause of noise signals in the negative edge of PGin. Hence, by giving the parameters as zero we tend to get a more ideal case output but we also tend to get sharper edges without giving rise to any proper square shaped pulse in the output and we also notice that there is a small burst of voltage at the negative edge of PGin. To rectify this we can give a small bit of rise and fall time for the input pulse. This to some extent reduces the overshoot that was seen **(from a signal dip in the negative edge of PGin seen in output X (NAND gate) we reduced the noise from 2.6 to 3.1 V (Note: output X keeps the signal high (3.3V) throughout the transient time and only dips at the positive edge of the PGin, if the signal dips anywhere else by any amount less than 3.3V we consider that to be some noise)).**
- From ***Table.12, Table.13, Table.14*** we can now conclude on which is the best parameters for our design
    - In ***Table.12*** we can see that Case 4 has small width values for both pmos and nmos when compared to all the other cases.
    - In ***Table.13*** we can see that Case 4 has almost the same delay as Case 1
    - In ***Table.14*** we can see that Case 4 has less average power dissipation when compared to all the other cases.
- Hence, we can say that for out circuit Case 4 is the best and Case 3 is the worst as average power dissipation is very high (***Table.14***) from all the other cases.
- But if the design needs to have the delay relations, then Case 3 can be choosen
- **Therefore Pulse width of X>Y>Z is successfully achieved.**

6. References

Understanding of Circuit and its respective delay:

- 2.4-GHz Area-Efficient and Fast-Locking Subharmonically Injection-Locked Type-I PLL (IEEE paper on VLSI Vol.28, Nov 2020)

Pulse generator theory and its advantages, disadvantages and application its working process:

- Wikipedia.org
- Net search regarding working principle of pulse generators and few daily life examples were taken for better understanding.

Understanding width-resistance relations with respect to pmos and nmos:

- www.electronics.stackexchange.com
- Wikipedia regarding how transistors work
- Forum for Electronics (edaboard.com):
    - to understand how width has relation with resistance and dealy.

To check any parameters regarding the tool:

- Tanner tool parameter guide
- www.electronics.stackexchange.com (website)
