

Basic Electronics :- (BE)

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Electrical

→ Electrical device is made up of the material like conductors.

→ The power level or voltage level in electrical is very large. (220V peak voltage).

→ The frequency of operation of electrical circuit is very small. (50 Hz or 60 Hz).

→ The size of electrical devices is very large.

Electronics

→ Electronics devices are made up of materialise semi-conductor. (ex-Si, Ge...)

→ The power level or voltage level in electronics is very small (in milli volt range mv).

→ The frequency of operation of electronics circuit is very large.

(MHz, GHz, THz :)

\downarrow \downarrow \downarrow
 10^6 10^9 10^{12}

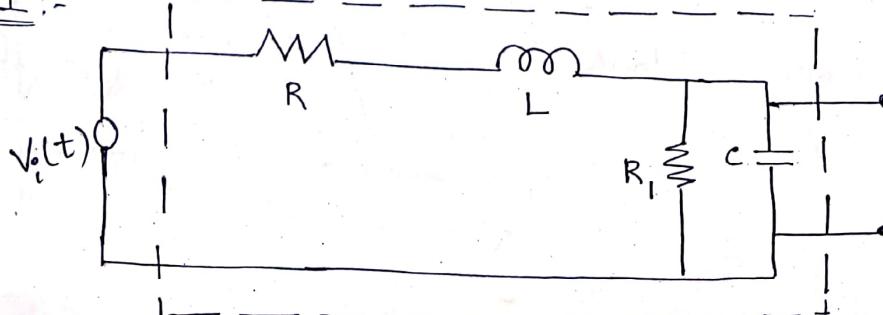
→ The size of the electronics devices is very small.

Signal :-

→ Signal is a physical quantity, which is function of one or more than one independent variable like 't' or special variable. (x, y, z, \dots).

Example:- voltage, current, power, temperature, distribution, speech signal, image signal, video signal. (Audio)

Ex-1 :-



The output of electrical circuit consisting of a passive element like resistance, conductors and inductors may be sinusoidal signal.

$$V_o(t) = V_m \sin \omega_o t$$

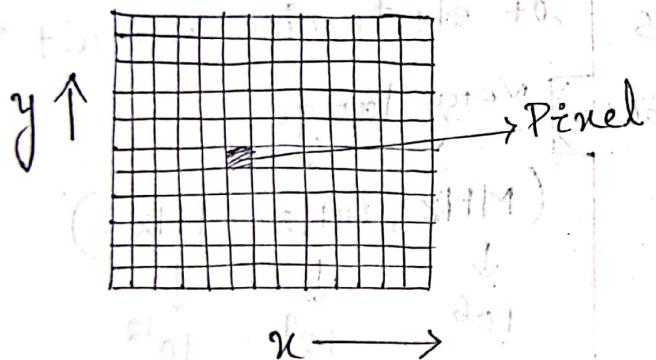
Ex:2 :-

Physical
domain
Signal

Transmitte

Audio
Recorder

Ex:3 :-



Tent Book :-

① Electronics Device & Circuit by Boylestads (EDC)

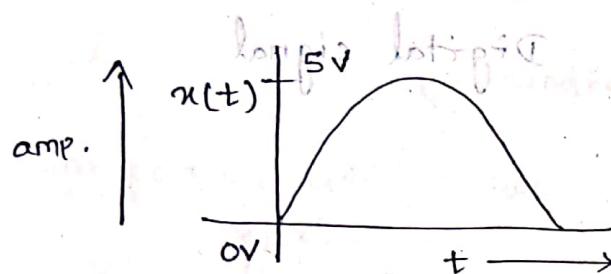
② Micro-electronics by Sedra & Smith.

③ Electronics device & circuit by Millman and Halkin.

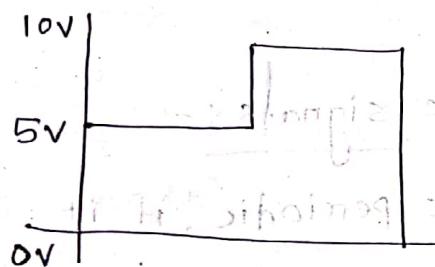
Analog signal & digital signal :-

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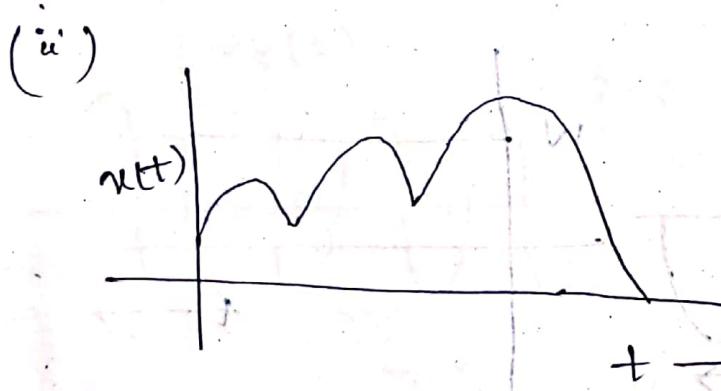
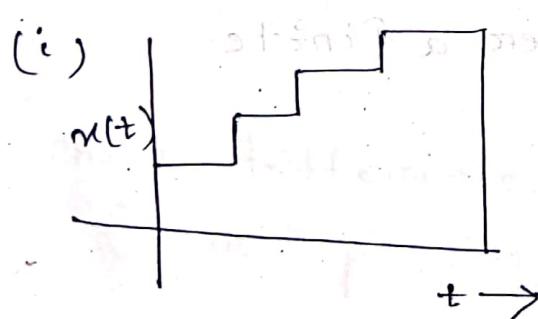
→ A signal is said to be analog signal, if the signal having an infinite no. of amplitude levels or amplitude states.



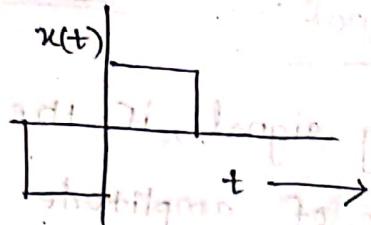
→ A signal is said to be a digital signal, if the signal is having a finite no. of amplitude levels or amplitude states.



Q:- classify the following signals as analog and digital signal.

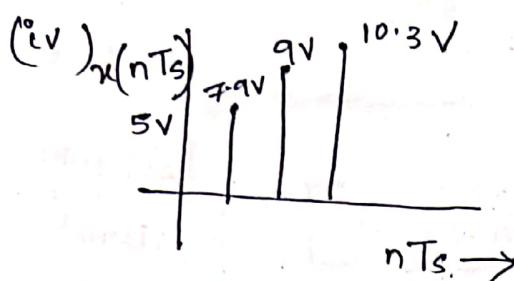


(iii)



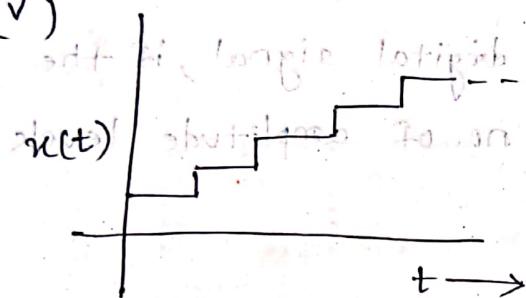
Digital signal

(iv)



Digital signal

(v)



Periodic and non-periodic signals :-

→ A signal is said to be periodic, if it

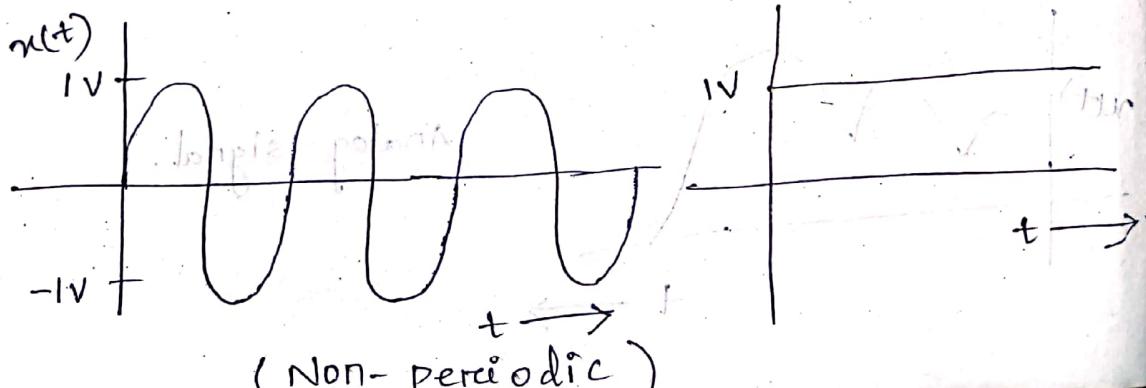
satisfies the following condition :-

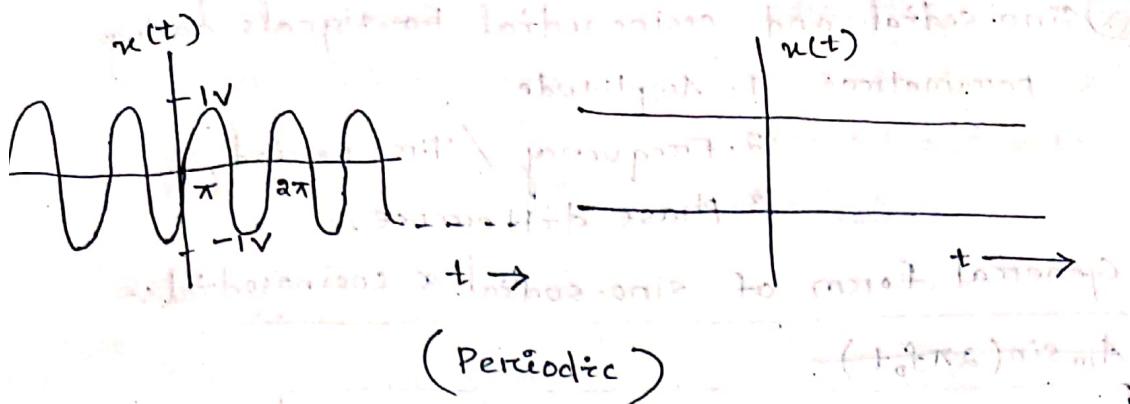
① Signal must be everlasting. (i.e; it must exist from $-\infty$ to $+\infty$.)

② It should be repeated over a finite interval of time.

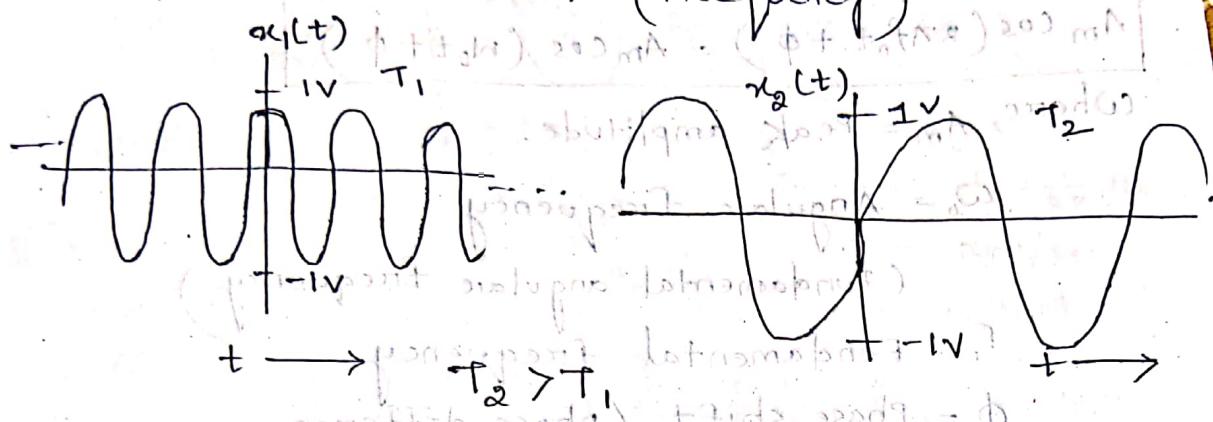
Otherwise, non-periodic.

Ex:-

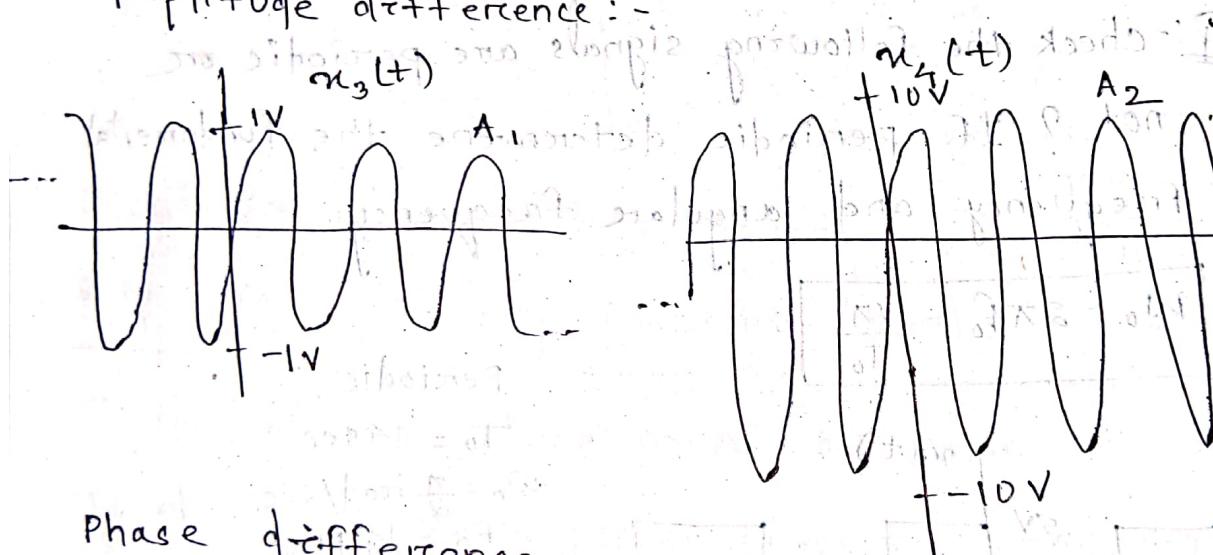




Time period difference :- (Frequency)

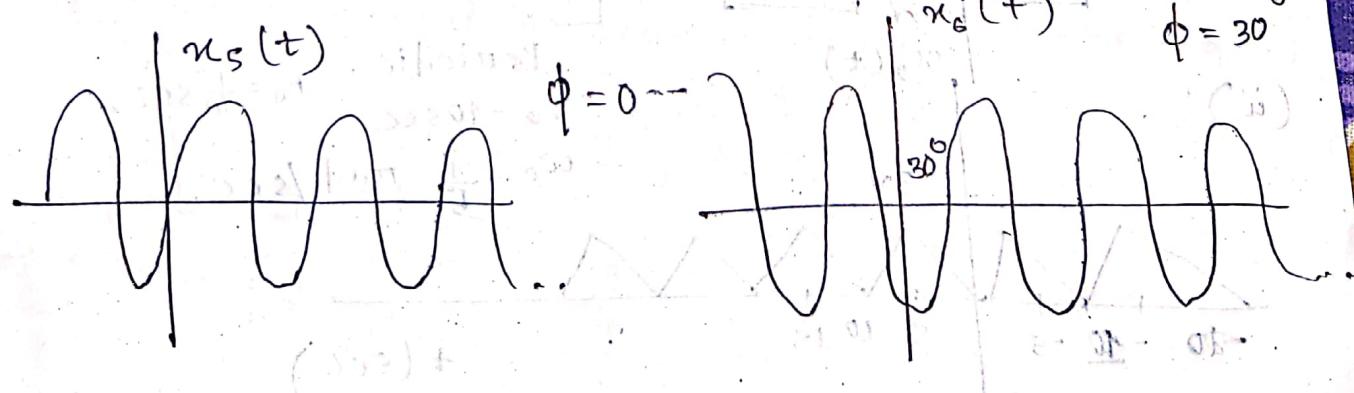


Amplitude difference :-



Phase difference :-

(starting point)



* Sino-sodical and cosinosodical ~~to~~ signals having

3 parametres. 1. Amplitude

2. Frequency / Time period.

3. Phase difference.

General form of sino-sodical & cosinosodical:-

$$A_m \sin(2\pi f_0 t)$$

(Cosine)

$$A_m \sin(2\pi f_0 t + \phi) = A_m \sin(\omega_0 t + \phi)$$

$$A_m \cos(2\pi f_0 t + \phi) = A_m \cos(\omega_0 t + \phi)$$

Where, A_m = Peak amplitude.

ω_0 = Angular frequency

(Fundamental angular frequency)

f_0 = Fundamental frequency

ϕ = Phase shift / phase difference

Q:- check the following signals are periodic or not? If periodic determine the fundamental frequency and angular frequency.

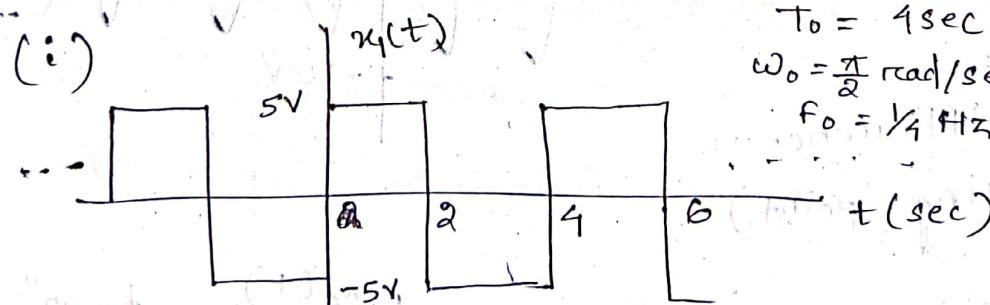
$$\omega_0 = 2\pi f_0 = \frac{2\pi}{T_0}$$

Periodic.

$$T_0 = 1 \text{ sec}$$

$$\omega_0 = \frac{\pi}{2} \text{ rad/sec}$$

$$f_0 = 1/4 \text{ Hz}$$

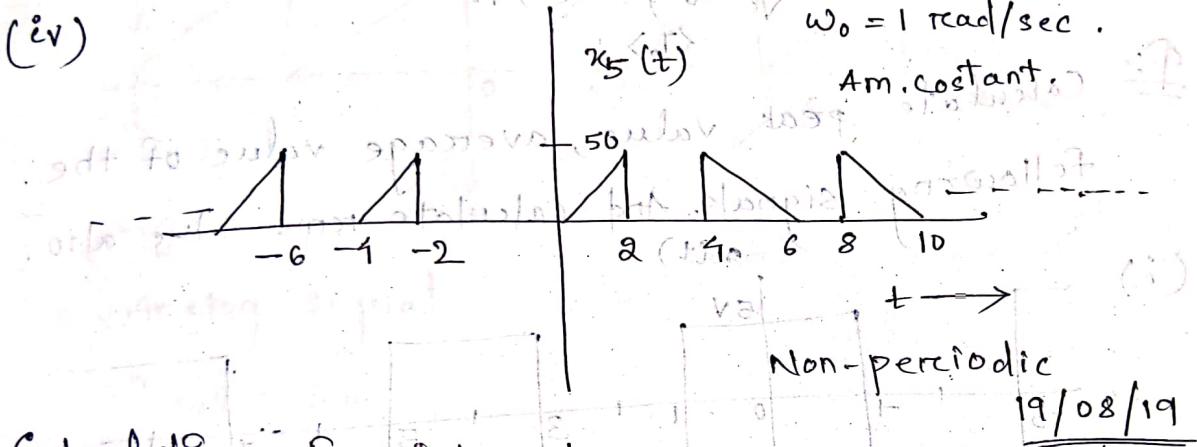
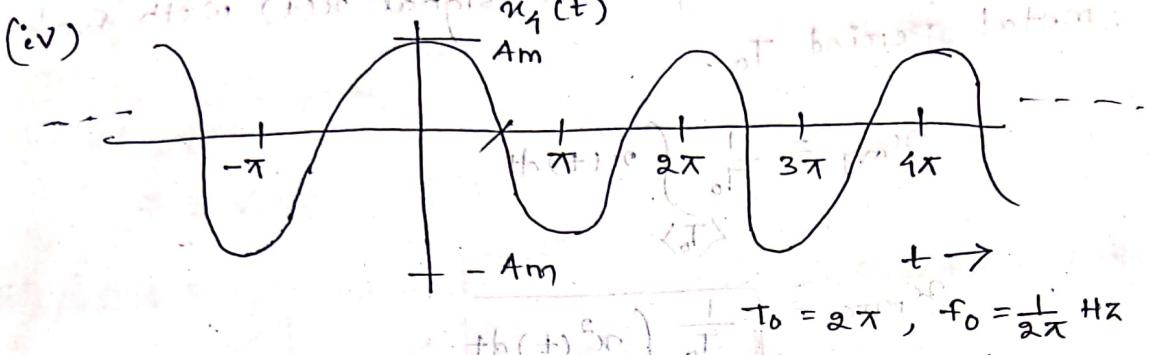
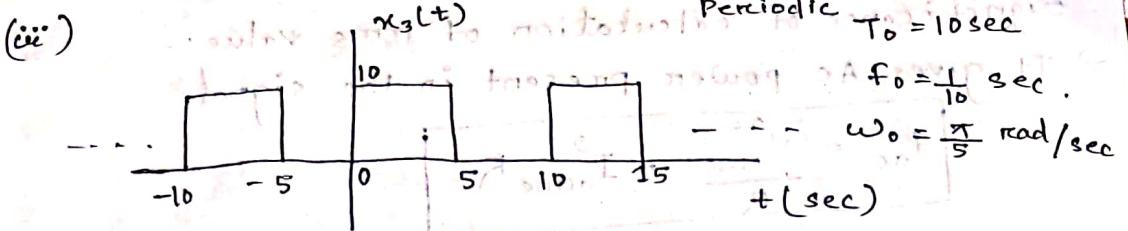


(ii)

Periodic.

$$T_0 = 10 \text{ sec} \quad f_0 = 1/10 \text{ sec}^{-1}$$

$$\omega_0 = \frac{\pi}{5} \text{ rad/sec}$$



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Calculation of peak value, average value and

R.M.S. value of any periodic signal :-

Significance of calculation of peak value:-

→ It gives maximum power present in the signal.

Significance of calculation of avg. value:-

→ It gives the total dc power present in the signal.

$$P_{dc} = \frac{V_{avg}^2}{R} = I_{avg}^2 R$$

Similarly,

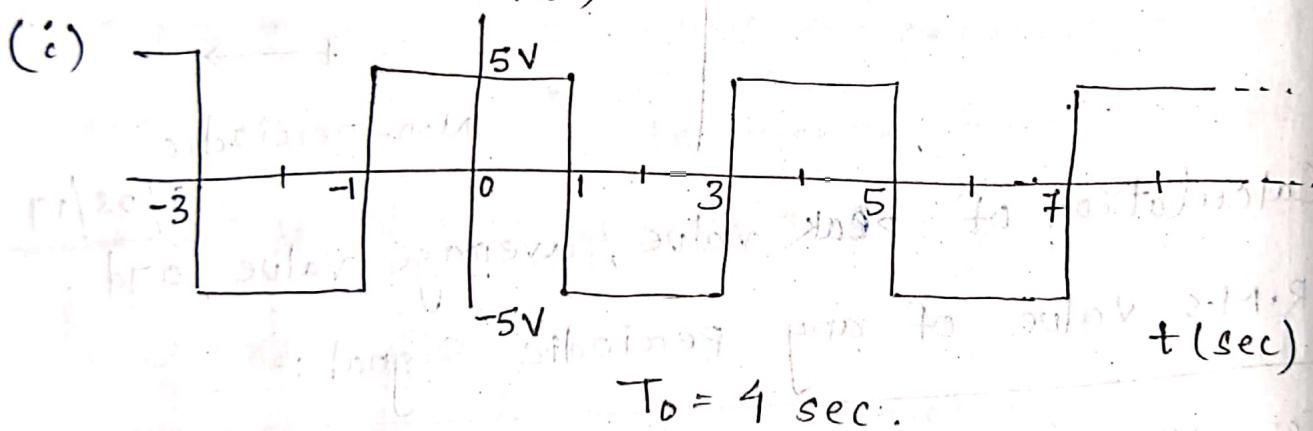
$$P_{peak} = \frac{V_p^2}{R} = I_p^2 R$$

Let's consider a periodic signal $x(t)$ with fundamental period T_0 .

$$x_{avg} = \frac{1}{T_0} \int_{T_0} x(t) dt$$

$$x_{rms} = \sqrt{\frac{1}{T_0} \int_{T_0} x^2(t) dt}$$

Q:- Calculate peak value, average value of the following signals. And calculate rms value also.



$x_{peak} = 5$ V (Periodic Signal) - digital signal

$$x_{avg} = \frac{1}{T_0} \int_{T_0} x(t) dt$$

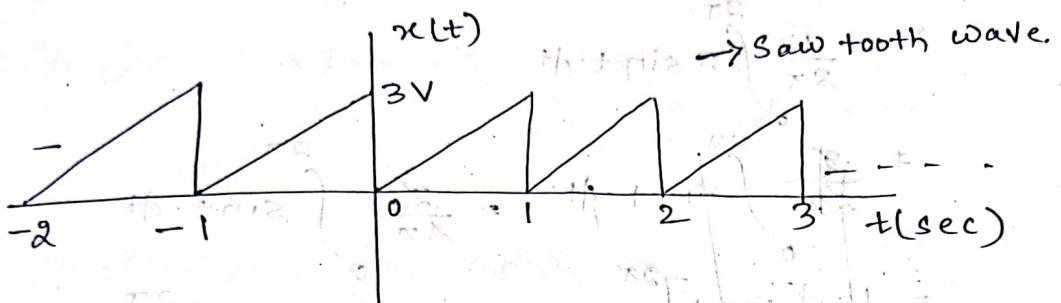
$$= \frac{1}{4} \int_0^4 x(t) dt$$

$$= \frac{1}{4} \left[\int_0^1 5t dt + \int_1^3 (-5)t dt + \int_3^4 5t dt \right]$$

$$= \frac{1}{4} \left[5 + (-10) + 5 \right] = \frac{1}{4} \times 0 = 0$$

$$\begin{aligned}
 x_{rms} &= \sqrt{\frac{1}{T} \int_0^T x^2(t) dt} \\
 &= \sqrt{\frac{1}{1} \left(\int_0^1 25 dt + \int_1^3 25 dt + \int_3^4 25 dt \right)} \\
 &= \sqrt{\frac{1}{1} (25 + 50 + 25)} \\
 &= \sqrt{\frac{1}{1} \times 100} \\
 &= 10 V
 \end{aligned}$$

(ii)



$$T_0 = 1 \text{ sec}$$

Analog signal.

$$\text{Hence, } y = mx + c$$

$$x_{peak} = 3 V$$

$$x_{avg} = \frac{1}{T_0} \int x(t) dt$$

$$= \int_0^1 3t \cdot dt$$

$$= 3 \frac{t^2}{2} \Big|_0^1$$

$$= \frac{3}{2} V$$

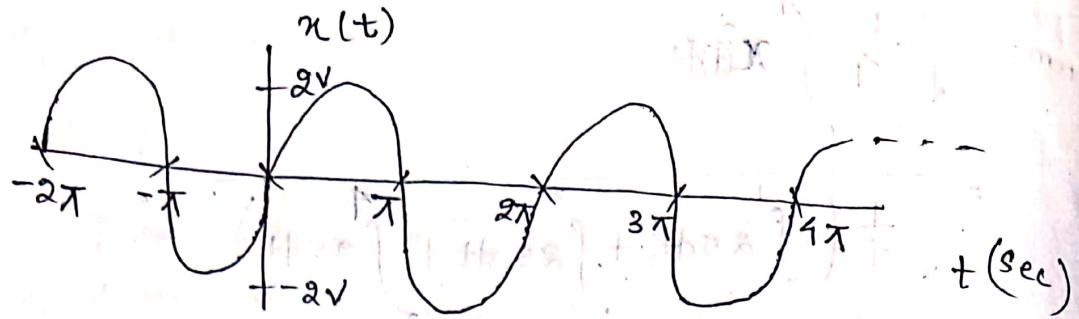
$$x_{rms} = \sqrt{\frac{1}{T_0} \int_0^{T_0} x^2(t) dt} = \sqrt{\frac{1}{1} \int_0^1 (3t)^2 dt}$$

$$= \sqrt{\int_0^1 \frac{9t^2 + 9}{3} dt} = \sqrt{3(1)^3}$$

$$= \sqrt{3} V$$

Ans

(iii)



$$T_0 = 2\pi \text{ sec.}$$

$$u_{\text{peak}} = 2V, f_0 = \frac{1}{2\pi}$$

$$\boxed{A_m \sin \omega_0 t} \\ \boxed{2 \sin t}$$

$$\therefore h_0 = 2\pi f_0$$

$$= 2\pi \times \frac{1}{2\pi} =$$

$$u_{\text{avg}} = \frac{1}{2\pi} \int_0^{2\pi} u(t) dt$$

$$= \frac{1}{2\pi} \int_0^{2\pi} 2 \sin t dt$$

$$= \frac{1}{2\pi} \int_0^{2\pi} \sin t \cdot dt$$

$$= \frac{1}{\pi} \left[\cos t \right]_0^{2\pi}$$

$$= -\frac{1}{\pi} \cos(2\pi + 0)$$

$$= -\frac{1}{\pi} \cos 2\pi$$

$$= \frac{2}{2\pi} \int_0^{2\pi} \sin t \cdot dt$$

$$= \frac{1}{\pi} \left[-\cos t \right]_0^{2\pi}$$

$$= -\frac{1}{\pi} [\cos 2\pi - \cos 0]$$

$$= -\frac{1}{\pi} [1 - 1] = 0V$$

Ans

OR

$$= \frac{1}{2\pi} \left[\int_0^{\pi} 2 \sin t \cdot dt + \int_{\pi}^{2\pi} 2 \sin t \cdot dt \right]$$

$$= \frac{1}{2\pi} \left[2 \left[\cos t \right]_0^{\pi} + 2 \left[-\cos t \right]_{\pi}^{2\pi} \right]$$

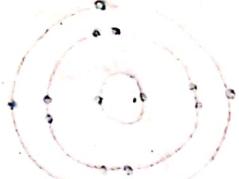
$$= \frac{1}{2\pi} \left[-\{\cos \pi - \cos 0\} + \{\cos 2\pi - \cos \pi\} \right]$$

$$= \frac{1}{\pi} \left[-(-1+1) + (1-1) \right]$$

$$= \frac{1}{\pi} \times 0$$

$$= 0V$$

$$\begin{aligned}
 x_{\text{rms}} &= \sqrt{\frac{1}{T_0} \int_{T_0}^{\infty} x^2(t) dt} \\
 &= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} 1 \sin^2 t dt} \\
 &= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \frac{1 - \cos 2t}{2} dt} \\
 &= \sqrt{\frac{1}{2\pi} \left(\int_0^{2\pi} \frac{1}{2} dt - \int_0^{2\pi} \frac{\cos 2t}{2} dt \right)} \\
 &= \sqrt{\frac{1}{2\pi} \left(\frac{1}{2} \times (2\pi - 0) - \frac{1}{2} \int_0^{2\pi} \sin 2t dt \right)} \\
 &= \sqrt{2} \text{ Volt.}
 \end{aligned}$$



Note-1

$$A_m \sin 2\pi f_0 t + \phi \text{ or } A_m \sin \omega t$$

Peak value = A_m

$$x_{\text{avg}} = 0$$

$$x_{\text{rms}} = \frac{A_m}{\sqrt{2}}$$

Note-2 $A_m \cos 2\pi f_0 t + \phi$ or $A_m \cos \omega t$

Peak value = A_m

$$x_{\text{avg}} = 0$$

$$x_{\text{rms}} = \frac{A_m}{\sqrt{2}}$$

$$x_{\text{avg}} = \frac{1}{T_0} \int_0^{T_0} x(t) dt$$

= Area under $x(t)$

T_0

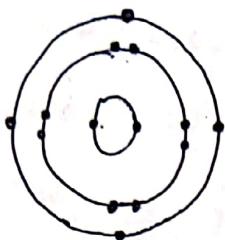
If area is 0, then $x_{\text{avg}} = 0$.

21/08/19

Semiconductor Material :-

→ Valency 4 elements like Si, Ge are used as semiconductor material.

$Si_{14} \rightarrow 1s^2, 2s^2, 2p^6, 3s^2, 3p^6 \rightarrow$ Electronic configuration of Si^{14} atom.



(Atomic str^r of Si atom)

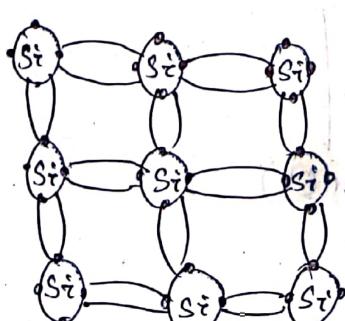
- Conduction is possible when the e^- is free from the nucleus i.e; free e^- can produce conduction.
- Outermost shell e^- can be free from nucleus. i.e; Outermost e^- , when they will free from the nucleus can provide conduction.
- The inner shell e^- , never be free from the nucleus and this inner shell e^- always bound e^- , they never produce conduction.

$Ge_{32} \rightarrow 1s^2, 2s^2, 2p^6, 3s^2, 3p^6, 3d^{10}, [1s^2, 4p^2]$



State Covalent Bond :-

It is formed by sharing of e^- between atoms.

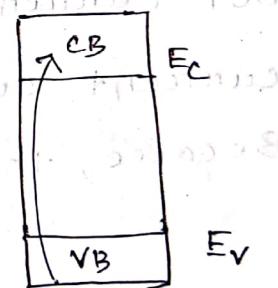


Silicon Crystal.

- In Si crystal only a large no. of Si atoms are present, each atom tries to get stability, by sharing the e⁻ with the neighbouring atoms. Such that each atom gets 8 e⁻ in the outermost shell by sharing the e⁻. As a result, formation of covalent bond.
- The e⁻ which are present in the covalent bond aren't free e⁻ and they aren't produce the conduction, bcoz the conduction is bcoz of the free e⁻.
- To increase the conductivity of the Si crystal we should increase the temperature. By increasing the sufficient temp., some of covalent bonds are break as a result, there will be generation of equal no. of free e⁻ and ~~holes~~ holes.

→ When the covalent bond will break, e⁻ will move from valency band to conduction band & the e⁻ becomes free.

Concept of hole:-



- The absence of e⁻ in covalent bond, is known as hole.
- Hole is +ve & charge of it 1.6×10^{-19} C.
- (E) Note:
- The Si crystal consists upon of only the Si atoms. So, it is known as pure semi-conductor or intrinsic semiconductor.
- In it, No. of hole = No. of free e⁻ i.e. in

pure semiconductor, $n = p$ plan (topper) is
electron conc. = hole conc.

Here, $\sigma_n = nq\mu_n$ and, $\sigma_p = nq\mu_p$ (principle of
current conduction)

Conductivity due to e^- is defined as $nq\mu_n$,
and conductivity due to hole is known
as $nq\mu_p$.

P = Conc. of hole; μ_n = Mobility of e^-

n = Conc. of e^- ; μ_p = Mobility of hole

Always $\mu_n > \mu_p$

Note :- In intrinsic semiconductor, $\sigma_n > \sigma_p$ (i.e. $\mu_n > \mu_p$)

In intrinsic semiconductor, $\sigma_n > \sigma_p$ (i.e. $\mu_n > \mu_p$)

$I_n = \sigma_n E A$ and $I_p = \sigma_p E A$

\rightarrow In intrinsic semiconductor, $I_n > I_p$

Electron conc. = hole conc. \Rightarrow mobility of

But current due to free e^- is greater than
current due to hole.

Because, the mobility of free e^- $>$ mobility of

$$J = \sigma E$$

$$J_n = \sigma_n E$$

$$\frac{I_n}{A} = nq\mu_n E$$

$$\Rightarrow I_n = nq\mu_n EA$$

\therefore Hence Total current (I)

$$I = I_n + I_p$$

$$\text{Again, } J_p = \sigma_p E = nq\mu_p E$$

$$\Rightarrow I_p = nq\mu_p EA$$

In intrinsic S.C., $n = p$, $\mu_n > \mu_p$ and $I_n > I_p$.

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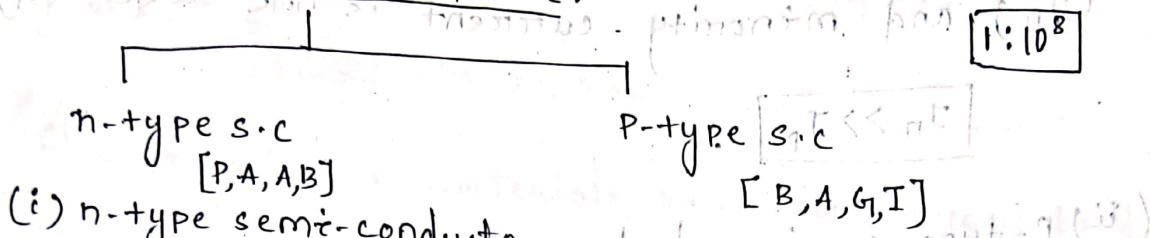
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→ To increase the conductivity, by increasing the temp. of intrinsic semiconductors isn't a good soln. So, increase the conductivity we should go for doping concept.

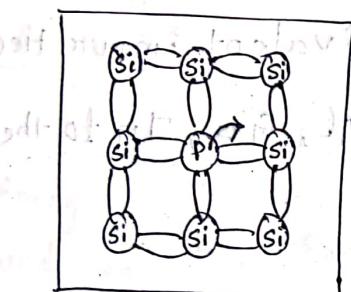
→ Doping means addition of impurities to pure/intrinsic semiconductors.

→ By addition of impurities to pure/intrinsic s.c. becomes extrinsic s.c.

Extrinsic Semiconductors:-



(i) n-type semiconductors:



→ It is formed by addition of impurities (donor impurities) like P, As, At, Sb, Bi.

→ Addition of pentavalent impurities into pure s.c., the pentavalent impurity becomes octate by sharing 1e⁻ of neighbouring Si atom. As a result one free e⁻ will be left out from the pentavalent impurities outermost shell. This e⁻ will be filled which will take part in conduction.

→ Total conductivity in n-type s.c. is because of conductivity due to free e⁻ & the holes.

$$\text{So, } I = I_n + I_p$$

$$J_n = \sigma_n E$$

$$J_p = \sigma_p E$$

$$n J_n = n \sigma_n E A \text{ and } p J_p = p \sigma_p E A \text{ with } p < n$$

$\therefore J_n \gg J_p$

Note:- In p-type semiconductor due to addition of impurities

\rightarrow In n-type s.c., the majority of carriers is e^- & minority carrier is hole.

\rightarrow In n-type s.c., the majority current is e^- current (J_n) and minority current is hole current (J_p)

$$J_n \gg J_p$$

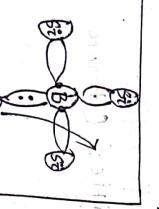
(ii) P-type semi-conductor:

$\rightarrow J_n$ is formed by addition of trivalent impurity (acceptor impurities) like B, Al, Ga, In to the

intrinsic s.c./ pure s.c.

$$\Rightarrow J_n \gg J_p$$

[P.A.Q]



$$J_n = J_p + J_h$$

[P.A.Q]

$$= J_p A + J_n A$$

As

$$J_p = \sigma_p E A$$

$$J_n = n \sigma_n E A$$

$$= \sigma_p n \mu_p E A + n \sigma_n \mu_n E A$$

Again $\sigma_p > \sigma_n$ and $n < p$

$$\Rightarrow J_p > J_n$$

Note:- $J_n \gg J_p$

\rightarrow Hole is majority carrier and e⁻ is minority carrier.

\rightarrow Hole current is majority and e⁻ current is

minority. Hence

$$I = I_p + I_b$$

Hence doping effect is more than mobility effect.

Paul's exclusion principle:

26/08/2019

> Each e^- should have unique energy level. (No two e^- will have same energy level).

Energy Band :-

> It is the collection of closely spaced energy levels.



Classification of materials based on energy bands

- (1) Insulator
- (2) Conductor
- (3) Semi-conductor



$E_g = E_c - E_v$ = Energy band gap.

E_c = Lowest energy level in conduction band.

E_v = Highest energy levels in valency band.

$E_c - E_v = \text{Energy band gap.}$ (E_g)

Insulator :-

> In case of insulator, the energy band gap is very large, so by thermal excitation, no e^- will move from valency band to conduction band. Hence there is no free e^- available in conduction band. So, there will be no conduction in case of insulator.

conductivity (σ) = 0

$\Rightarrow \sigma = 0$
 $\Rightarrow \rho = \frac{1}{\sigma} = \infty$ (Resistivity)

$$I = D$$

Conductor:

\Rightarrow In case of conductor, valency band & conduction band overlap each other. So, a large no. of free e⁻ available in CB. Hence conductivity

$\sigma \neq 0$ (large) \rightarrow $I \neq 0$

$\Rightarrow \rho = \frac{1}{\sigma} \neq \frac{1}{0}$ (small)

$$I \neq 0$$

Semi-conductor:

\Rightarrow In case of this, there is moderate energy gap. So, by thermal excitation some of covalent bond will break & some e⁻ will move from VB to CB. As a result, a moderate no. of free e⁻s and holes will be available.

Hence $\sigma \neq 0$ (moderate)

$\Rightarrow \rho \neq \frac{1}{\sigma} \Rightarrow \rho \neq \frac{1}{0}$ (moderate)

$$I = I_n + I_p$$

Note:-

\Rightarrow All intrinsic or extrinsic semiconductors behaved like insulators at 0°K due to absence of

$$\rho = c$$

$$\rho =$$

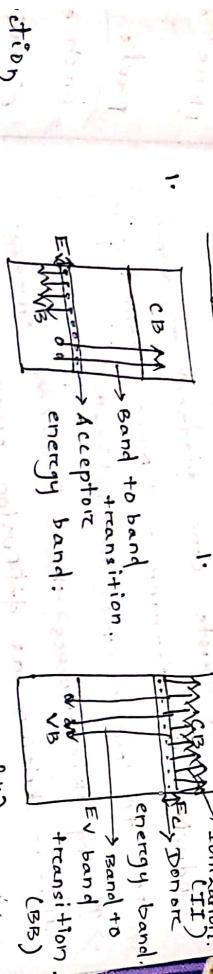
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Her

P+

P-type S.C

N-type S.C



(at 0°K)
 $p=0, \sigma=0$
 $f=v, I=D$ (at 0°K), $I \neq 0$, $I \neq D$
 $(at 300K)$

(at 0°K)
 $p=0, \sigma=0$
 $f=v, I=D$ (at 0°K), $I \neq 0$, $I \neq D$
 $(at 300K)$

Hence;
 $I = I_{BB} + I_{IT}$

$\Rightarrow I = I_{P(BB)} + I_{n(CB)}$ (In N-type S.C)
 $I_{IT} = I_P + I_n$

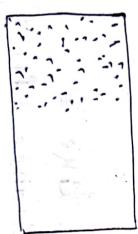
But ; $I = I_{BB} + I_{IT}$

$= I_n + I_P$. (In P-type S.C)
 $= I_n + I_P + I_{P(BB)} + I_{P(IT)}$

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more
 ble.
 Diffusion and Drift phenomenon :-

N-type S.C



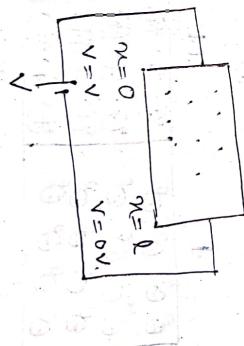
$n=0$
 $n=n_1$

$n_1 > n_2$

$\frac{dn}{dx} \neq 0$, $\frac{dn}{dx} = \frac{n_2 - n_1}{1 - 0}$

S.C

P-type S.C



$n=0$
 $n=n_2$

$v=v$
 $v=0v$

$\frac{dn}{dx} \neq 0$, $\frac{dn}{dx} = \frac{n_2 - n_1}{1 - 0}$

→ Diffusion is a natural occurring phenomena,

When there exists conc. gradient in semi-conductor, the carriers will move from higher conc. to lower conc. automatically.

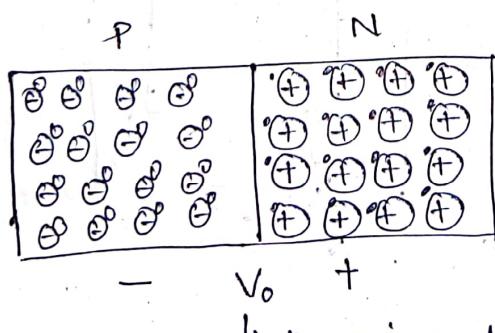
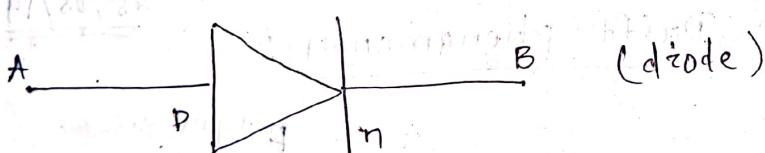
→ During this process, there is some current, this is known as diffusion current.

→ When there exist potential gradient in semi-conductor carriers will move inside the semi-conductor, this process is known as drift process.

→ When there exist potential gradient, carriers will move inside the S.C. bcoz of the movement of carriers inside the S.C., there will be some current inside the S.C. is called drift current.

P-n junction diode:

By Schematic diagram:-



(It acts like a capacitance effect)

↳ Barrier potential/
Contact point.



depletion region.

- When P-type and N-type S.C.
bcz of diffusion process e⁻ will move from N-type
S.C. and hole will move from P-type to
N-type S.C. (hole generate in this region) so
as a result hole with e⁻ pair will disappear
at the junction. or at about 10 nm is generated
After some time, diffusion will stop. Cuz to
-ve plate in P-type S.C. will repel the e⁻
will N-type S.C. and generated +ve plate in
N-type S.C. will repel the e⁻ will P-type S.C.

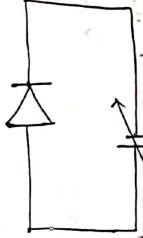
Note..

- ① Junction allows the flow of minority characters, but it opposes flow of majority characters.
- ② Inside the P-N junction, a -ve plate is generated in P-side & +ve plate is in N-side.
- ③ At +ve plate there are some +ve potential and -ve " " " " " +ve potential.
Inside the junction there will be some potential diff. bet P-type S.C & N-type S.C.
This is called contact potential or barrier potential.

$$V_0 = 0.7 V (\text{Si})$$

$$V_0 = 0.3 V (\text{Ge})$$

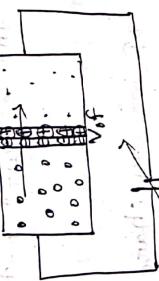
Forward Bias of PN Junction diode:-



→ When PN Junction diode is connected to an external DC voltage, such a manner that, P side of the diode is connected to the plate of the supply and N side of diode is connected to -ve plate of the supply.

→ The diode is said to be forward biased.

$$I = I_n + I_p \quad \text{and} \quad I = I_n + I_p + I_d$$



→ When $V_f < 0.7V$, less amount of current will flow, because of minority carrier will diffuse across the junction.

→ When $V_f > 0.7V$, more majority carrier will diffuse across the junction.

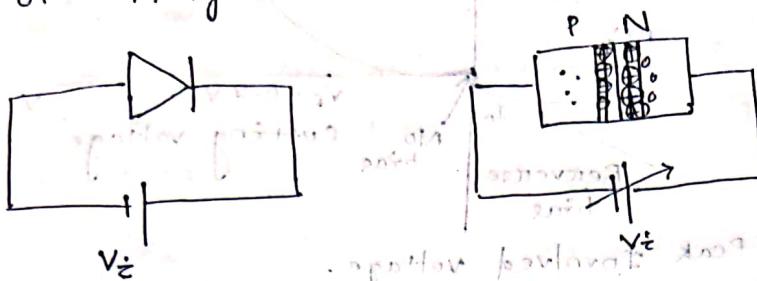
As a result, a diffusion current will flow from P side to N side.

→ But, increasing V_f beyond $0.7V$, diffusion current will decrease, because more no. of carrier diffuse across the junction.

→ The nature of the increasing current, by increasing V_f is exponential. (Experimentally proved.)

Reverse Bias of PN Junction diode:

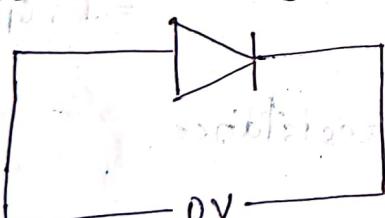
→ A PN Junction diode is said to be reverse bias, when P-side of diode is connected to -ve plate of supply & N-side is connected to +ve.



→ By increasing V_Z , depletion region width will increase, there will be no flow of majority carrier across the junction, only the minority carrier will drift across the junction.

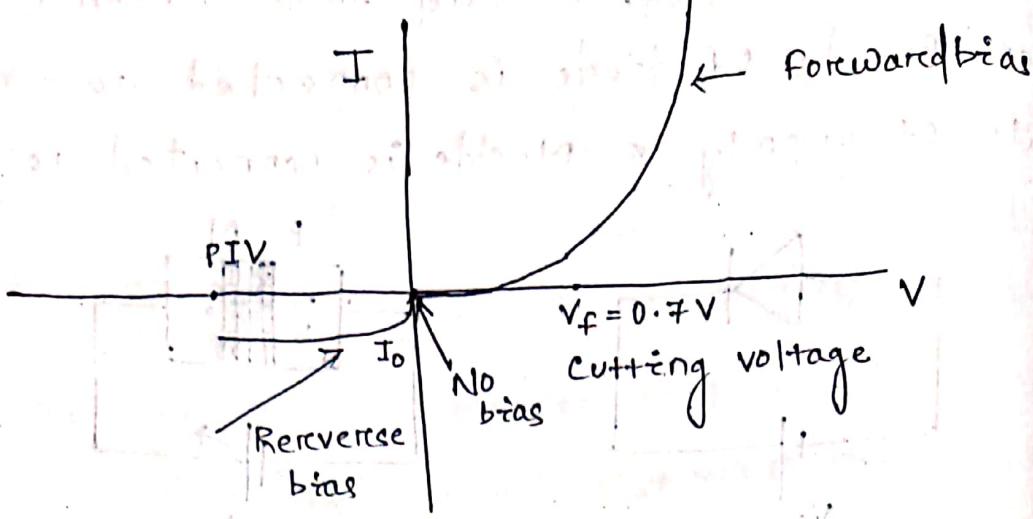
→ The net current across the junction is because of only the drifting of minority carrier which is flow from N side → P side.

→ The diode is said to be under no bias condition, whence when no external bias voltage is applied across the PN junction.



→ During no bias condition, there will be no flow of majority carrier across the junction.

→ There will be existence of depletion region across the junction.



PIV - Peak Inverse voltage.

~~Diode current voltage :-~~

$$I = I_0 \left(e^{\frac{V_D}{nV_T}} - 1 \right)$$

Where, V_D = Voltage across the diode \rightarrow FB

I_0 = Reverse saturation current

I = Current across diode.

V_T = temperature equivalent voltage $= \frac{T}{11600}$

At 300 K , 27°C .

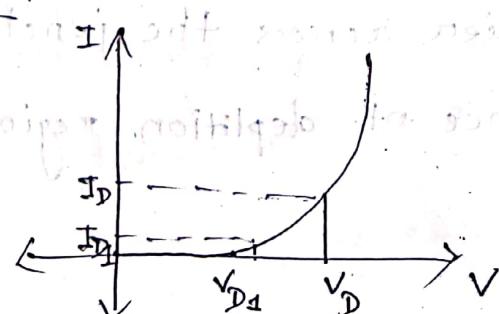
$$V_T = 25\text{ mV} \text{ or } 26\text{ mV.} \quad n = 2, \text{ Si} \\ n = 1, \text{ Ge.}$$

Diode resistance level :-

(a) DC resistance or static resistance.

(b) AC or dynamic resistance.

DC :-



→ It is defined as the ratio of voltage across the diode to the current flowing through the diode.

A_c = Change in voltage / Change in current

→ It is defined as the ratio of change in voltage to the change in current i.e., $R_{ac} = \frac{dV_D}{dI_D}$ slope



$$R_{ac} = \frac{1}{\frac{dI_D}{dV_D}} = \frac{1}{I_0 (e^{V_D/nV_T}) \times \frac{1}{nV_T}}$$

$$= \frac{nV_T}{I_0 (e^{V_D/nV_T})}$$



for forward bias, $I_D = I_0 (e^{V_D/nV_T})$

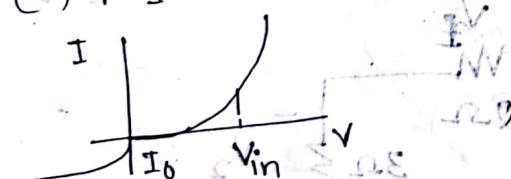
$$\approx I_0 (e^{V_D/nV_T})$$

For reverse bias, $I_D = I_0 (e^{V_D/nV_T})$

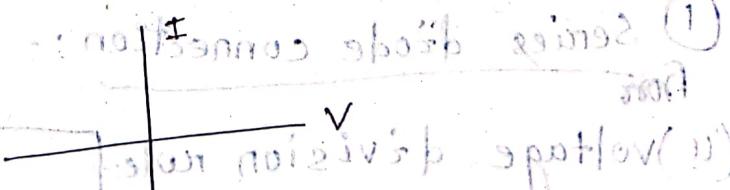
Ideal diode vs practical diode:

Practical

(1) V-I



$$V_{in} = 0.7 V \text{ or } 0.3 V$$



$$V_{in} = 0V$$

(2) R_B current ≠ 0

$$- \infty$$

$$R_B \times V = 0V$$

(3) R_B Resistance ≠ ∞

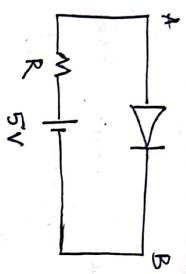
Equivalent model of PN Junction diode



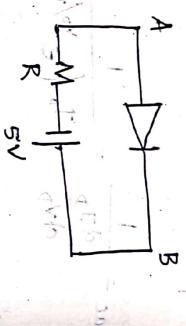
1. Linear piecewise model
2. Simplified model
3. Ideal model

→ check the diode is forward biased or reverse biased and replace the diode by its equivalent model in any electric circuit.

F.B



R.B



① Linear piecewise model :-



② Simplified model :-

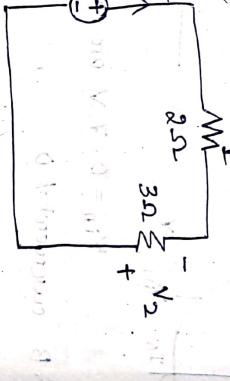


③ Ideal model :-



Application :-

① Series diode connection :-



From
(a) voltage division rule:-

$$V_1 = \frac{V \times R_1}{R_1 + R_2}$$

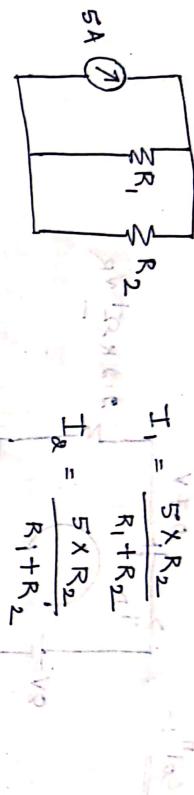
$$V_2 = \frac{V \times R_2}{R_1 + R_2}$$

$$V_1 = ? , V_2 = ?$$

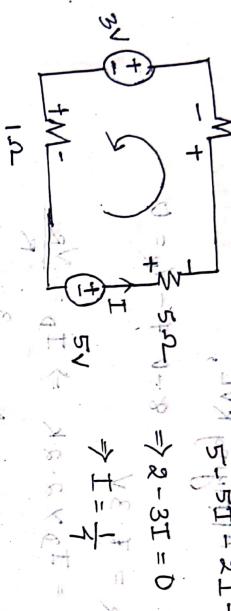
$$V_1 = \frac{5 \times 2}{2+3} = 2V$$

$$V_2 = \frac{-5 \times 3}{5} = -3V$$

(b) Current division:-



★ KVL :-



$$3V + 5V - 2I - V = 0$$

$$\Rightarrow 2I = 8V$$

$$\Rightarrow I = 4A$$

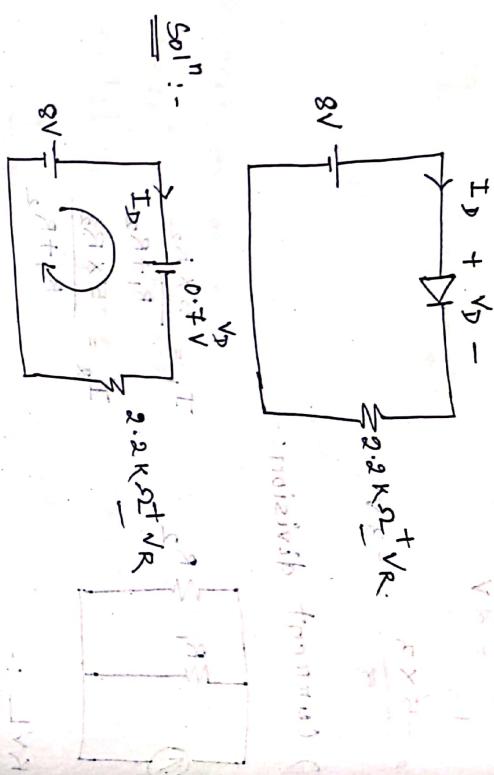
Statement:- In a linear bilateral network, the algebraic sum of all voltage across a loop is zero(0).

★ KCL :-

In a linear bilateral network, the algebraic sum of all current at any node is eq 0.



Q:- For the series diode connection shown in fig, determine V_D , V_{RD} , I_D .



$$V_D = 0.7V$$

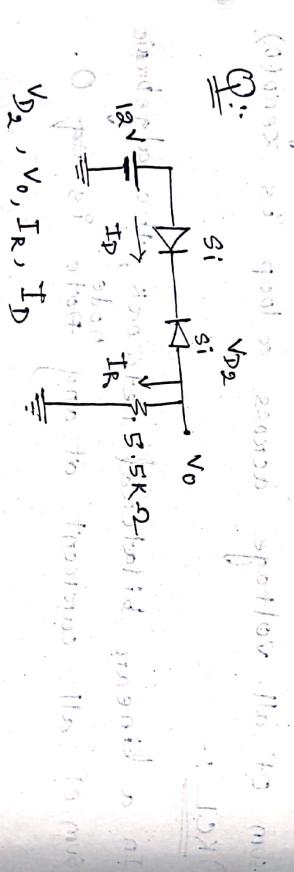
Soln:- Applying KVL,

$$V_D = E - I_R \cdot R \Rightarrow 8 - 0.7V_D - V_R = 0$$

$$V_R = I_D \cdot 2.2k \Rightarrow 3V = I_D \cdot 2.2k$$

$$I_D = \frac{V_R}{2.2k} = \frac{3}{2.2k}$$

$$\Rightarrow I_D = \frac{4.3}{10.2 \cdot 2.2k} = \frac{4.3}{22} \times 10^3 = 0.2 \text{ A}$$



$$V_D = 0.7V$$

$$I_R = 0 \text{ A} = I_D$$

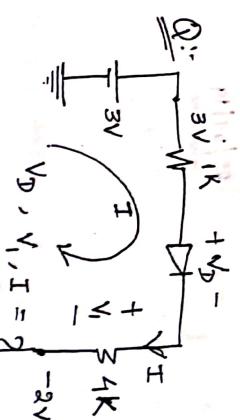
$$V_0 = 0 \times 5.6k = 0V$$

At node common between D1 and D2 not

Applying KVL

$$12 - 0.7V_D - V_{D2} = 0 = 0$$

$$V_{D2} = 11.3V$$



Hence

$$3 - IXK - 4K\bar{I} + 2 = 0$$

(Divide by common factor K)

$$5\bar{I} = \frac{5}{5}$$

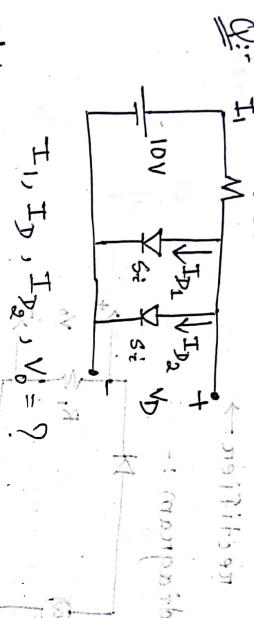
$$(\bar{I} = \frac{1}{5} = 0.2 \text{ A or } 200 \text{ mA})$$

$$V_D = 0$$

Ans. No dependent source in branch C.

Ans. 10V voltage source in branch B.

$$0.33 \text{ k}\Omega$$



$$I_1, I_D, I_{D2}, V_D = ?$$

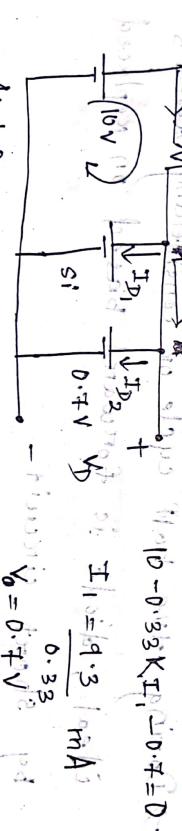
Note:-

→ Voltage across any two parallel branches is always equal.

→ Current through a series element will always

equal $-I_1$.

Applying KVL,



Applying KCL at A,

$$I_{D1} + I_{D2} + (-I_1) = 0$$

$$\Rightarrow 2I_{D2} = I_1 \Rightarrow I_{D1} = \frac{1}{2} I_1$$

Application of diode :-

- ① Diode as rectifier
- ② Diode as clipper
- ③ Diode as clumper
- ④ Diode as switch etc.

→ Diode as Rectifier :-

Rectifier → It is an electronic circuit, which converts AC. to DC. (Pulsating DC)

→ It is of 2 types.

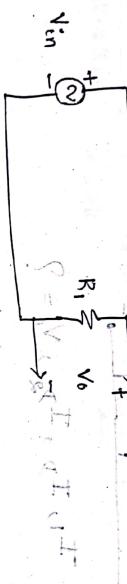
(i) Half wave rectifier

(ii) Full wave rectifier

Half wave rectifier →

Brilliant Hyper F.W.R

Full wave rectifier → center tapped F.W.R



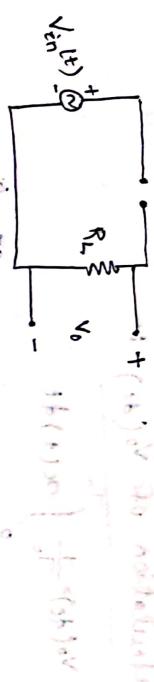
Working principle:-

During positive half cycle of input voltage, the diode is forward biased. So current flows through the diode and the load resistor. Hence output voltage is same as input voltage.



→ During negative half cycle or considering diode is ideal, diode is forward biased on replaced by short circuit.

$V_o = (V_m + E_v) + g(E_v - V_o)$



Apply KVL,

$$V_{in} - V_o = 0$$

$$\Rightarrow V_{in} = V_o$$

During +ve half cycle the diode will be forward biased & replace the diode by open circuit.



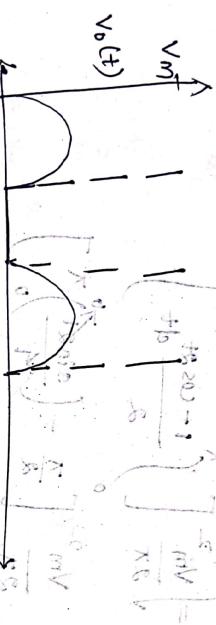
Apply KVL,

$$V_{in}(t) - V_o = 0$$

$$\Rightarrow V_o = 0$$

$$V_o = 0 \times R_L$$

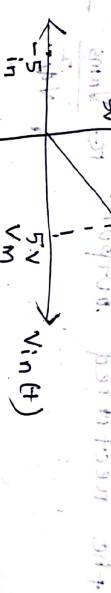
$$V_o = 0$$



To transfer characteristics: sketch time graph A

→ When ever we sketch time graph A

→ The graph depends on the input & output



Calculation of $V_o(\text{dc})$

$$V_o(\text{dc}) = \frac{1}{T_0} \int_0^{T_0} v_o(t) dt$$

$$\begin{aligned}
 &= \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin t \cdot dt + \int_{\pi}^{2\pi} V_m \sin t \cdot dt \right] \\
 &= \frac{1}{2\pi} \left[V_m \left[-\cos t \right] \Big|_0^{\pi} + V_m \left[-\cos t \right] \Big|_{\pi}^{2\pi} \right] \\
 &\quad \text{Average value of AC component is zero. Hence, it is removed.} \\
 &= \frac{1}{2\pi} \left[V_m \left(-\cos \pi + \cos 0 \right) \right] \\
 &= \frac{V_m}{\pi}
 \end{aligned}$$

$V_o(\text{rms})$ calculation:-

$$\begin{aligned}
 V_o(\text{rms}) &\geq \sqrt{\frac{1}{T_0} \int_0^{T_0} (v_o(t))^2 dt} \\
 &= \sqrt{\frac{1}{2\pi} \int_0^{\pi} (V_m \sin t)^2 dt} \\
 &= \sqrt{\frac{V_m^2}{2\pi} \left[\int_0^{\pi} \frac{1-\cos 2t}{2} dt \right]} \\
 &= \frac{V_m}{2\pi} \left[\frac{\pi}{2} - \left(\frac{\sin 2t}{4} \right) \Big|_0^{\pi} \right] \\
 &= \frac{V_m^2}{2\pi} \times \frac{\pi}{2} = \frac{V_m}{2}
 \end{aligned}$$

Ripple Factor: -

→ A ripple factor is defined as the ratio of AC component present in output or half of the output to the DC component present in the rectified output:

$$\text{Ripple Factor} = \sqrt{\frac{V_{\text{rms}}^2}{V_{\text{dc}}^2} - 1}$$

$$= \sqrt{\left(\frac{V_m}{2}\right)^2 - 1}$$

$$= \sqrt{\frac{V_m^2}{4} \times \frac{\pi^2}{V_m^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$= 1.021$$

Efficiency of Rectifier

\Rightarrow It is defined as the ratio of DC output power

to the AC output power

$$\eta = \frac{P_{dc}(o/p)}{P_{ac}(o/p)}$$

$$= \frac{V_{dc}^2}{V_{rms}^2} \times \frac{R_L}{R_L + R_s}$$

$$= \frac{V_{dc}^2}{V_{rms}^2} \times \frac{R_L}{R_L + R_s}$$

$$= \frac{V_{dc}^2}{V_{rms}^2} \times \frac{R_L}{R_L + R_s}$$

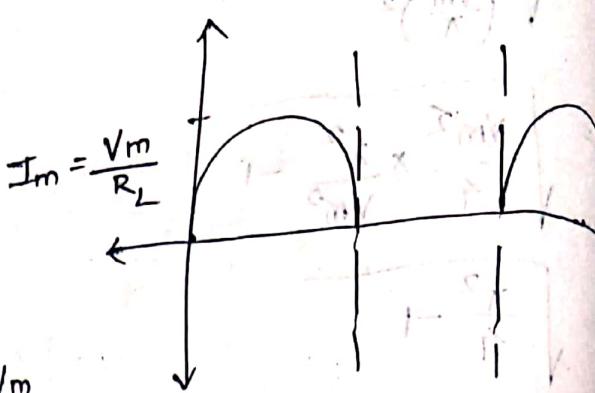
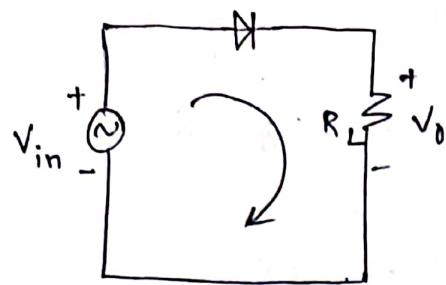
$$= \frac{\left(\frac{V_m}{2}\right)^2}{\left(\frac{V_m}{2}\right)^2}$$

$$= 10.6\%$$

Current through load

Efficiency of full wave rectifier

09/09/19

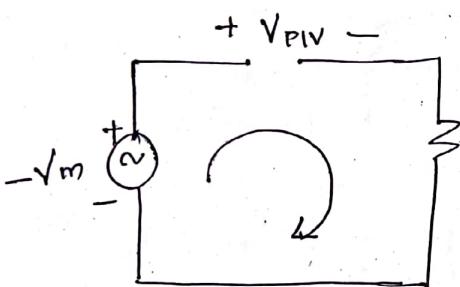


$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{V_m}{R_L} = \frac{V_m}{2R_L}$$

$$V_{dc} = V_{avg} = \frac{V_m}{\pi}$$

$$I_{dc} = I_{avg} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L} = \frac{V_m}{\pi R_L}$$

Peak reverse bias Peak Inverse Voltage:- (Calculated of PIV)
→ It is defined as the apply peak reverse bias voltage applied across the diode such that diode will safely work. (or diode will not work)



$$(-V_m) - V_{PIV} = 0$$

$$\Rightarrow V_{PIV} = -V_m$$

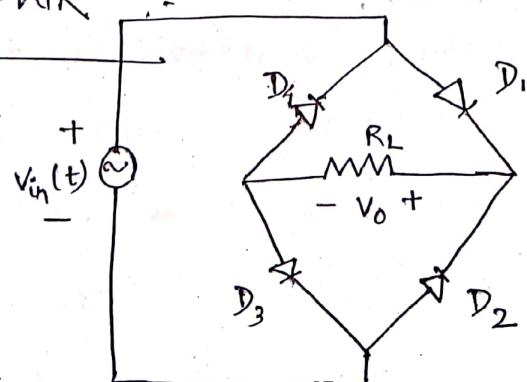
$$V_{PIV} = | -V_m | = V_m$$

$$V_{PIV} \leq V_m$$

①

Bridge type FWR

Circuit diagram:-



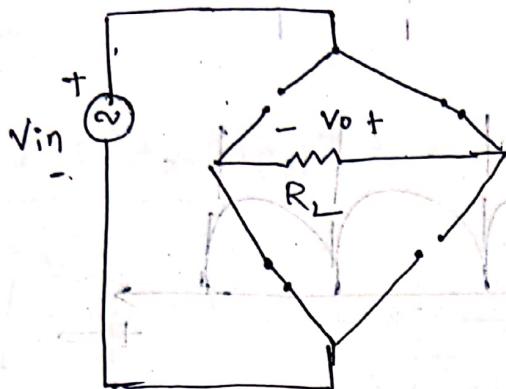
Operation :-

→ During +ve half cycle $D_1 \& D_3$ - forward biased
 $D_2 \& D_4$ - Reverse biased.

$D_1 \& D_3$ will be replaced by short circuit.

$D_2 \& D_4$ " " open circuit.

→ And circuit become now :-



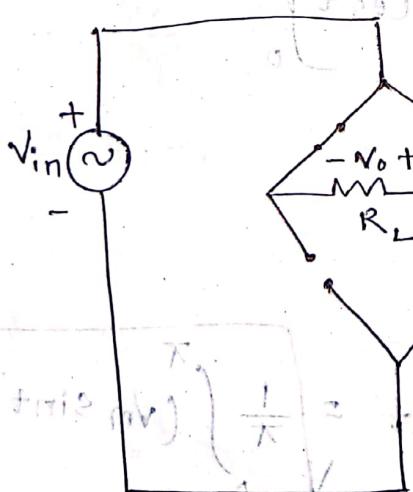
Applying KVL,

$$V_{in} - V_0 = 0$$

$$\Rightarrow V_{in} = V_0$$

→ During -ve half cycle, $D_1 \& D_3$ will be reverse biased & replaced by open circuit.

And $D_2 \& D_4$ - forward biased - replace by short circuit.



$$V_{in} + V_0 = 0$$

$$V_{in} = V_0$$

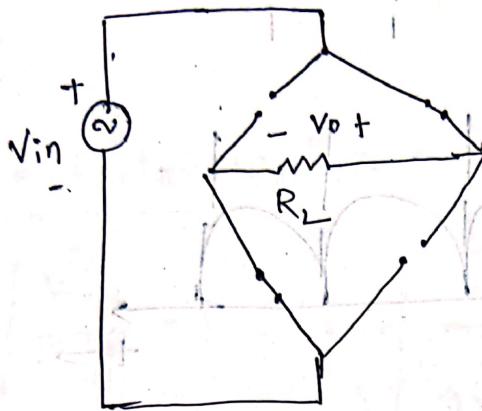
Operation :-

→ During +ve half cycle $D_1 \& D_3$ - forward biased
 $D_2 \& D_4$ - Reverse biased.

$D_1 \& D_3$ will be replaced by short circuit.

$D_2 \& D_4$ " " " open circuit.

→ And circuit become now :-



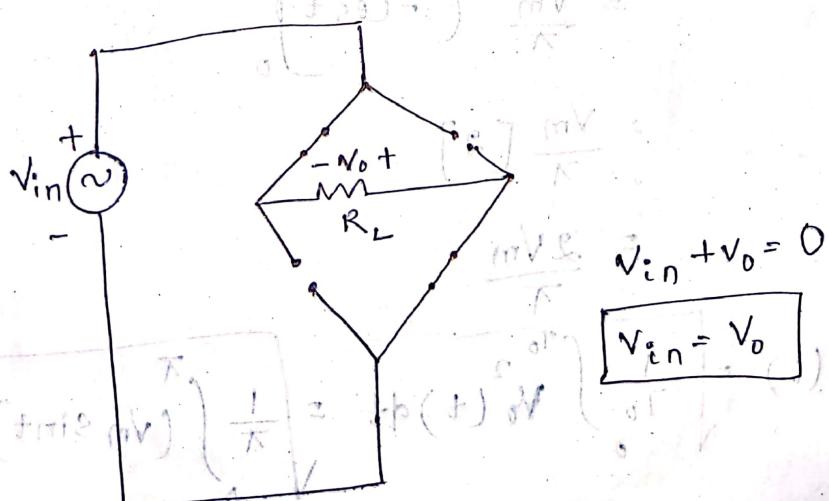
Applying KVL,

$$V_{in} - V_0 = 0$$

$$\Rightarrow V_{in} = V_0$$

→ During -ve half cycle, $D_1 \& D_3$ will be reverse biased & replaced by open circuit.

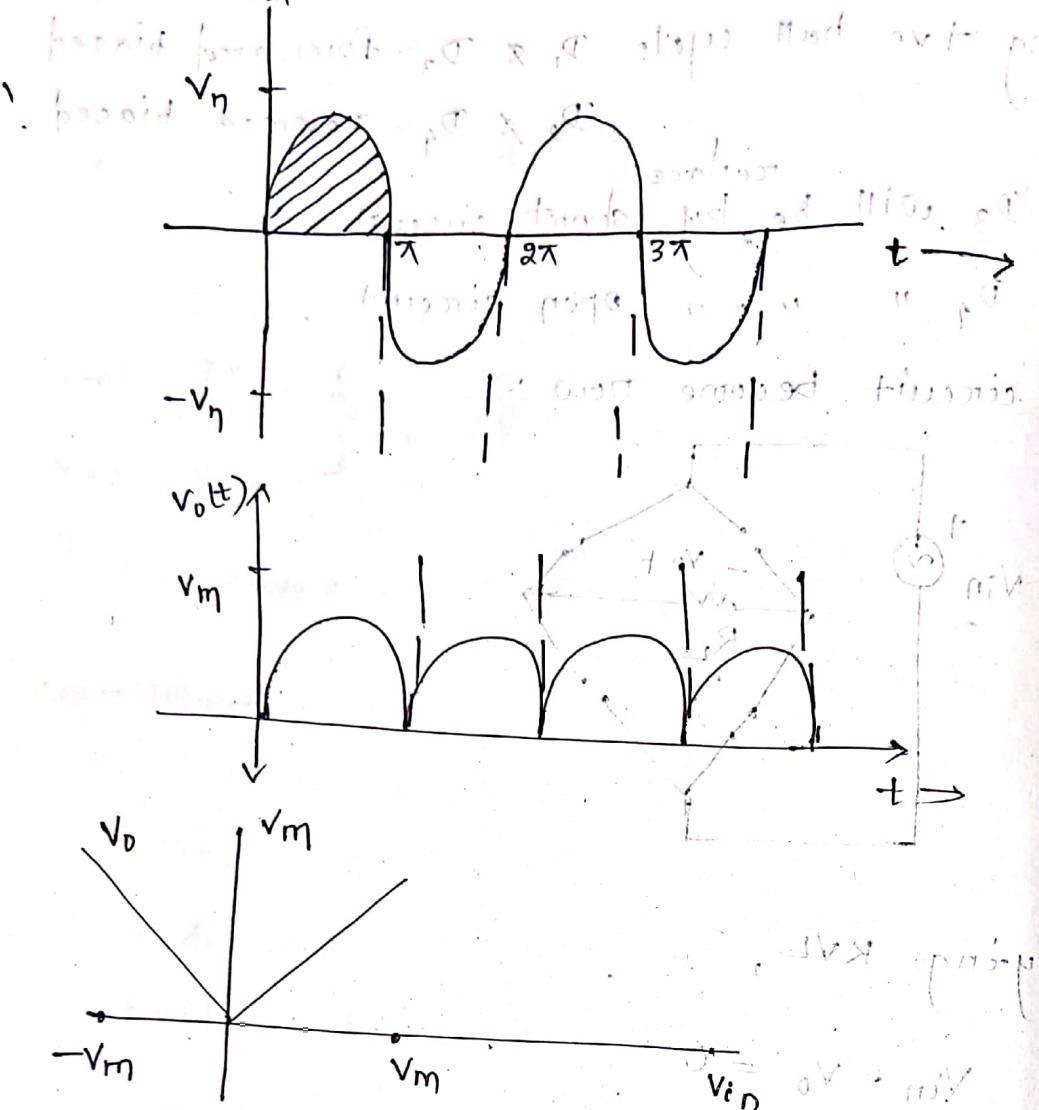
And $D_2 \& D_4$ - forward biased - replace by short circuit.



$$V_{in} + V_0 = 0$$

$$V_{in} = V_0$$

$$V_{in}(t) = V_m \sin t$$



$$V_{dc(0)} = V_{avg(0)} = \frac{1}{T_0} \int_{0}^{T_0} V_o(t) dt$$

$$\begin{aligned} &= \frac{1}{T_0} \int_{0}^{T_0} V_m \sin t dt \\ &= \frac{V_m}{\pi} (-\cos t) \Big|_0^{\pi} \\ &= \frac{V_m}{\pi} [2] \end{aligned}$$

$$\begin{aligned} V_{rms(0)} &= \sqrt{\frac{1}{T_0} \int_0^{T_0} V_o^2(t) dt} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (V_m \sin t)^2 dt} \end{aligned}$$

$$= \sqrt{\frac{V_m^2}{\pi}} \int_0^\pi \frac{1 - \cos 2t}{2} dt$$

$$= \sqrt{\frac{V_m^2}{\pi}} \left(\frac{t}{2} - \frac{\sin 2t}{4} \right)_0^\pi$$

$$= \sqrt{\frac{V_m^2}{\pi}} \left(\frac{\pi}{2} - 0 \right)$$

$$= \frac{V_m}{\sqrt{2}}$$

Ripple factor Cal :-

$$\text{Ripple factor} = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1} = 0.482$$

Efficiency :-

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

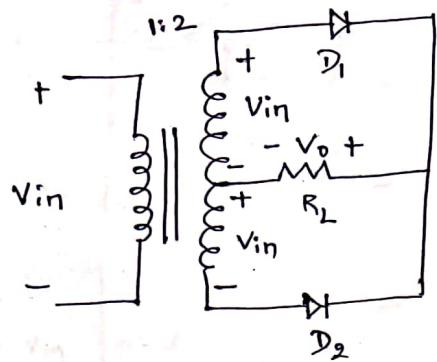
$$= \frac{V_{dc}^2}{R_L} \times 100\%$$

$$= \frac{V_{ac}^2}{R_L} \times 100\%$$

$$= 81\%$$

② Center tapped type FWR

Circuit diagram :-

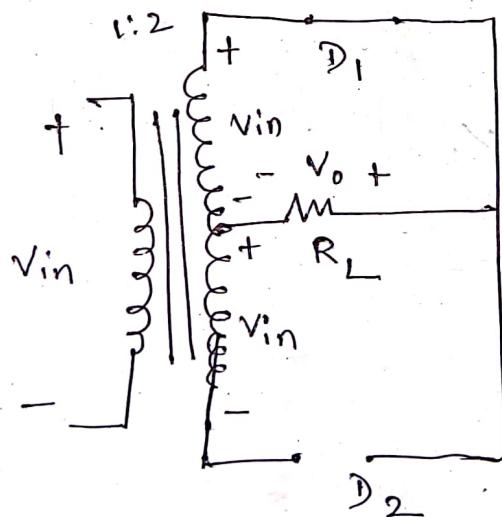


Operation :-

→ The turn ratio of the transistors is 1:2. So,
the voltage appears across the secondary
coil is $2V_m$.

→ During +ve half cycle of V_{in} ,
 D_1 will be forward biased, replace by short circuit.

D_2 " reverse " replace by open circuit.



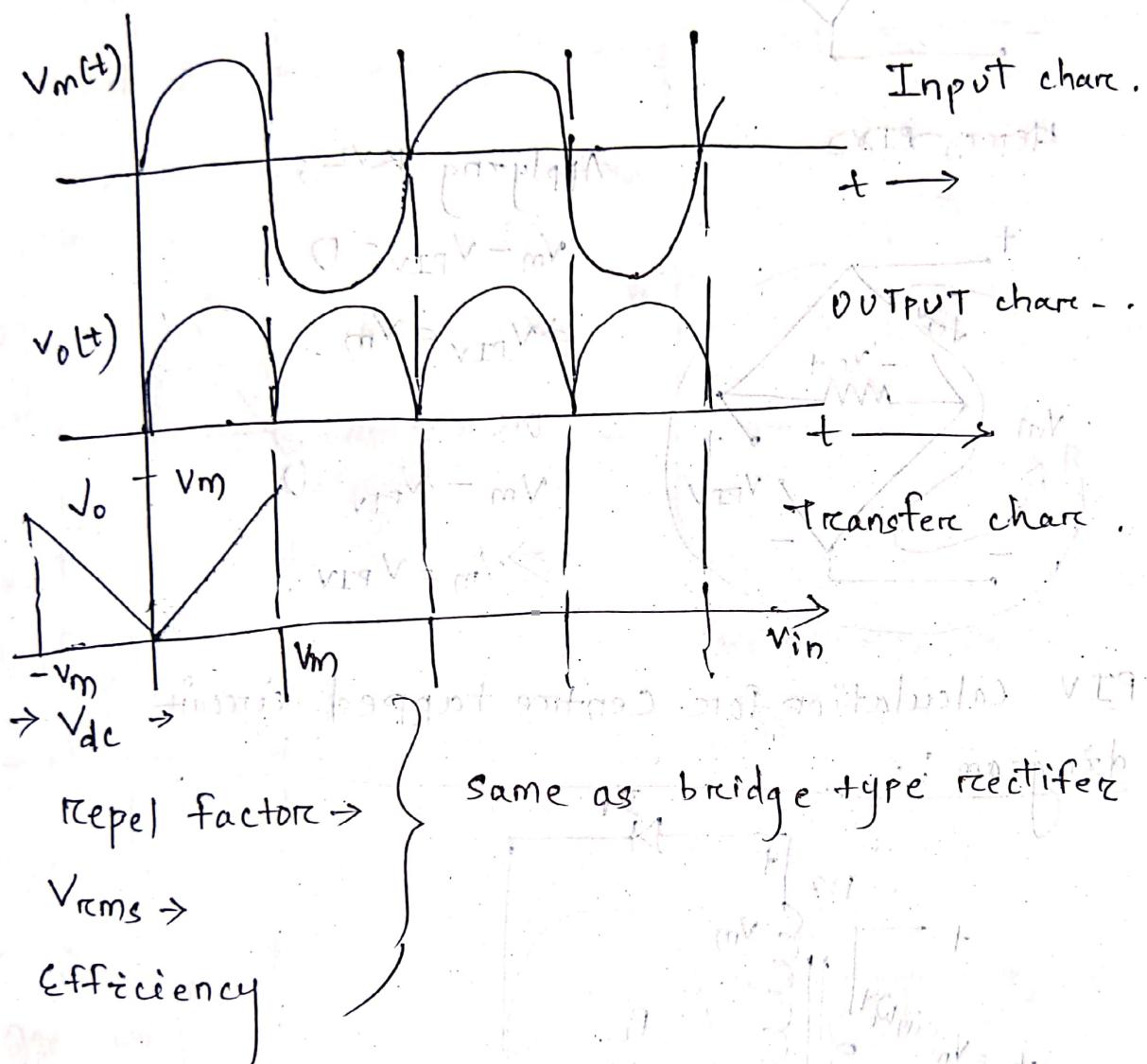
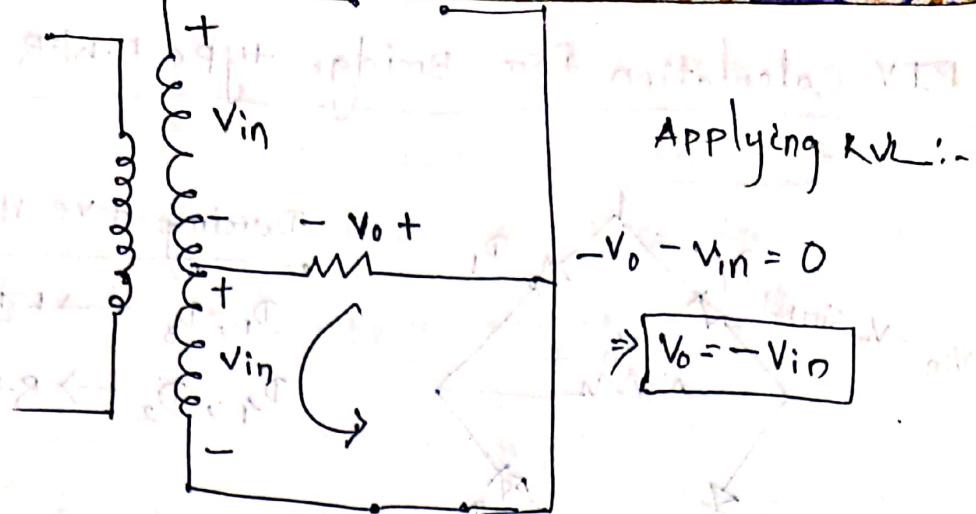
Applying KVL,

$$-V_0 + V_{in} = 0$$

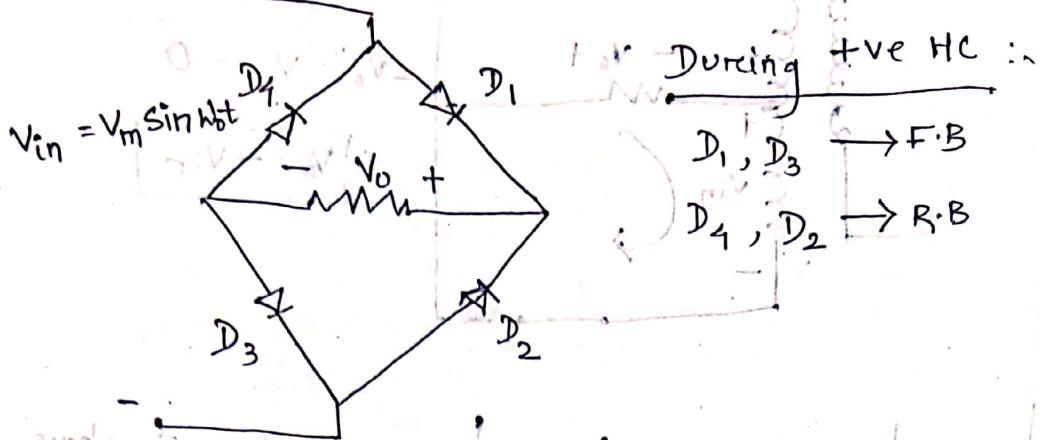
$$\Rightarrow V_0 = V_{in}$$

→ During -ve half cycle of V_{in} ,
 D_1 is reverse biased.

D_2 is forward biased.



PIV Calculation for Bridge type F.W.R :-



~~During -ve H.C.~~

Applying KVL;

$$V_m - V_{PIV} = 0$$

$$\Rightarrow V_{PIV} = V_m$$

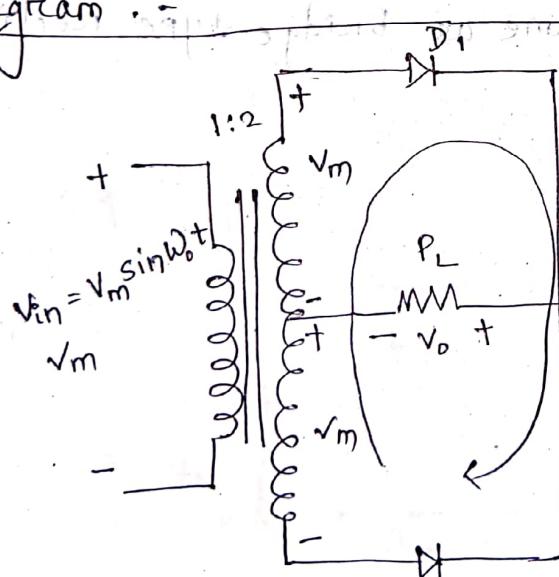
O.R.C

$$V_m - V_{PIV} = 0$$

$$\Rightarrow V_m = V_{PIV}$$

PIV calculation for Centre tapped circuit

diagram :-



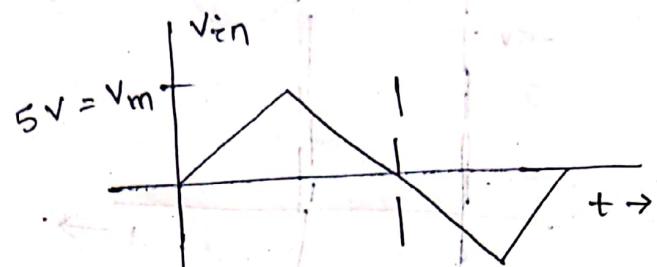
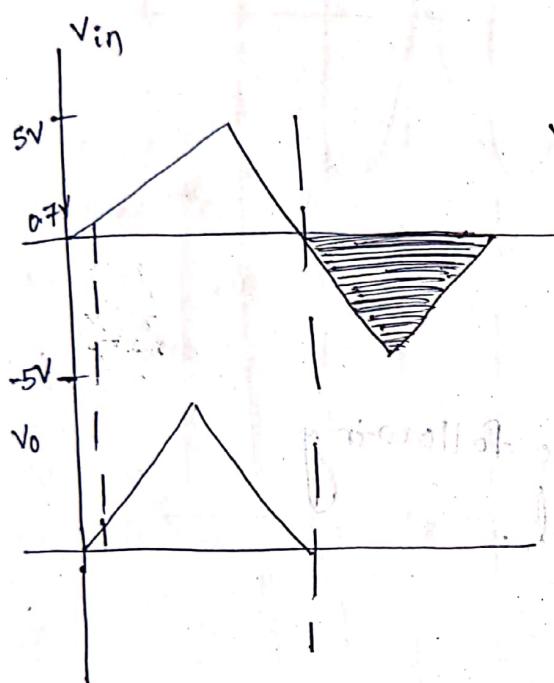
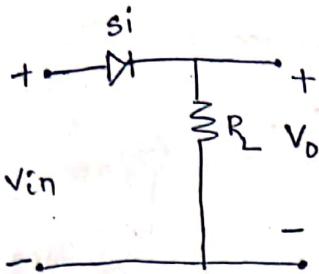
During +ve H.C. :-

Applying KVL; $V_{PIV} + V_m + V_m = 0$

$$\Rightarrow V_{PIV} = [-2V_m] = 2V_m$$

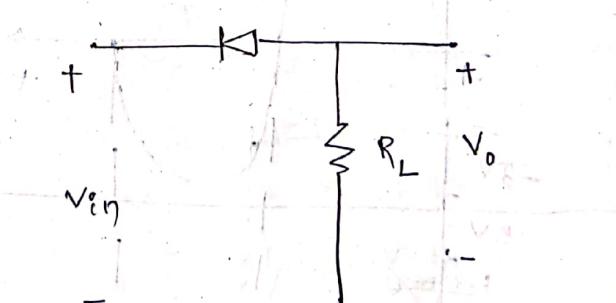
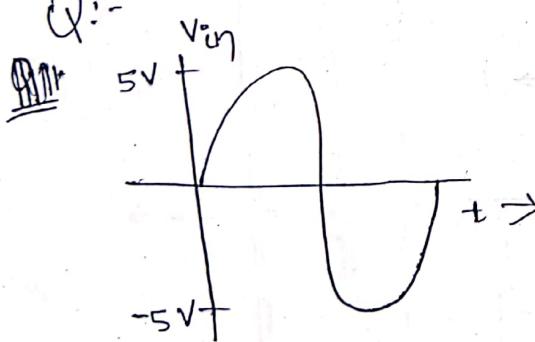
Clippers:-

→ It is an electronic circuit consisting of diode, resistor; which is used to clip or remove some portion of apply input signal.

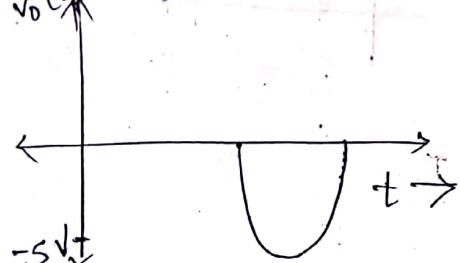


$$V_o = 1.6 \text{ V}$$

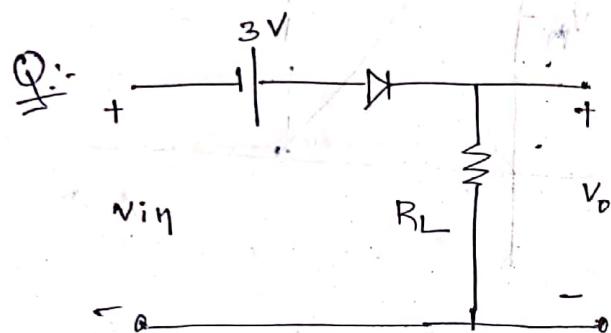
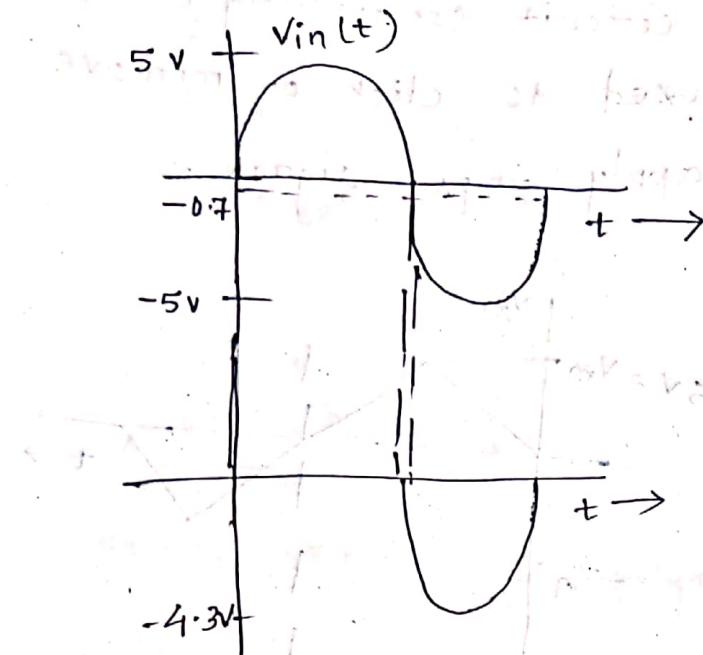
Q:-



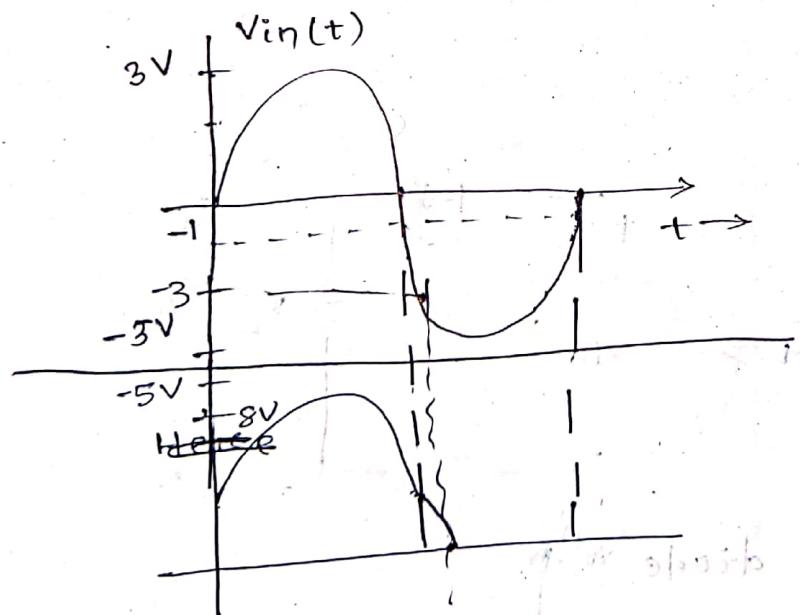
Hence; for ideal diode $V_o(t)$

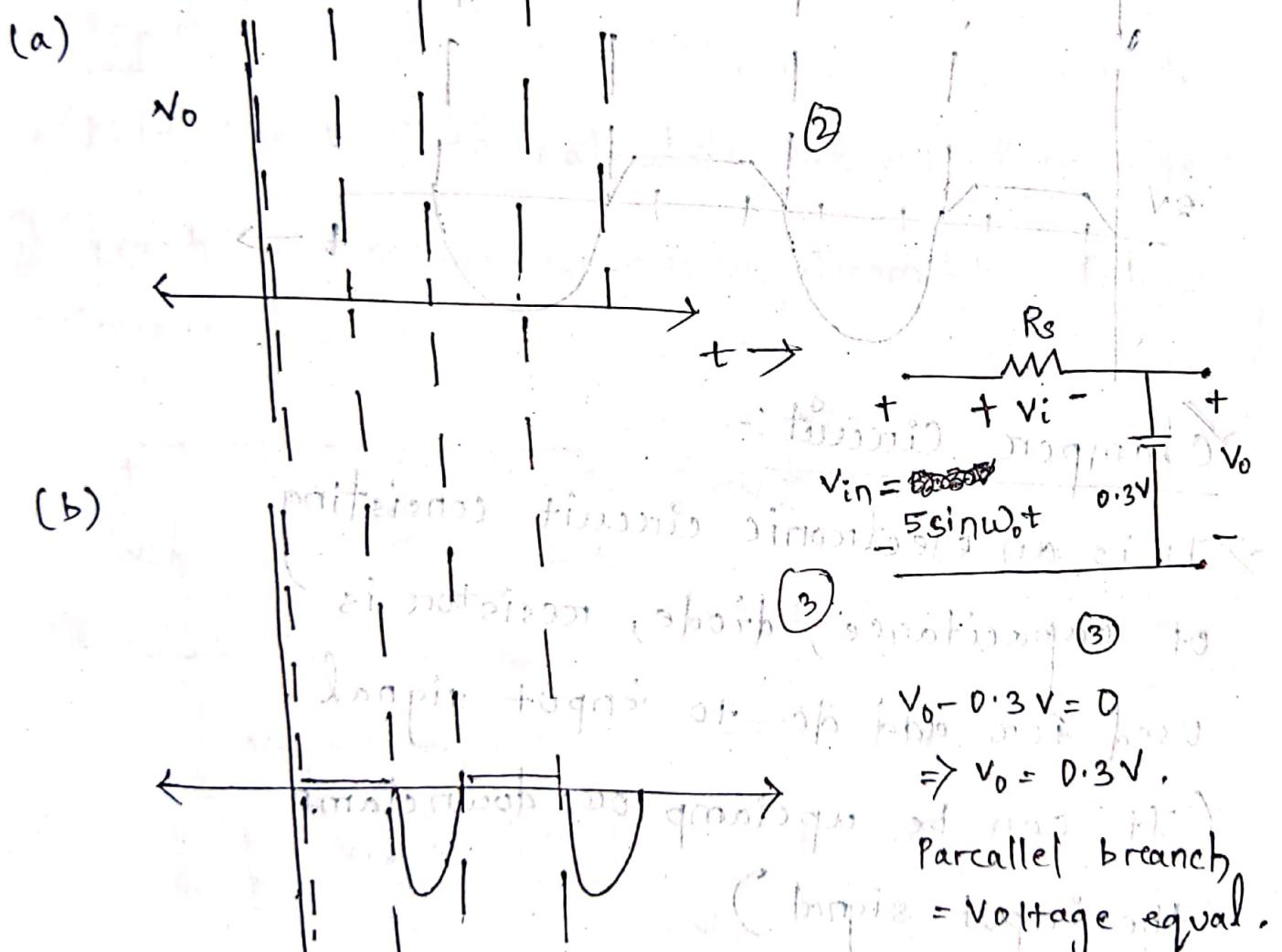
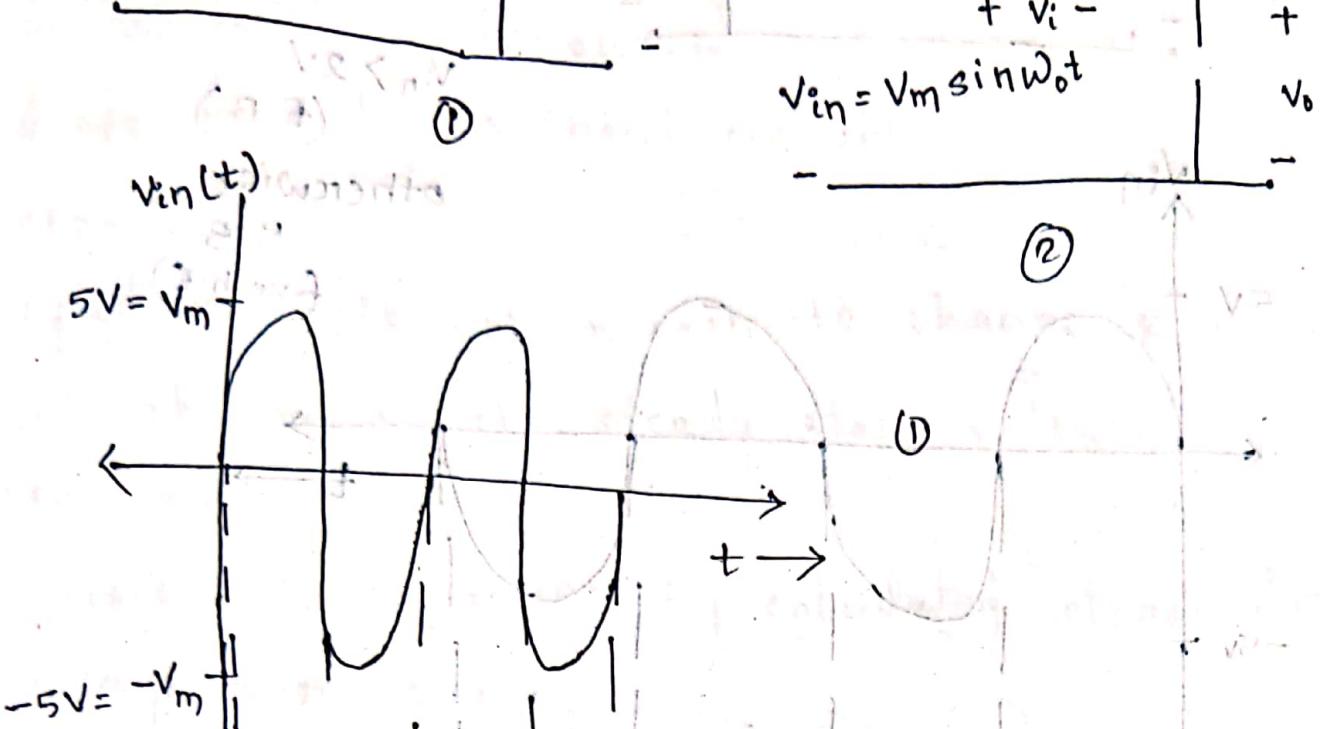


$$v = 0.7v \quad (\text{Non-ideal})$$

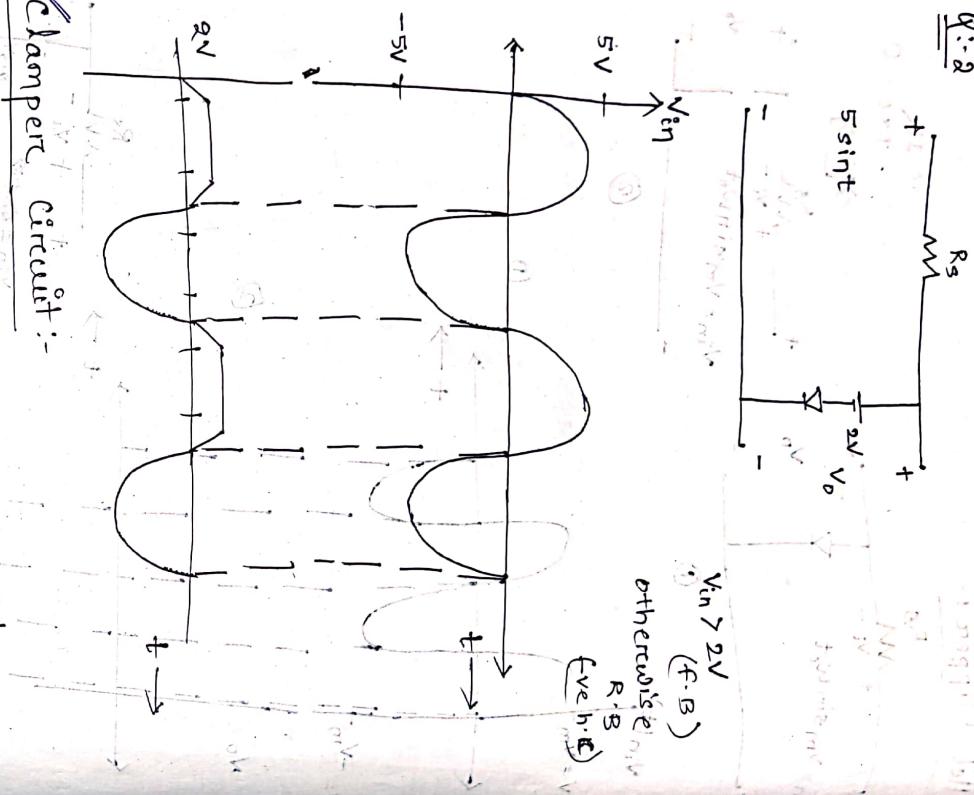


Sketch the output of the following
conside the diode is ideal.

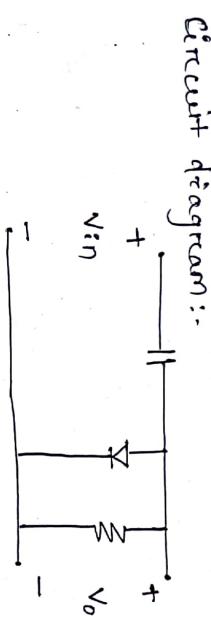




Q.2



- Clamper circuit :-
- It is an electronic circuit consisting of capacitance, diode, resistor is used for add dc to input signal.
- (It can be up clamp or down clamp the input signal)



steps / Procedure to analysis the clampere circuit:-

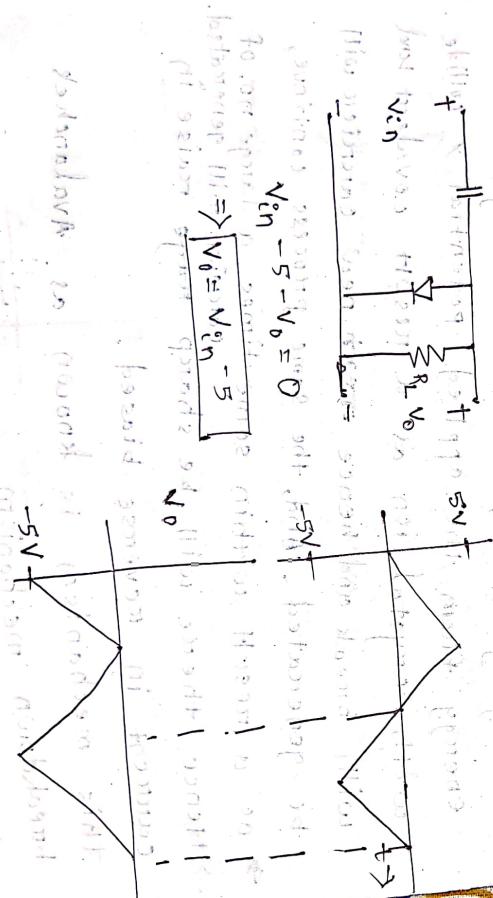
Step-1:- Start the analysis of clampere circuit from that part of half cycle of input such that the diode will be forward biased & replace the diode with by a short circuit.

Step-2:- Now switch on the DC voltage source. The capacitor will gets a path to charge & it will charge to its steady state voltage.

Step-3:- Replace the capacitor by calculated steady state voltage from step 2; now solve for output voltage.

Step-4:- Now draw the output waveform. Now apply the KVL to calculate the output voltage (V_o)

Q. Sketch the output waveform from the following circuit:



Zener diode

\Rightarrow It is heavily doped P-N junction diode.

\Rightarrow Construction wise both are same but only difference is in doping conc. i.e. in P side, there is more doping.

V-I characteristics :-

\Rightarrow V-I characteristics of zener diode consists up a parts. (1) Forward biased (same as forward junction diode)

(2) Reverse biased

It is divided into 2 parts :-

(a) Non-breakdown (same as normal P-N junction diode)

(b) Break down mechanism :-

\Rightarrow A thermally generated carrier falls down in

(a) Junction diode, which will collide with crystal lattice, as a result covalent bond is

break, & hence carrier will generate,

\Rightarrow Newly generated carrier will get sufficient

energy from the applied potential & collide

with crystal ion as a result covalent bond will break and hence next new carrier will

be generated. And, the same process continue,

\Rightarrow as a result within some times, a large no. of carrier will generate

\Rightarrow Hence there will be sharp rise in current in reverse biased.

This mechanism is known as Avalanche breakdown mechanism.

Zener breakdown

\Rightarrow Due to heavily well bent at the electric field

pull out carrier

be on the ca

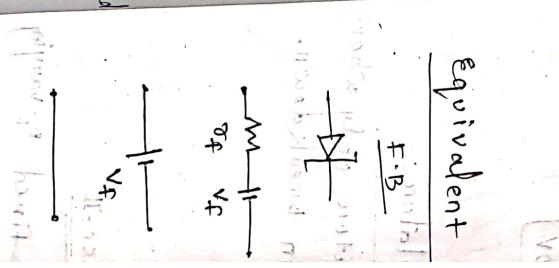
the crystal b

carrier will

pull out car

As a result, there is short range this is

Schematic dr



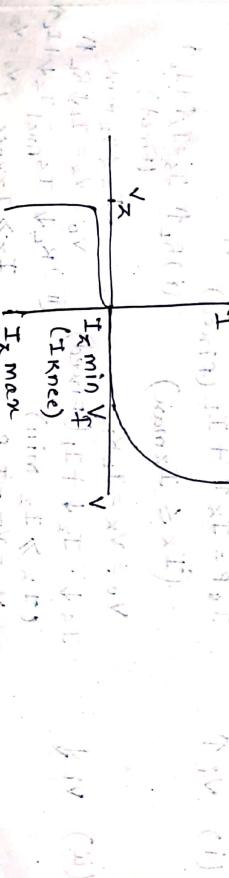
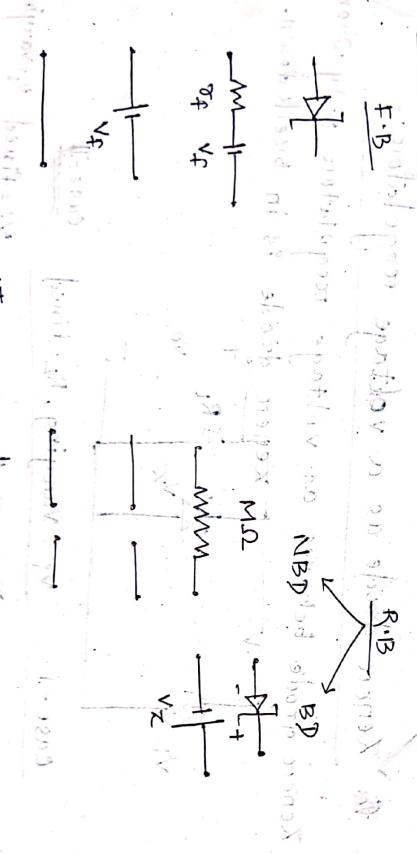
Zener break down:

→ Due to heavily doped, a high electric field will be at the junction, due to the high electric field a large amount of force will be on the carrier. This large force will pull out carrier from the covalent bond of the crystal bond. Also newly generated carriers will have high force & they will pull out carriers from the covalent bond. As a result, large no. of carriers & hence there is short zener raise in current. this is called zener breakdown mechanism.

Schematic diagram of zener diode:-



Equivalent model of zener diode:-

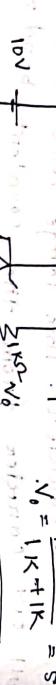


Application :-

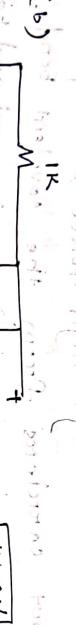
\rightarrow It behaves as voltage regulator.

Calculate V_o for the following circuit.

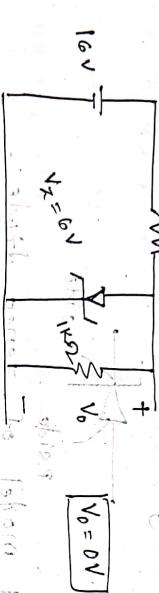
(a)



(b)

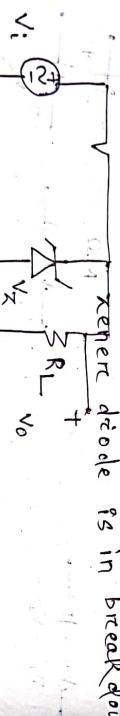


(c)



Kenner diode as a voltage regulator :-

Kenner diode behaves as voltage regulator only when Kenner diode is in breakdown.



Case-I $V_i = \text{varying}, R_L = \text{fixed}$ Case-II

(i) $V_i \uparrow$

$$I_{SP} = I_x \uparrow + I_L (\text{fixed}) \quad V_i = \text{fixed} \quad R_L = \text{varying}$$

$$(I_x \leq I_{x\max})$$

$$V_o = V_x = I_x R_L$$

(ii) $V_i \downarrow$

$$I_S \downarrow = I_x \downarrow + I_L (\text{fixed}) \quad I_x < I_{x\max}$$

$$(I_x \gg I_{x\min}) \quad (i) R_L \downarrow \quad I_{S\text{fixed}} = I_x \downarrow + I_L \uparrow R_L \downarrow$$

$$V_o = V_x = I_x R_L \quad (ii) I_x \gg I_{x\text{knee}}, V_o = V_x$$

Transistor

Date:

Transistor =

It is a 3 terminal electronic device (one terminal is input , second terminal is output and 3rd terminal is controlling terminal) which is used to transfer current through different resistance paths.

Transistor is classified into two —

1) BJT (bipolar junction transistor)

2) FET (field effect transistors)

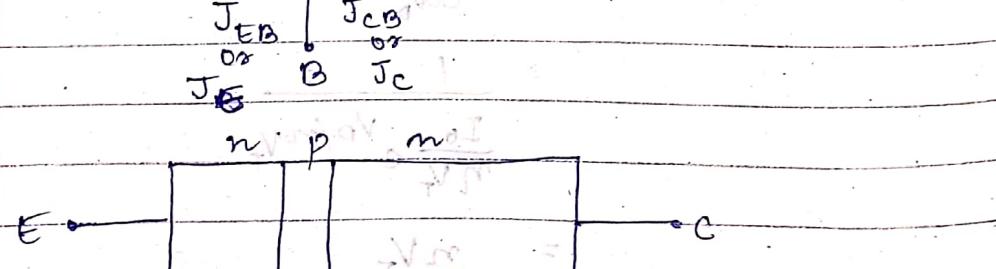
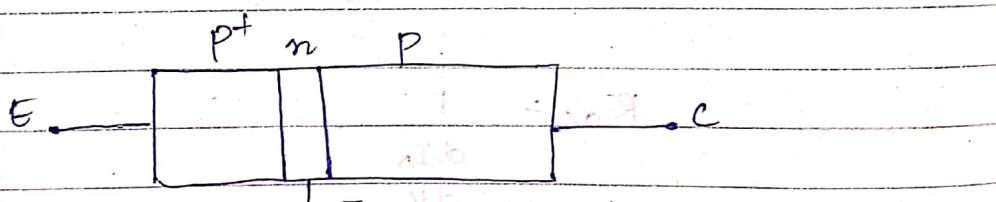
BJT =

In case of a BJT, conduction is due to both ~~more~~ e^- and e^+ , i.e., conduction is due to bipolar carriers (electron \rightarrow -ve and hole \rightarrow +ve).

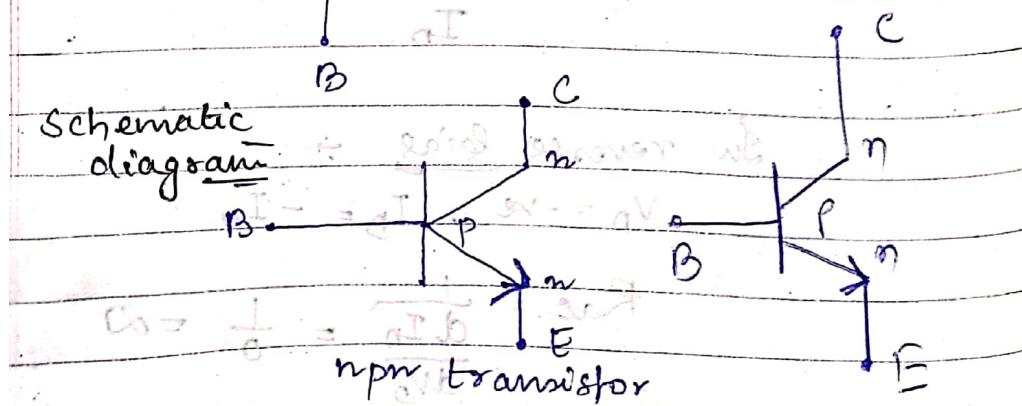
Classification of BJT =

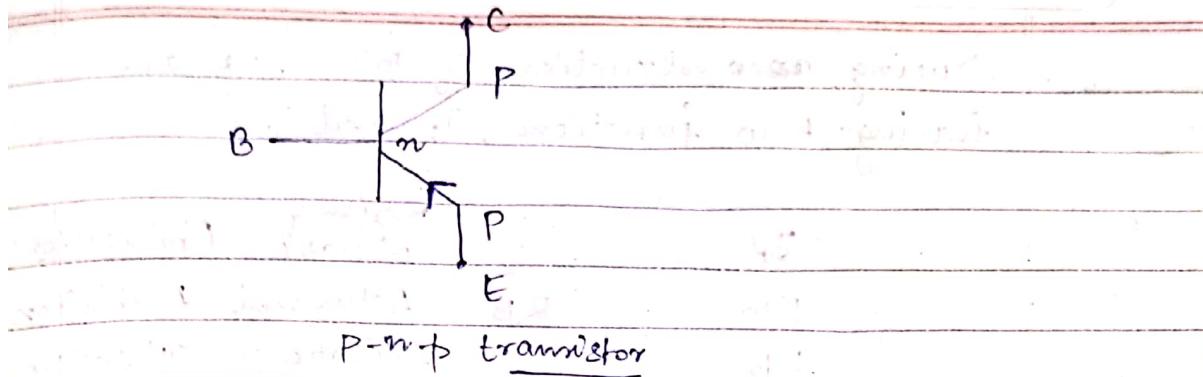
① n-p-n transistor

② p-n-p transistor

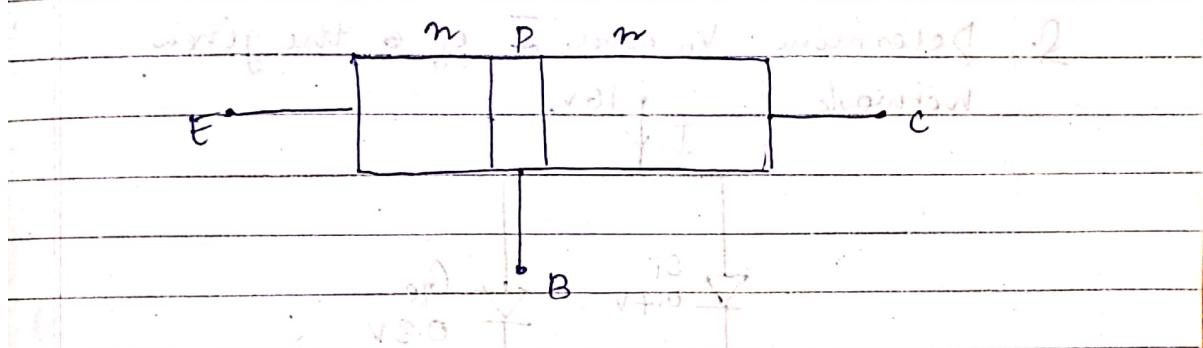


Schematic diagram





Construction of BJT



When two diodes with both p sides of each diode are superimposed with each other results in formation of n-p-n transistor.

there are 3 regions; Emitter region heavily doped with pentavalent impurities, Base region which is lightly doped, and Collector region which is moderately doped.

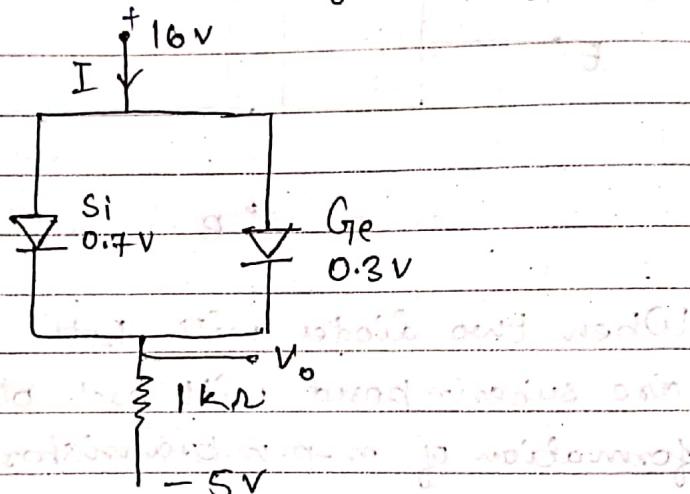
There are two junctions formed over here; one is emitter base junction (emitter junction, J_E) and second is collector base junction (collector junction, J_C).

length of Emitter region is moderate and length of Base region is very narrow and length of Collector region is very large. Length of base region is narrow because to avoid more hole-electron recombination in it so as to transfer a large no. of carriers from Emitter to Collector region.

During construction of BJT, we are having two junctions, J_E and J_C

J_E	J_C	Region of operation Application
F_B	R_B	Active mode Amplifier
F_B	F_B	Saturation " ON switch
R_B	R_B	Cut off " OFF switch
R_B	F_B	Inverse " Attenuator

Q. Determine V_o and I of the given network.



\Rightarrow In 1st case, $I = 0.7 + 0.3 = 1A$

16V - 1A \times 1kΩ = 15V

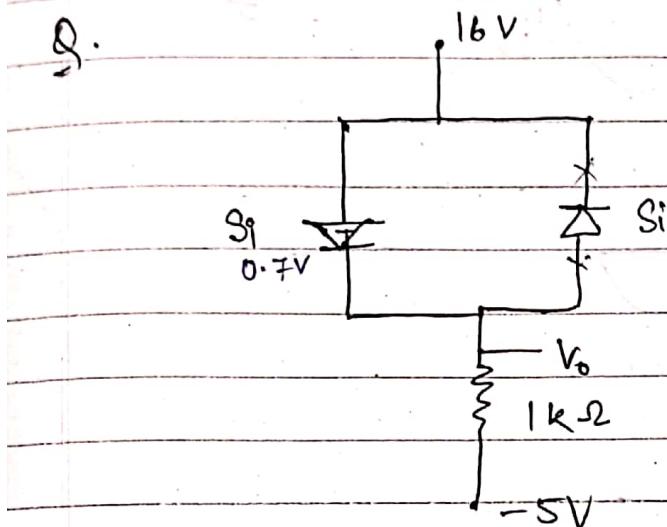
15V - 5V = 10V

$V_o = 10V$

$I = \frac{10}{1k} = 10mA$

$$I_2 = \frac{15.3 - (-5)}{1k\Omega} = 20.3 \text{ mA}$$

Q.

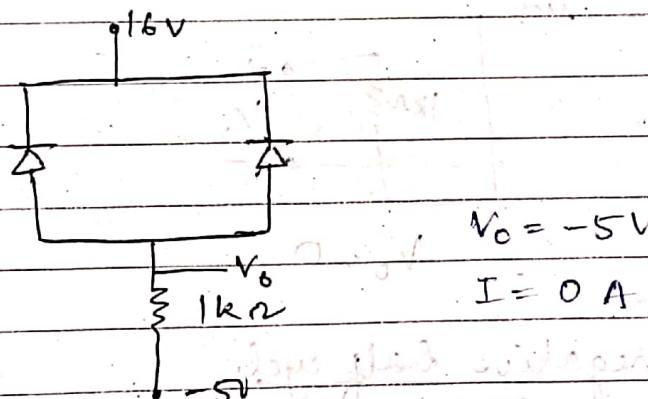


2)

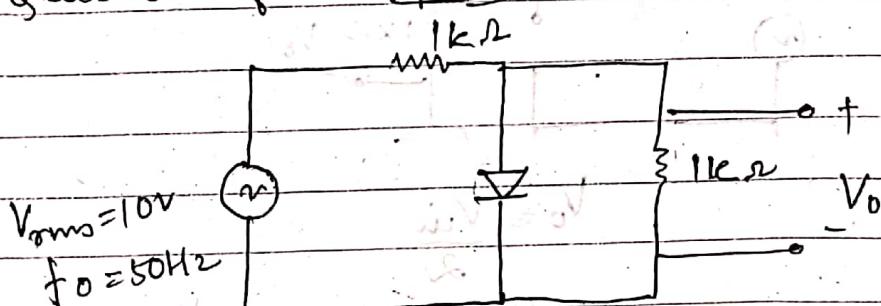
$$V_o = 15.3 \text{ V}$$

$$I = \frac{15.3 - (-5)}{1k\Omega} = 20.3 \text{ mA}$$

Q



Questions of rectifiers :-



Sketch I/O/P, transfer characteristic,

V_{rms} and $V_{o,dc}$

$$2) V_{in} = 10\sqrt{2} \sin 100\pi t \text{ V}$$

$$V_m = 10\sqrt{2} \text{ V}$$

for +ve H.C. :-

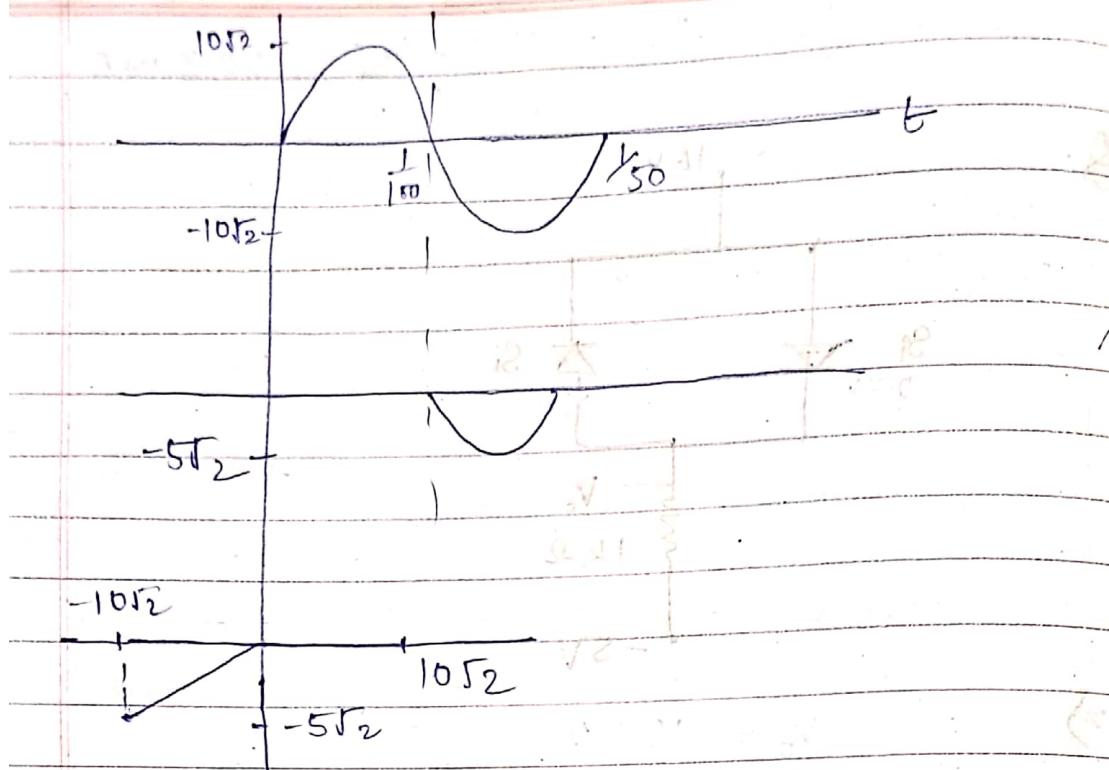
$$V_o = 0 \text{ V}$$

for -ve H.C. :-

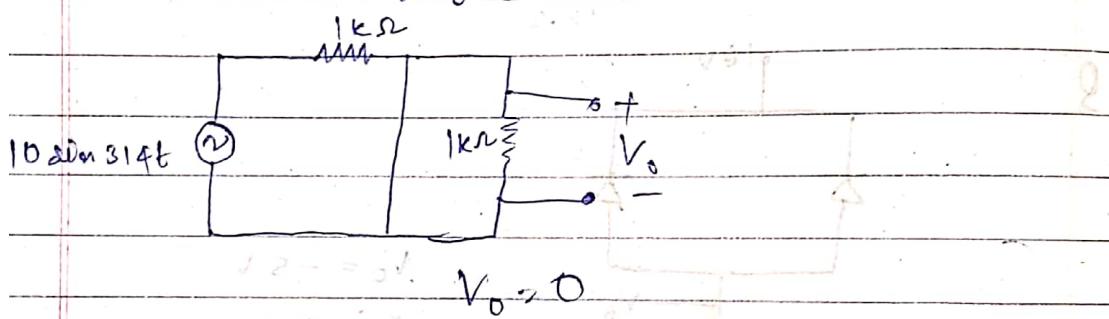
$$V_o = -10 \text{ V}$$

$$V_o = -\frac{10}{2} \times 1 = -5 \text{ V}$$

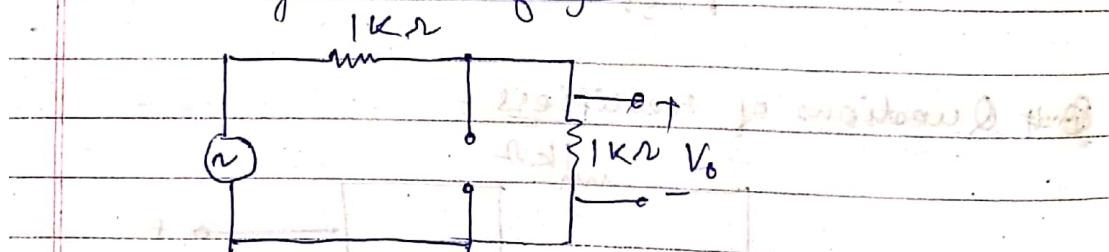
$$= -5 \text{ V}$$

V_{in} 

in +ve half cycle



in negative half cycle



$$V_o = \frac{V_{in}}{2}$$

$$V_o \text{ avg} = \frac{1}{Y_{50}} \int_0^{1/100} 0 dt + \frac{1}{Y_{50}} \int_{1/100}^{1/50} 5\sqrt{2} \sin(100\pi t) dt$$

$$V_o \text{ rms} = \sqrt{\frac{1}{Y_{50}} \int_0^{1/100} 0^2 dt + \frac{1}{Y_{50}} \int_{1/100}^{1/50} (5\sqrt{2} \sin 100\pi t)^2 dt}$$

$$\therefore V_o \text{ rms} = 0$$

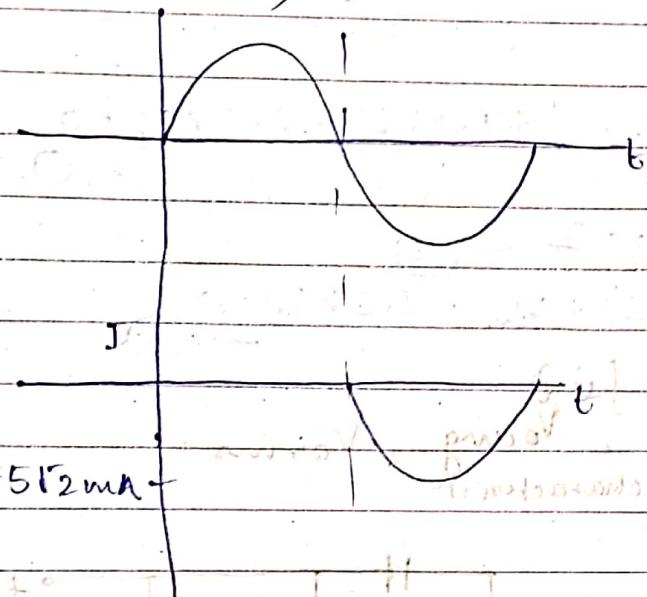
during -ve H.C.:

during +ve H.C.
 $I = 20A$

$$I = \frac{V_{in}}{2K\Omega} = \frac{10\Omega}{2K\Omega} \sin 100\pi t$$

$$= 5\sqrt{2} \sin 100\pi t \text{ mA}$$

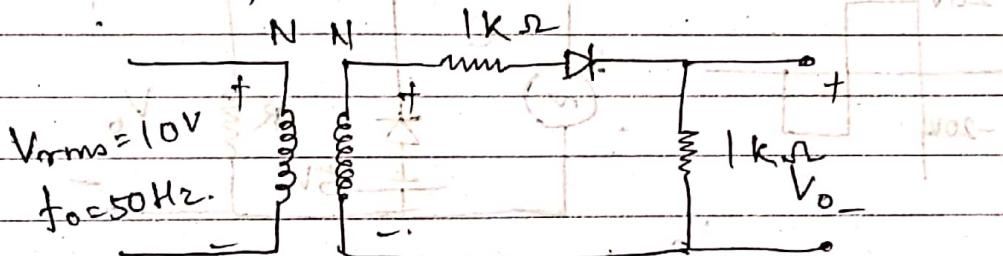
$V_{in}(t)$



$-5\sqrt{2} \text{ mA}$

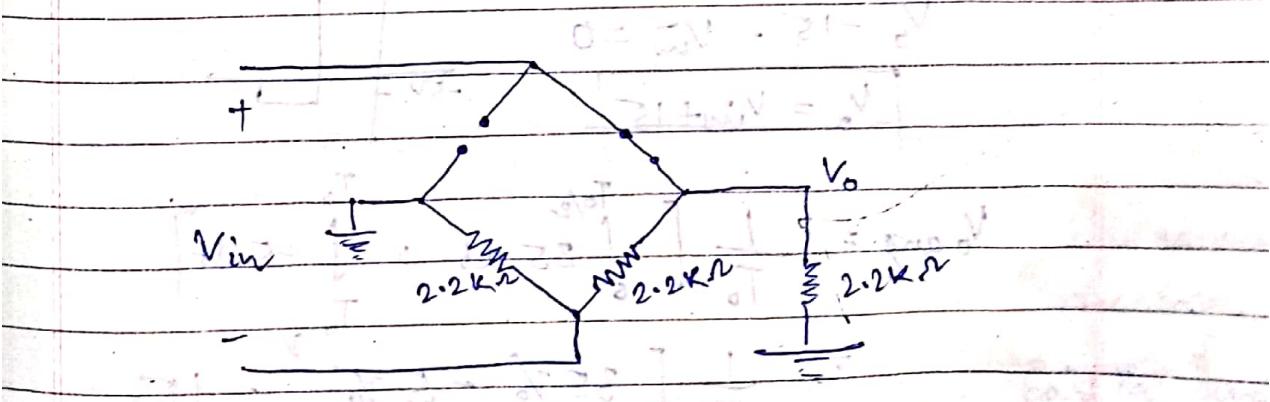
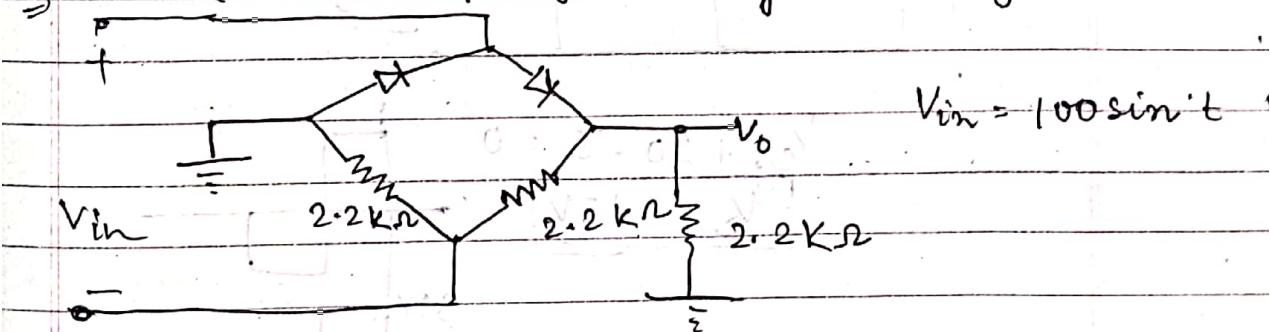
phase of output
is not defined
because not defined

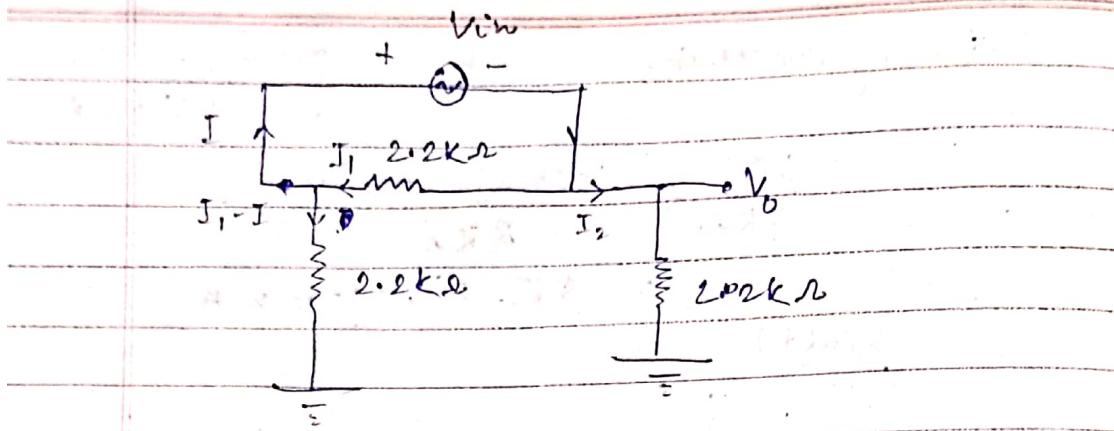
Q.



(Same as prev. question)

Q. Sketch V_o for following circuit given —



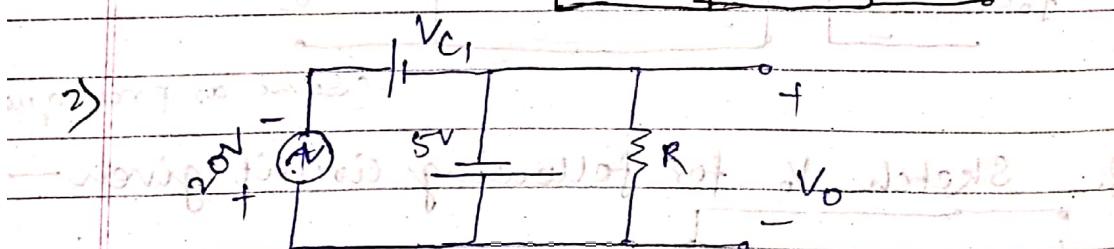
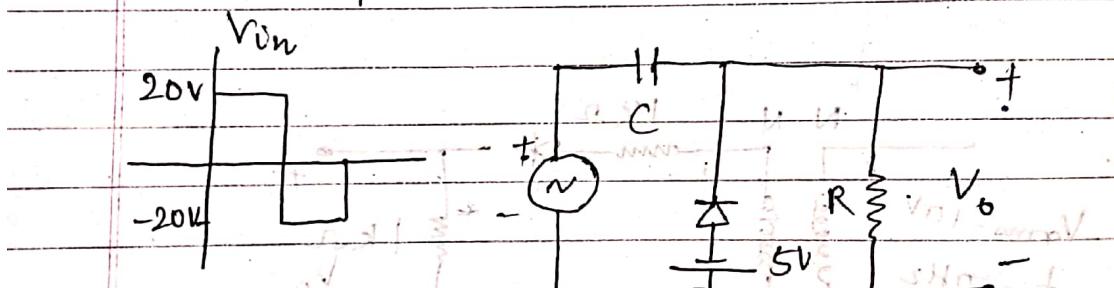


$$2.2K(I_1 - I_2) + 2.2KI_1 - 2.2KI_2 = 0 \quad \text{--- (1)}$$

$$I_1 + I_2 = I \quad \text{--- (2)}$$

$$2.2K(I_1 - I) + V_{in} - 2.2KI_2 = 0 \quad \text{--- (3)}$$

Q Sketch V_o , $V_{o\text{avg}}$, $V_{o\text{rms}}$ transfer characteristic.



$$V_{C_1} + 20 - 5 = 0$$

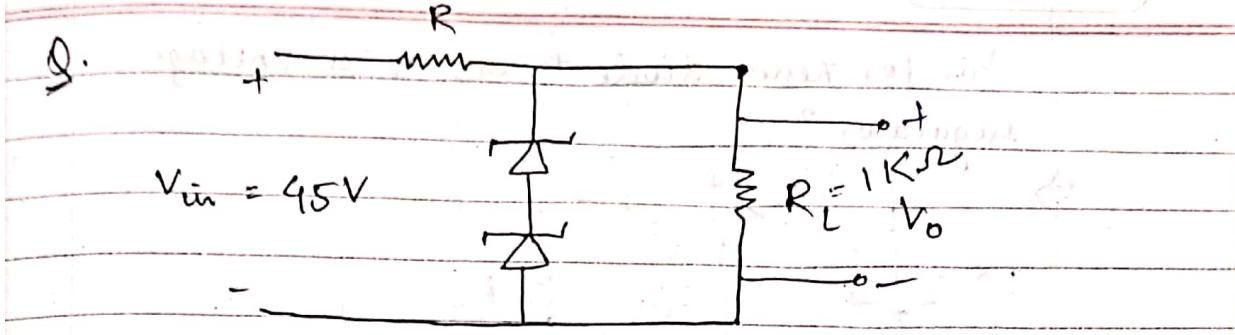
$$V_C = -15V$$

$$V_o - 15 - V_{in} = 0$$

$$V_o = V_{in} + 15$$

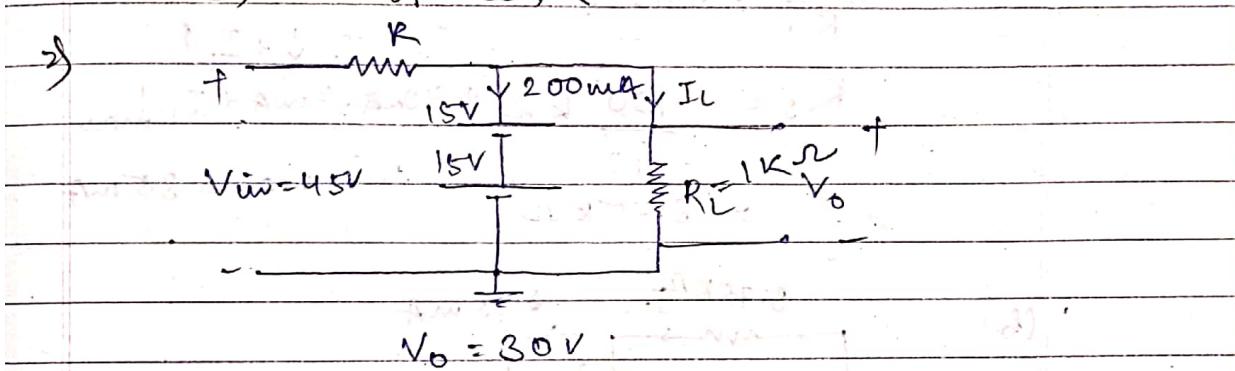
$$V_{o\text{avg}} = -\frac{1}{T_0} \left[\int_{T_0/2}^{T_0/2} 85 dt + \int_{T_0/2}^{T_0} -5 dt \right]$$

$$= -\frac{1}{T_0} \left[35 \frac{T_0}{2} - 5 \frac{T_0}{2} \right] = 15V$$



each 2 zener diode rated as 15V, 200mA
If circuit is connected to 45V unregulated supply, determine -

- regulated o/p voltage across R_L
- resistance, R



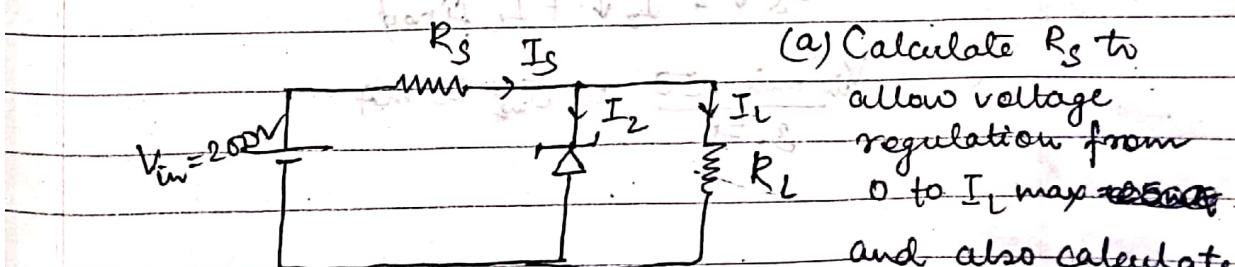
$$I_L = \frac{30 - 0}{1k\Omega} = 30mA$$

$$I = 230mA$$

$$I = \frac{45 - 30}{R}$$

$$R = \frac{15}{230} k\Omega$$

Q. If a 50V, 5-40mA Zener diode is used as shown in regulated circuit -



and also calculate I_L max

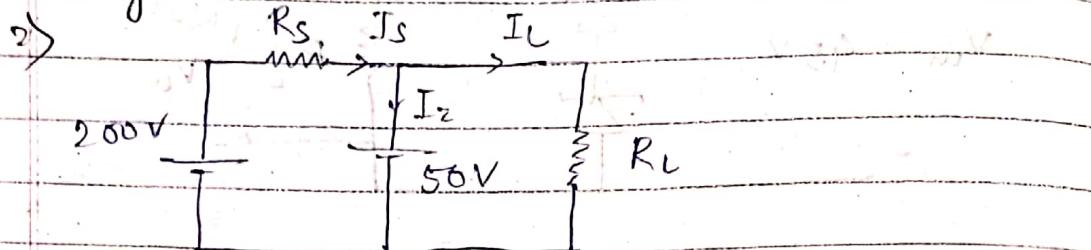
(b) If R_s is set as found in part (a) and I_L is fixed at 25mA then what is range of I_s

When Zener diode is given in voltage regulator mode, it is always in B.D region.

Page No.:

Date:

V_{in} for Zener diode to act as a voltage regulator?



(a) When $V_{in} = 200V$, $I_S = I_Z + I_L$

$$I_S = 40mA + 0mA \quad (\text{at } V_{in} = 200V)$$

$$I_S = 40mA \quad (\text{at } V_{in} = 200V)$$

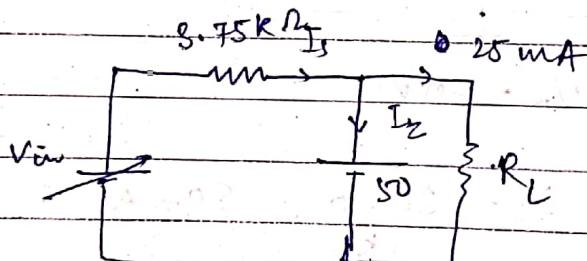
$$\frac{200 - 50}{R_s} = 40mA \quad (\text{at } V_{in} = 200V)$$

$$I_S = I_Z + I_L$$

$$R_s = \frac{150}{40} k\Omega \Rightarrow 40mA = 5mA + I_{Lmax}$$

$$\therefore I_{Lmax} = 35mA$$

(b)



When $V_{in} \uparrow$

$$I_S \uparrow = I_Z \uparrow + I_L \text{ fixed}$$

$$I_{Smax} = 40mA + 25mA = 65mA$$

$$\therefore V_{in max} = \frac{50}{3.75k\Omega} = 65mA$$

(c) When $V_{in} \downarrow$

\rightarrow Zener diode breakdown in reverse bias

$$I_S \downarrow = I_Z \downarrow + I_L \text{ fixed}$$

For breakdown (a)

$$V_{in min} = \frac{50}{3.75} = 5mA + 25mA$$

of breakdown

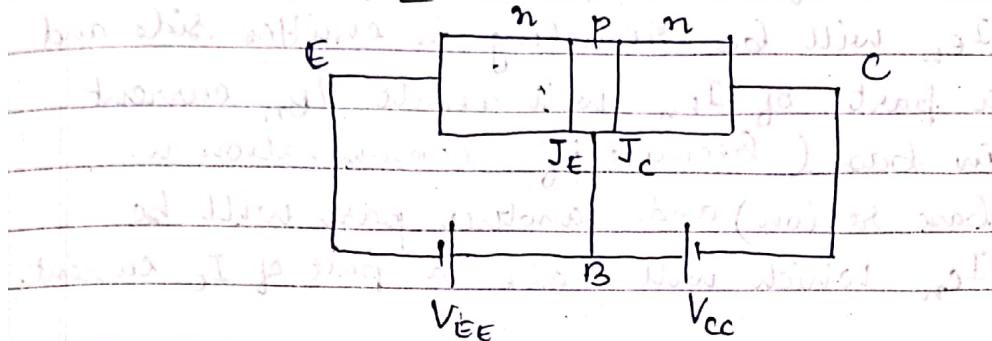
\rightarrow $I_S \downarrow$ at $V_{in} = 50V$

Date
26/02/19

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Units

Operation of BJT \Rightarrow different modes of operation



NOTE \Rightarrow if $V_{EE} > V_{CC}$ then J_E is more F.B.

Saturation region of operation \Rightarrow J_C is more R.B.

Forward

Saturation

Reverse bias

Saturation

If $V_{EE} > V_{CC}$

i.e. J_E is more

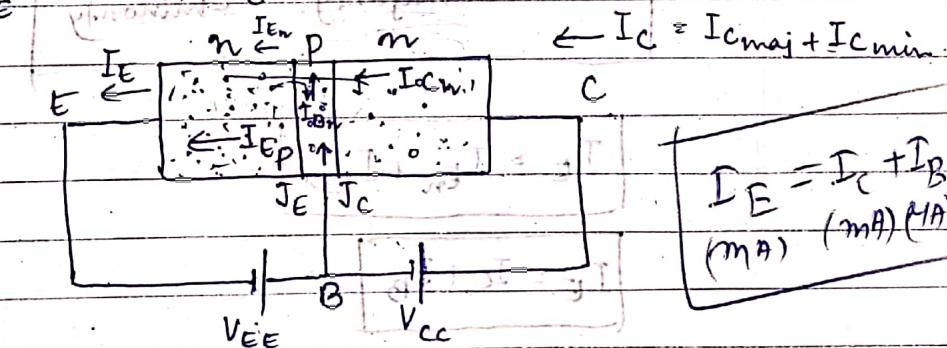
~~F.B than J_C~~ than J_E is more F.B than J_C.

If $V_{EE} < V_{CC}$

i.e. J_C is more R.B

In active region \Rightarrow

$J_E \rightarrow F.B, J_C \rightarrow R.B$



~~so either J_E is FB by application of V_{EE} as~~

~~shown above and J_C is RB by applying V_{CC} .~~

Due to $J_E \rightarrow F.B$, the majority carrier e^- in emitter will diffuse and ~~no~~ recombination takes place in base region and a large no. of

diffused carriers from emitter will ~~will~~ drift towards collector because base is lightly doped and

~~so narrow base width~~ \Rightarrow no drift

Because of this diffusion, a diffused current I_{E_n} will be resulting in emitter side and a part of I_{E_n} will result I_{B_n} current in Base (Because of recombination in base region) and another part will be I_{C_n} which will make a part of I_c current.

Because of V_{EE} , there will be some minority current I_{E_p} which is some part of emitter current and I_{B_p} in base which is a part of base current, as a result

$$I_E = I_{E_n} + I_{E_p}$$

Due to $J_c \rightarrow R_B$, a collector majority current and minority current and total collector current -

$$I_c = I_{c\text{ majority}} + I_{c\text{ minority}}$$

$$I_E = I_{E_n} + I_{E_p}$$

$$I_E = I_c + I_B$$

Configuration of BJT :-

1. Common Base (CB) mode.

2. Common Emitter (CE) mode.

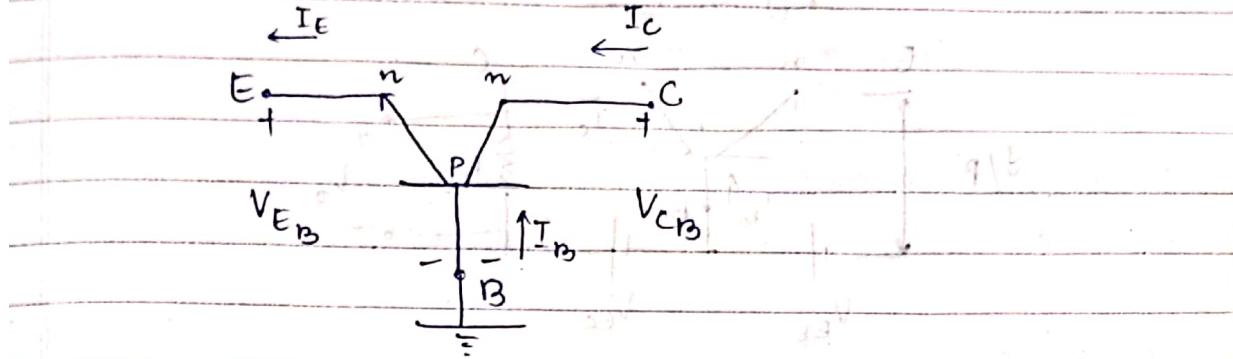
3. Common Collector (CC) mode

to learn about it has named said with help of

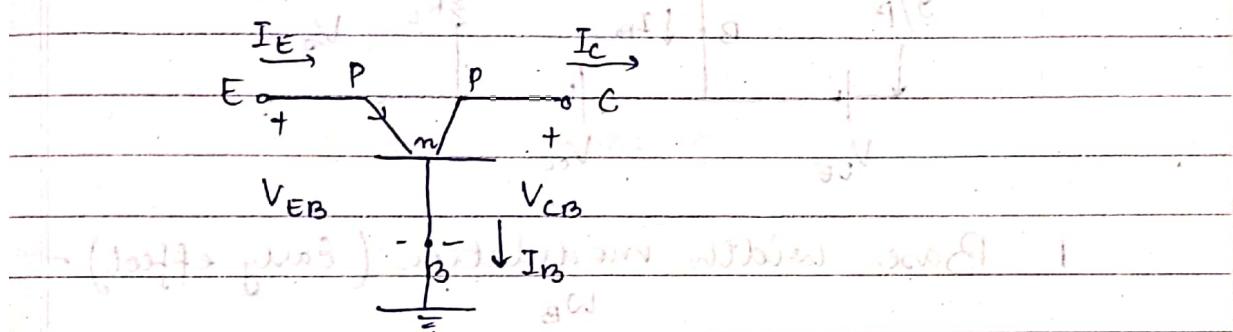
Common Base mode easiest to understand

if Base terminal is common to both input and output of BJT is known

as common base.



for common base configⁿ, input current is I_E and V_{EB} is input voltage and V_{CB} output voltage and $I_C \rightarrow$ output current.



here V_{EB} , I_E , V_{CB} and I_C are four variables out of which two variables are dependent variable and remaining two are independent variable.

- Current Amplification factor in CB \Rightarrow

$$\alpha \triangleq \frac{\Delta I_C}{\Delta I_E} \Rightarrow \frac{I_C - I_{C\text{minority}}}{I_E - 0} = \alpha$$

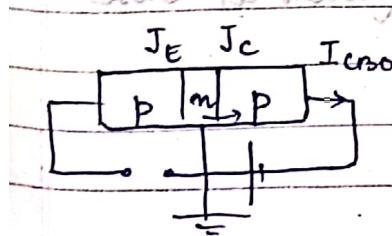
It is defined as the ratio of change in I_C & I_E .

Now this ratio is α of $I_C - I_{CBO}$ & I_E .

Now $\alpha = I_C - I_{CBO}$ & I_E .

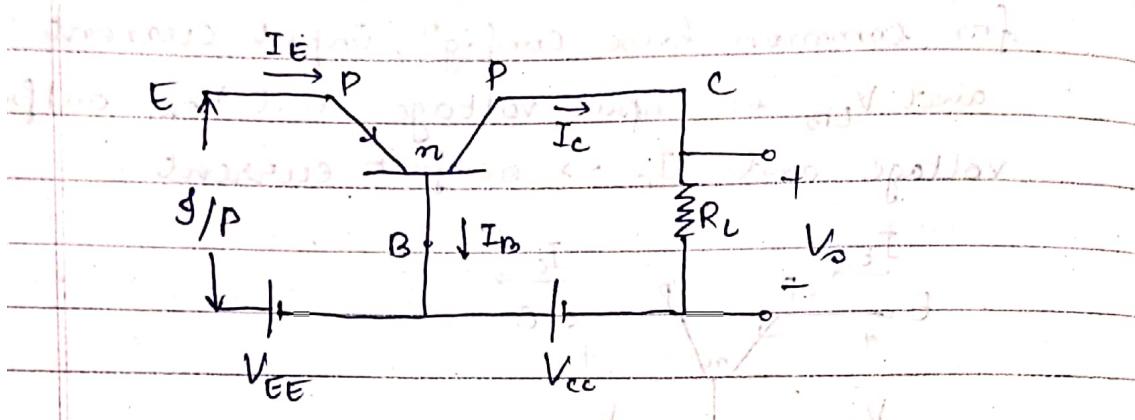
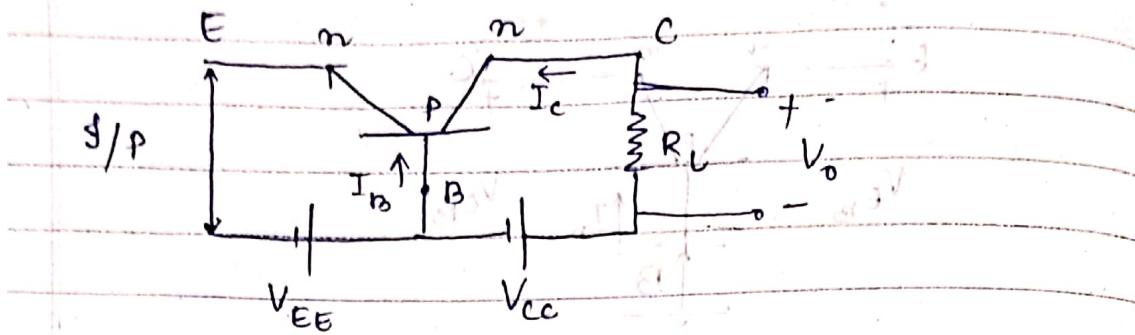
$I_C = I_E + I_{CBO}$

$I_C = I_E + I_{CBO}$

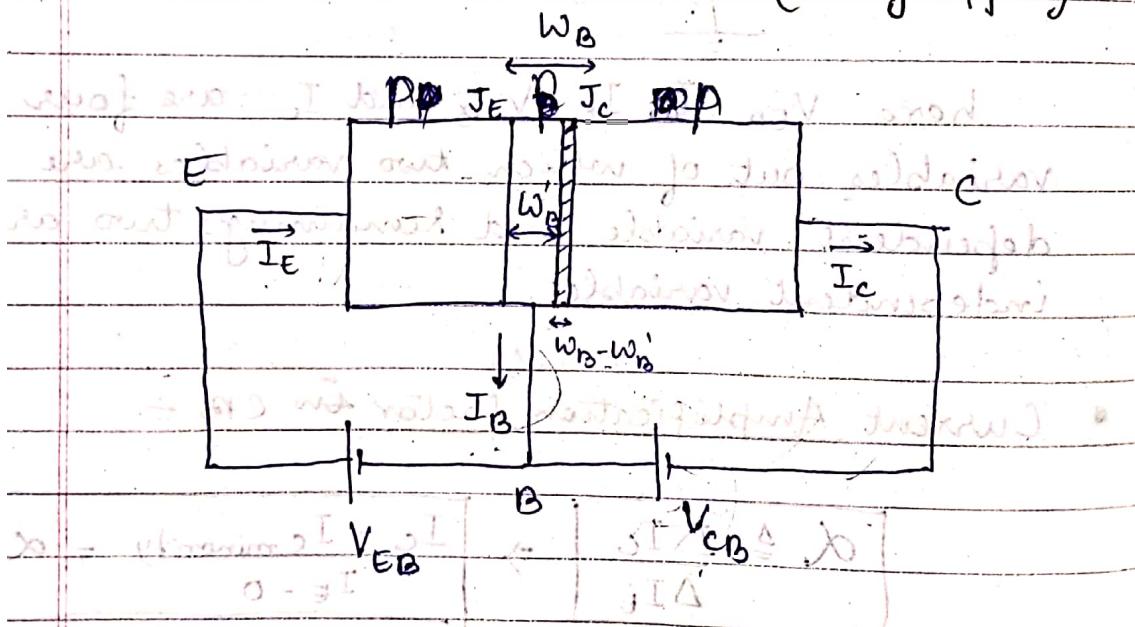


I_{CBO} is reverse saturation current in CB configⁿ with open ~~emitter~~ J_E .

• C-B configuration :-



I. Base width modulation (Early effect) :-



Ques:- By increasing V_{CB} , i.e., by increasing $R_{B} \rightarrow J_C$, effective base width will decrease (depletion region will more penetrate towards lightly doped side).
As effective base width changes with change in V_{CB} , this is known as Base width modulation.

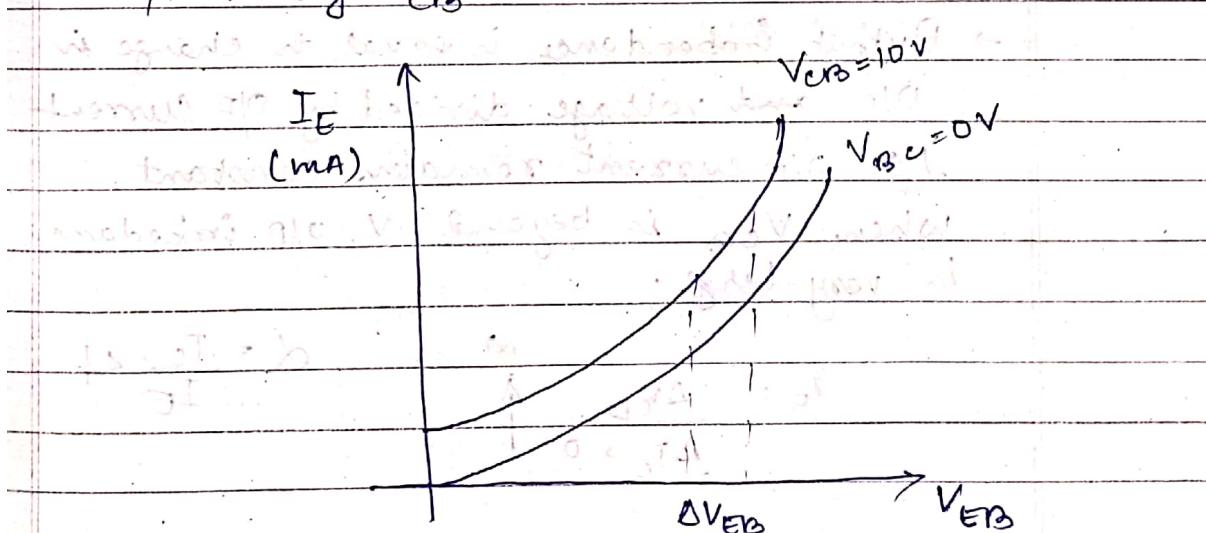
Ans:- When V_{CB} increases, J_C increases, R_B decreases, I_B increases, I_C increases, V_o increases.

Effect 1 \rightarrow By increasing V_{CB} , effective base width will decrease and hence less recombination will take place in base region so more no. of majority carriers will swift from E to C side and hence α increases.

Effect 2 \rightarrow By increasing V_{CB} , concⁿ gradient increase and hence I_E increases.

Effect 3 \rightarrow By increasing V_{CB} in large amount, eff. base width will disappear and this condⁿ is known as reach through / punch through.

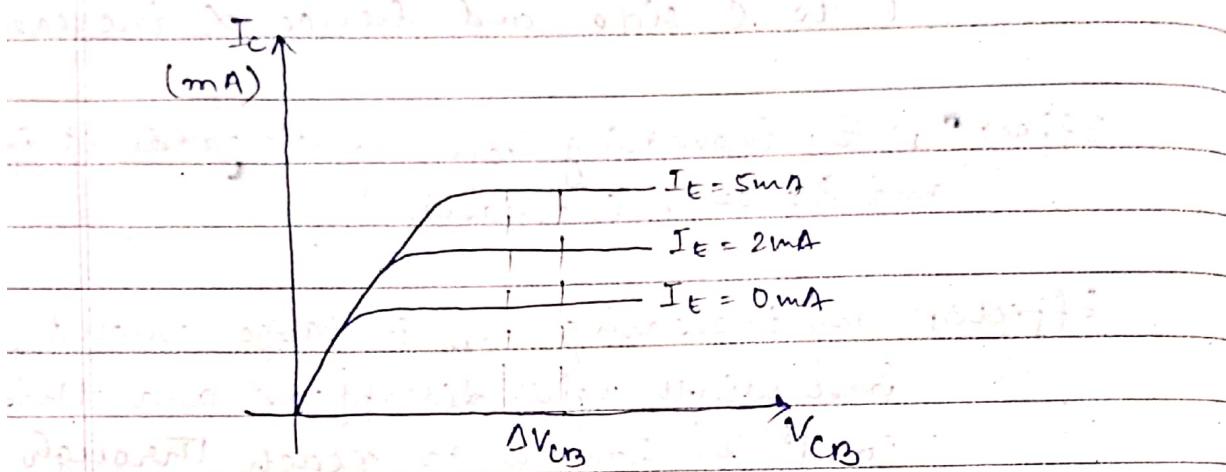
Input Characteristics:
This is the characteristics curve betⁿ I/P curve voltage V_{EB} and input current I_E by keeping o/p voltage V_{CB} const.



I_E is rapidly increased with small change in I/P voltage V_{EB} due to β effect.
→ $\Delta I_E \propto \Delta V_{BE}$ (most at saturation)
→ the input impedance of CB config is less.
→ I_E is almost independent of V_{CB}

Output characteristics :

It is a characteristics curve between O/P voltage V_{CB} and O/P current I_C keeping input current I_E constant.



→ I_C varies with V_{CB} at very low voltage, most probably less than 1V.

→ When V_{CB} increases beyond 1V, I_C is

constant because of early effect.

→ Output impedance is equal to change in O/P voltage divided by O/P Current

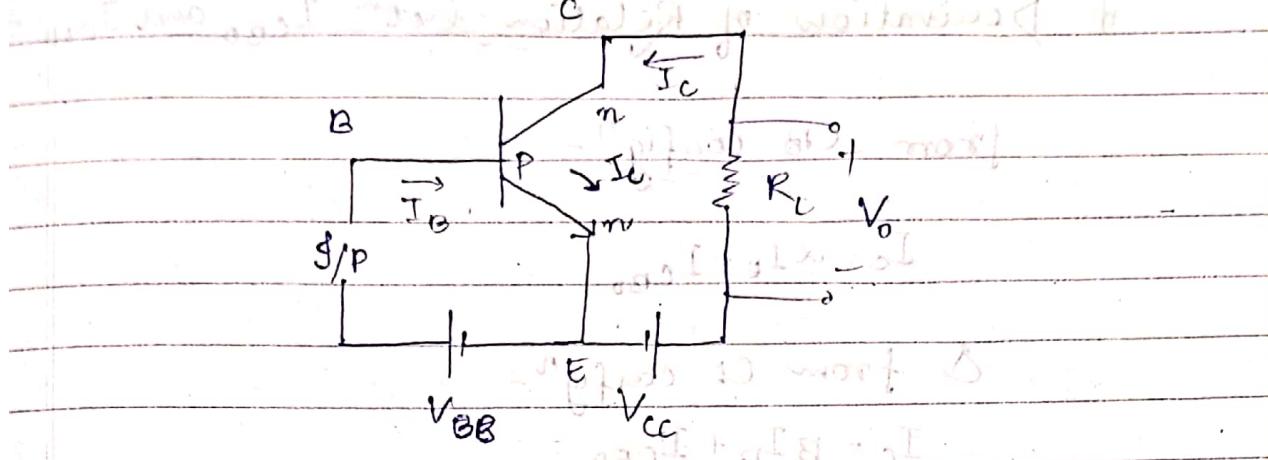
As O/P current remains constant

when V_{CB} is beyond 1V, O/P impedance is very large.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \xrightarrow{I_C \rightarrow 0} \infty \quad \alpha = \frac{I_C}{I_E} < 1$$

Common Emitter Config :

The config of BJT in which emitter is common to both S/P and O/P is known as common emitter config. S/P is applied betw. B and E and O/P is taken betw. C and E.



- Common emitter Amplification factor (β) \doteq
 β is defined as change in O/P current and
change in S/P current

$$\beta \doteq \frac{\Delta I_C}{\Delta I_B} = \frac{I_C - I_{CEO}}{I_B - 0}$$

$$\rightarrow I_C = \beta I_B + I_{CEO}$$

Amplification leakage/
factor current minority current

- Relationship betⁿ α and β \doteq

$$\text{From above } \beta = \frac{\Delta I_C}{\Delta I_B}, \quad \alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_C + I_B$$

$$\Delta I_E = \Delta I_C + \Delta I_B$$

$$\rightarrow \frac{\Delta I_E}{\Delta I_C} = \frac{\Delta I_C}{\Delta I_C} + \frac{\Delta I_B}{\Delta I_C}$$

$$\rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\rightarrow \alpha = \frac{\beta}{\beta + 1}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

Derivation of Relation betw I_{CBO} and I_{CEO} :

from CB config:

$$I_C = \alpha I_E + I_{CBO}$$

& from CE config:

$$I_C = \beta I_B + I_{CEO}$$

$$\Rightarrow I_C = \beta (I_E - I_C) + I_{CBO}$$

$$\Rightarrow (B+1) I_C = \beta I_E + I_{CEO}$$

$$\Rightarrow I_C = \frac{\beta}{B+1} I_E + \frac{1}{B+1} I_{CEO} \quad \textcircled{1}$$

$$\text{Also, } I_C = \alpha I_E + I_{CBO} \quad \textcircled{2}$$

Comparing $\textcircled{1}$ & $\textcircled{2}$:

$$\alpha = \frac{\beta}{B+1}$$

$$I_{CBO} = \frac{1}{B+1} I_{CEO}$$

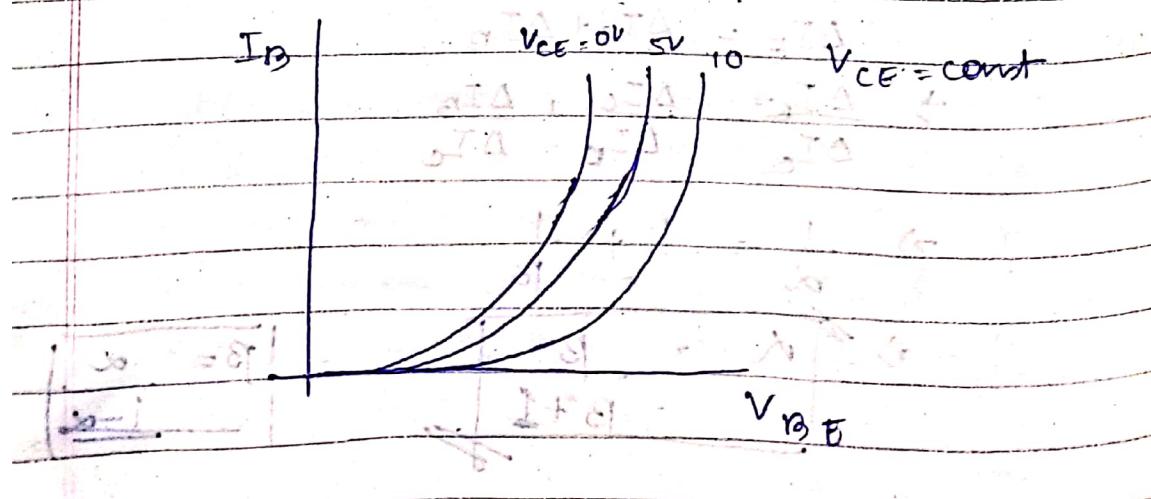
$$\Rightarrow I_{CEO} = (B+1) I_{CBO}$$

Input characteristics:

This is the input characteristic curve betw

I/P current I_B and I/P voltage V_{BE}

keeping O/P voltage V_{CE} constant.

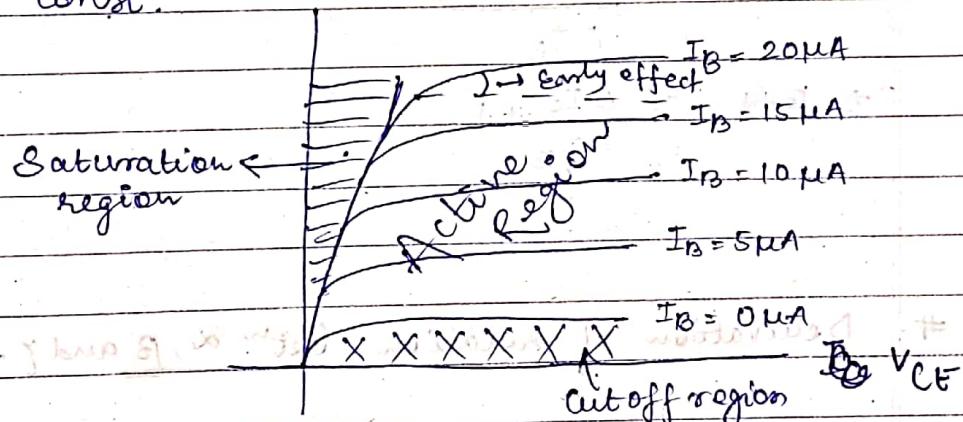


- The input characteristics resembles that of forward bias of diode as BE section of a transistor as forward biased diode at $V_C = 0V$.
- As V_{CE} increases, ~~these will be~~ effective base width will decrease as a result, less recombination in base region and hence less base current.
- As compared to common base, I_B increases less rapidly with V_{BE} . ~~so~~ So, S/P impedance of a CE is higher than S/P impedance of a CB

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at } V_{CE} \text{ const}$$

Output characteristics :

It is the characteristic curve betⁿ O/P voltage V_{CE} and O/P current I_C keeping S/P current I_B const.



The curve of I_B are not horizontal as those obtained in I_E in CB config. So, V_{CE} will influence the magnitude of I_C .

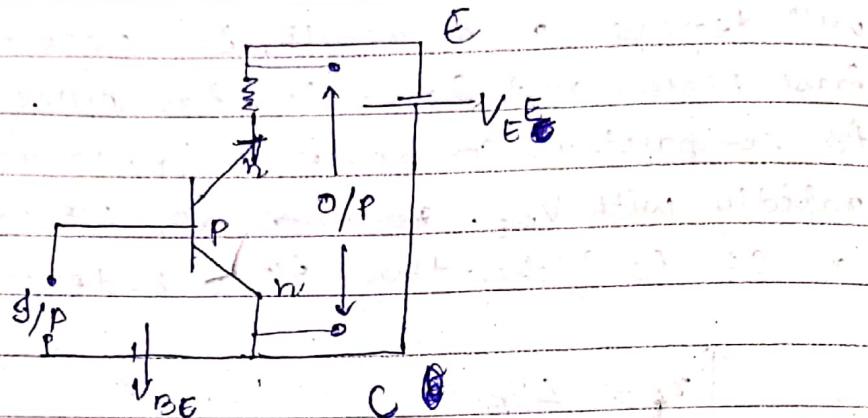
$$\text{Output impedance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

\rightarrow ~~for CB config~~ $r_o = \frac{\Delta V_{CE}}{\Delta I_C}$ (at I_E constant)

~~at this current, r_o is minimum~~

Common Collector Config:

In CC config of BJT, S/P is applied betⁿ base and collector and O/P taken betⁿ emitter and collector.



(Y)

Current Amplification factor for CC config:-

$$\text{Defn. } \gamma \stackrel{\Delta}{=} \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} + 1 = \frac{\Delta (I_C + I_B)}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_B} + 1$$

$$\Rightarrow \beta + 1 = \frac{\Delta I_C}{\Delta I_B} + 1$$

Derivation of relation betⁿ α , β and γ :

$$\text{As } \gamma = \beta + 1, \beta = \alpha$$

$$\therefore \gamma = \alpha + 1 = \frac{1+\alpha}{1-\alpha}$$

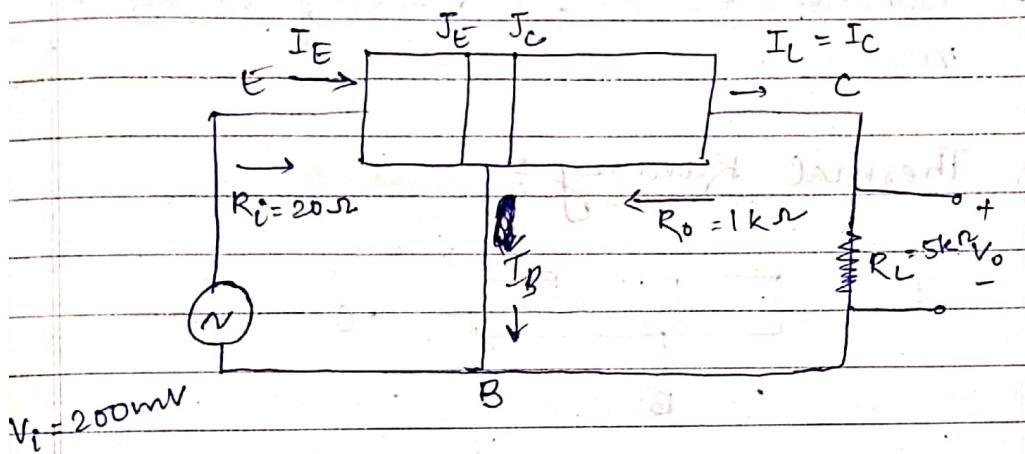
Comparison betⁿ CC, CE, and CB config:

Comparison is done with the characteristic parameters of BJT like S/P impedance (Z_i), O/P impedance (Z_o), current gain (A_I), A_v (voltage gain) and power gain (A_p).

Note: CE is best for amplification because CE config' is having both voltage and current gain.

Parameter	CB	CE	CC
Z _i	Low	Moderate	V. high
Z _o	High	Medium	Low
A _v	High	Medium	High Low
A _I	Low	Medium	High
A _p	No	Yes	Yes

Transistor as an Amplifier



for amplification of BJT, it must be in active mode (emitter $J_E \rightarrow J_B$ and $J_C \rightarrow R_B$) and

$$I_C = \beta I_B + (\beta + 1) I_{CBO} \longrightarrow CE$$

$$I_C = \alpha I_E + I_{CBO} \longrightarrow CB$$

1mA \approx 1μA

\downarrow neglected

$$I_C \approx I_E$$

$$\therefore I_C = \frac{V_i}{R_i} = \frac{200mV}{20\Omega} = 10mA$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{10mA}{100} = 100μA$$

$$\therefore V_o = I_B R_L = 100μA \times 5kΩ = 500mV$$

$$\therefore V_o = 500mV = 0.5V$$

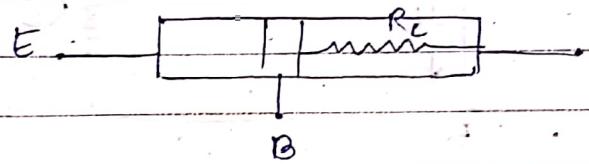
$$A_v = \frac{V_o}{V_i} = \frac{0.5V}{200mV} = 250$$

BJT biasing :-

Need of biasing -

- For faithful amplification, there should be exact replica reproduction of I/P ^{at} O/P.
- Biasing is needed for faithful amplification
 - Biasing circuit is needed to make $I_c(\text{dc})$ independent of B .
 - Biasing is needed for avoiding the thermal runway.

• Thermal Runway :-

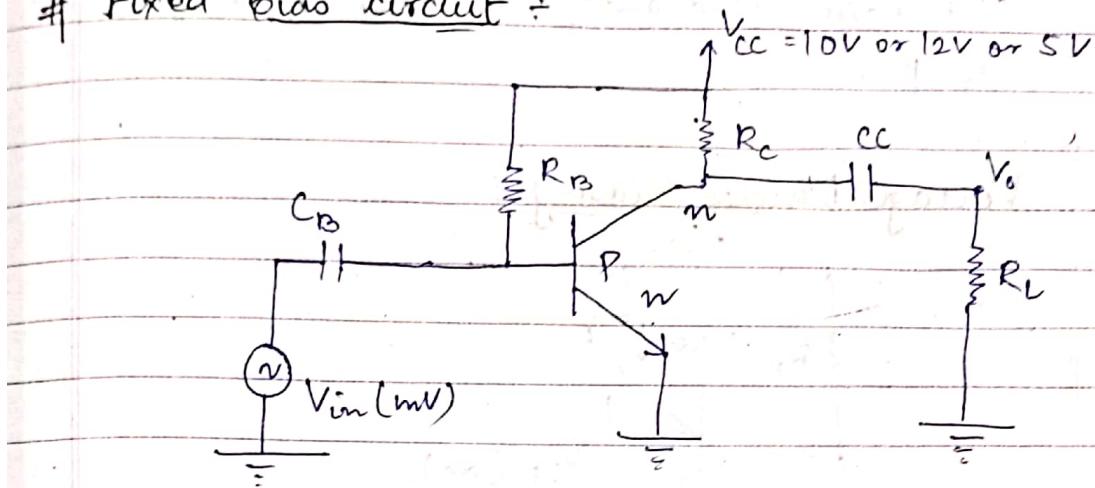


$$I_c = \beta I_B + (\beta + 1) I_{CBO}$$

$$I_c = \beta I_B + (\beta + 1) I_{C0}$$

By raise of the Temp., reverse saturation current I_{C0} will increase, thus I_c will increase and hence there will be heat dissipation in collector region ($I_c^2 R_c$). Because of this heat generation, the transistor gets heated and hence the temp. will increase and I_{C0} will increase, I_c will increase, $I_c^2 R_c$ will increase and this process will accumulate with short span of time, transistor will be burnt out and this process is called thermal runaway.

Fixed Bias circuit :-

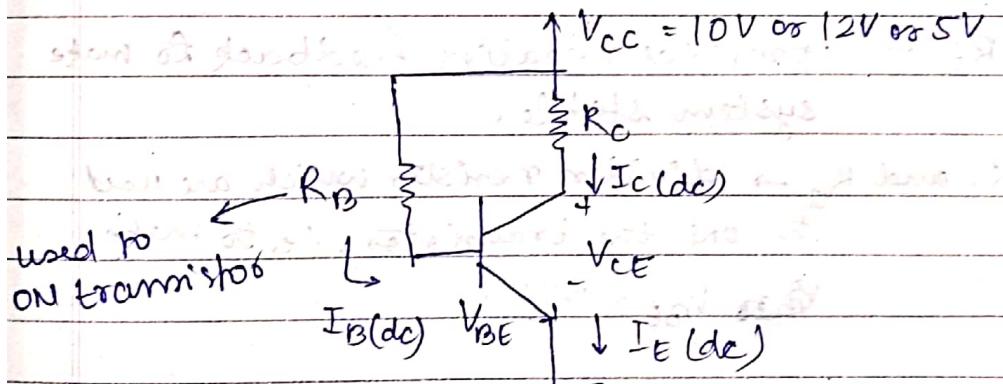


Amplifier with fixed bias circuit

DC analysis -

$$\text{freq} = 0, Z_C = \frac{1}{j\omega C} \quad (\because \omega = 2\pi f = 0)$$

After DC solution $Z_C = \infty$, i.e., Open circuit



Apply KVL in S/P loop :-

$$V_{CC} - I_{B(\text{dc})} R_B = V_{BE} = 0$$

$$\therefore V_{CC} = -I_{E(\text{dc})} R_B = V_{BE} = 0$$

Apply KVL in O/P loop :-

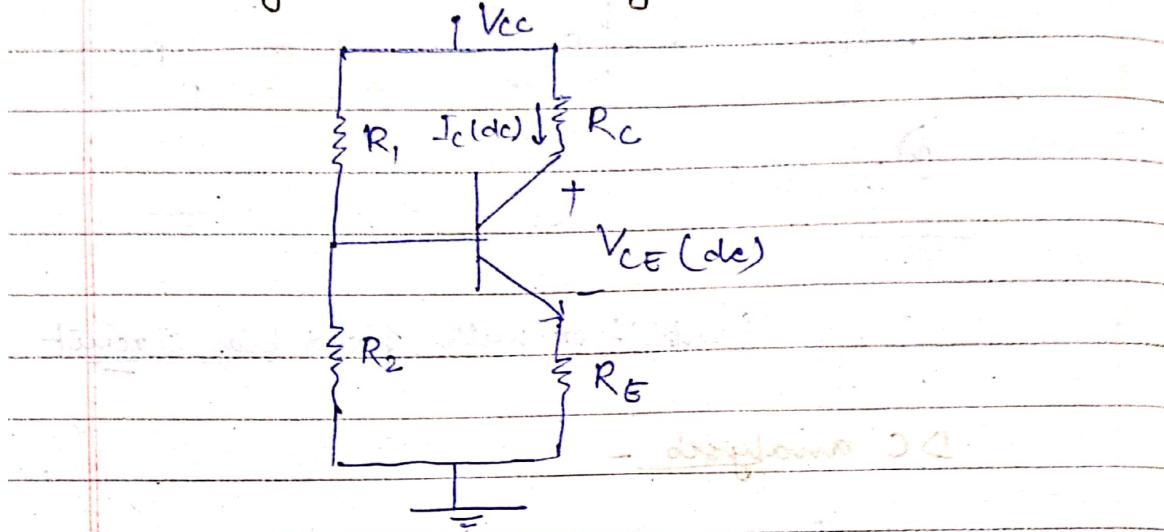
$$V_{CC} - I_{C(\text{dc})} R_C - V_{CE} = 0$$

$$I_{E(\text{dc})} = \frac{V_{CC} - V_{BE}}{R_B} \Rightarrow I_{C(\text{dc})}$$

Date : _____

It's main disadvantage is $I_C(\text{dc})$ is independent of β .

Voltage Divider biasing :

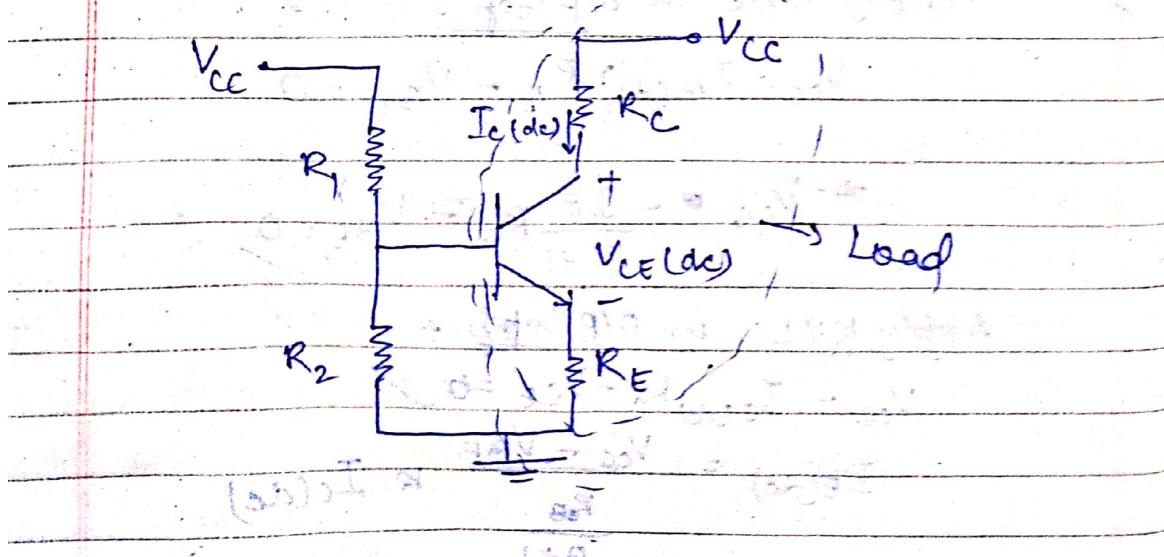


- Function : ~~to operate~~
 $R_E \rightarrow$ to make the transistor in safe mode.

$R_E \rightarrow$ provides negative feedback to make system stable.

R_1 and $R_2 \rightarrow$ divider resistor which are used to set the bias point, i.e. to make $V_{BE} = 0.7V$.

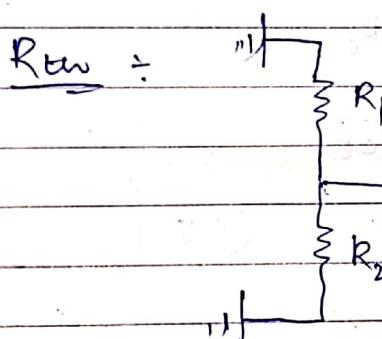
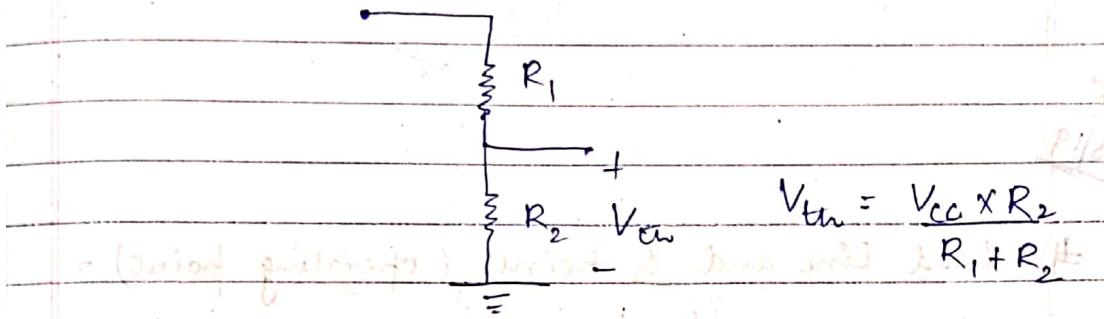
~~R_E in fixed bias circuit is dependent on transistor~~



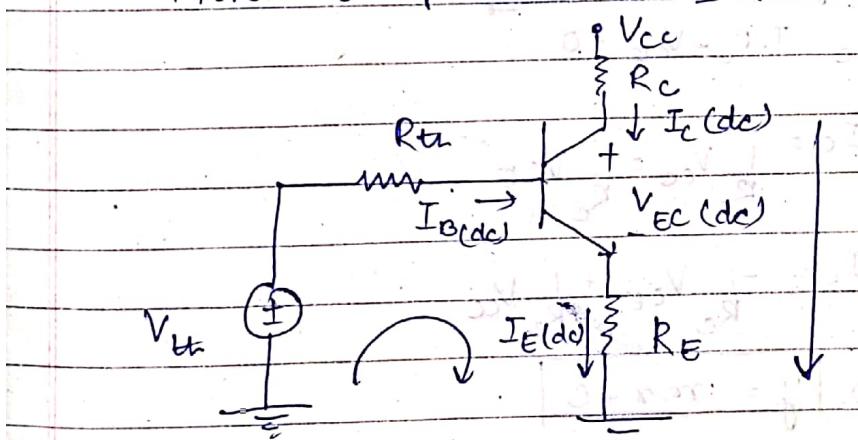
To make Thevenin's equiv. across the load shown -

$$V_{th} =$$

remove load by making open circuit load.



Thevenin's equivalent circuit :-



Applying KVL at O/P :-

$$V_{cc} - I_c(dc) R_C - I_E R_E = 0$$

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

Solving we get :-

$$I_E = \frac{V_{th} - V_{BE}}{R_E + R_{th}} = I_c(dc)$$

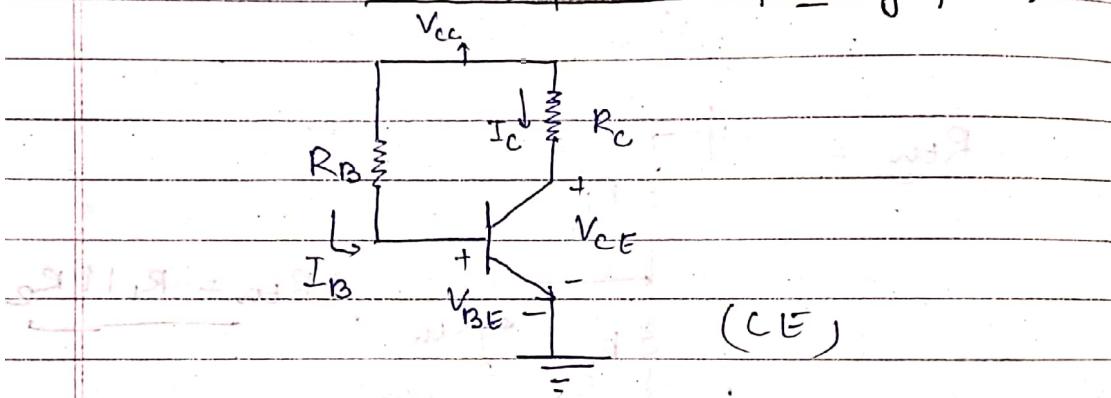
To make $I_C(\text{dc})$ independent of β :

$$R_E \gg R_{\text{th}} \frac{1}{\beta + 1}$$

$$\therefore I_C(\text{dc}) \approx \frac{V_{\text{th}} - V_{\text{BE}}}{R_E}$$

8/19

Load line and Q-point (operating point) :



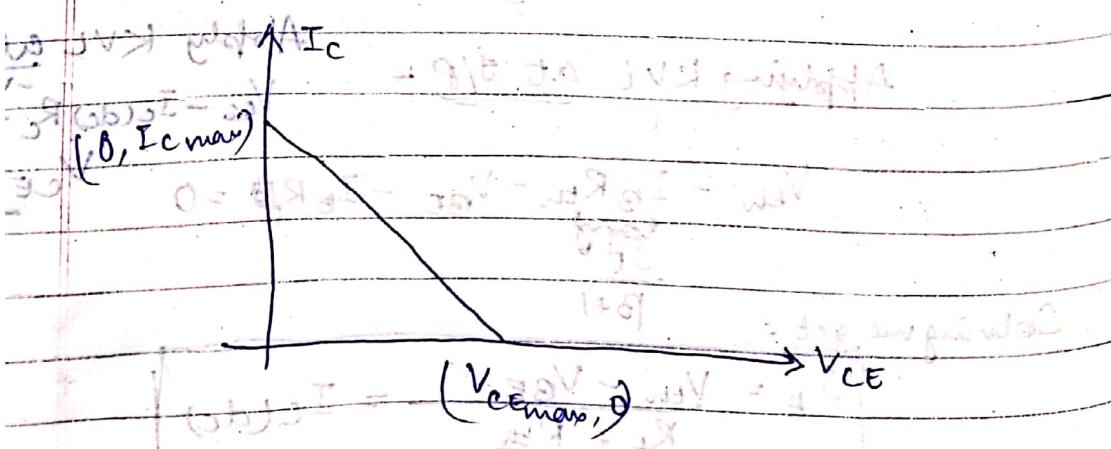
Applying KVL at o/p loop

$$V_{\text{cc}} - I_C R_C - V_{\text{CE}} = 0$$

$$I_C = \frac{1}{R_C} V_{\text{cc}} - \frac{1}{R_C} V_{\text{CE}}$$

$$I_C = -\frac{1}{R_C} V_{\text{CE}} + \frac{1}{R_C} V_{\text{cc}}$$

$$\Rightarrow y = mx + c$$

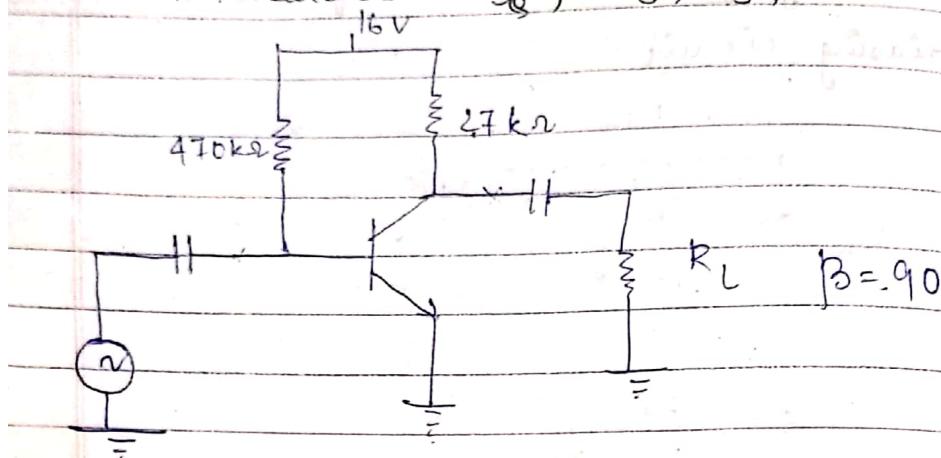


$$V_{CEQ} = V_{CE}(dc)$$

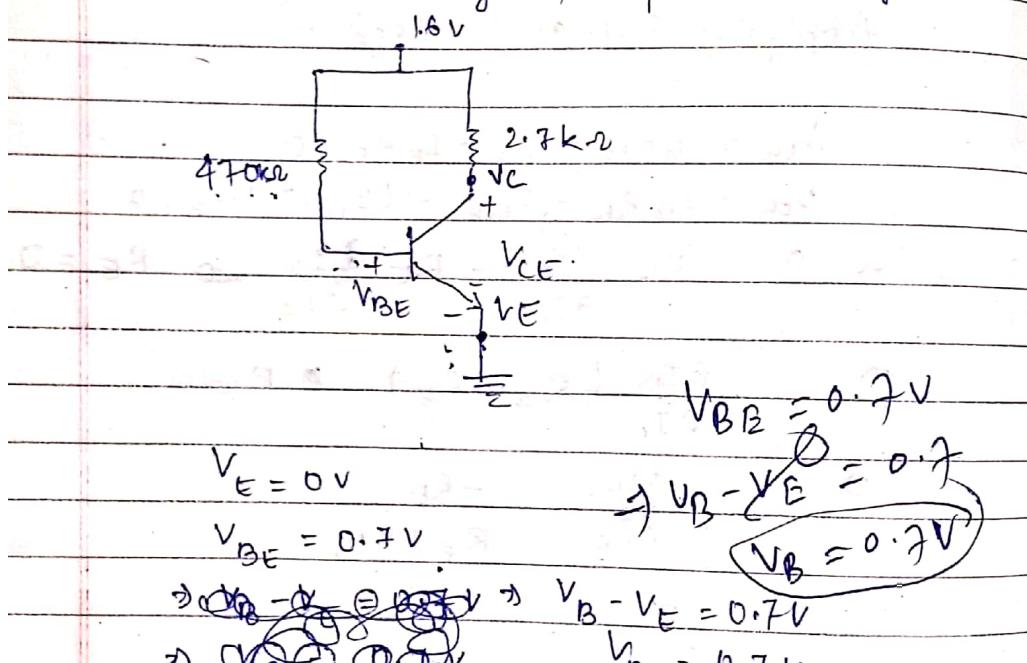
$$I_{CQ} = I_C(dc)$$

Q. For the circuit shown, determine the Q-point, i.e. (V_{CEQ}, I_{CQ})

Also calculate I_{BQ} , & V_C, V_B, V_E



for dc analysis, capacitor is open circuit



$$V_E = 0V$$

$$16 - I_B \cdot 470k - 0.7 = 0$$

$$I_B = \frac{15.3}{470k}$$

$$16 - I_C \cdot 2.7k - V_{CE} = 0$$

$$I_C = \beta I_B$$
$$= 90 \times I_B$$

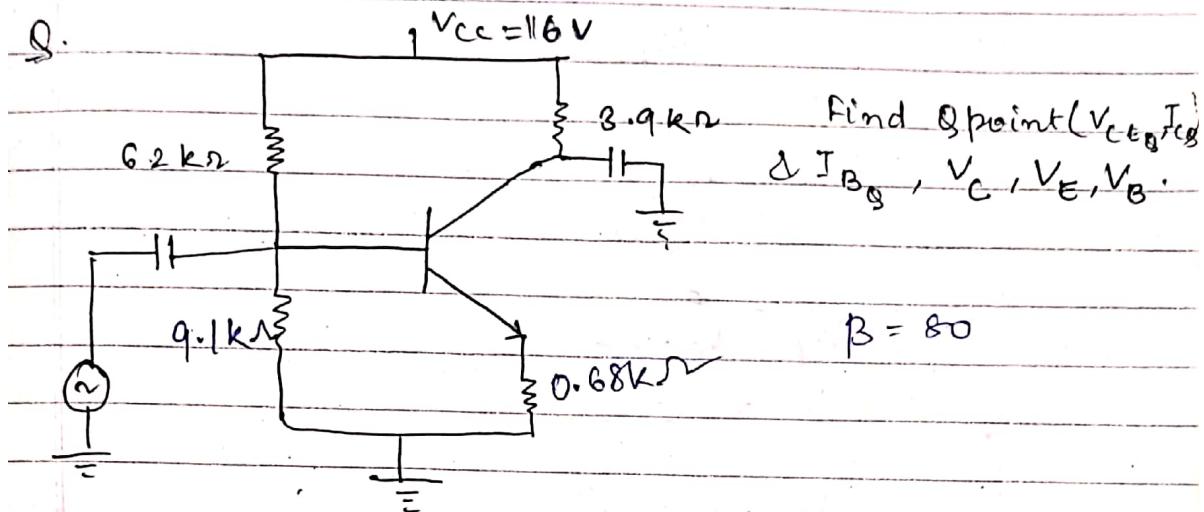
Q. Q-point V_{CEQ} , I_{CQ}

$$V_{CEQ} =$$

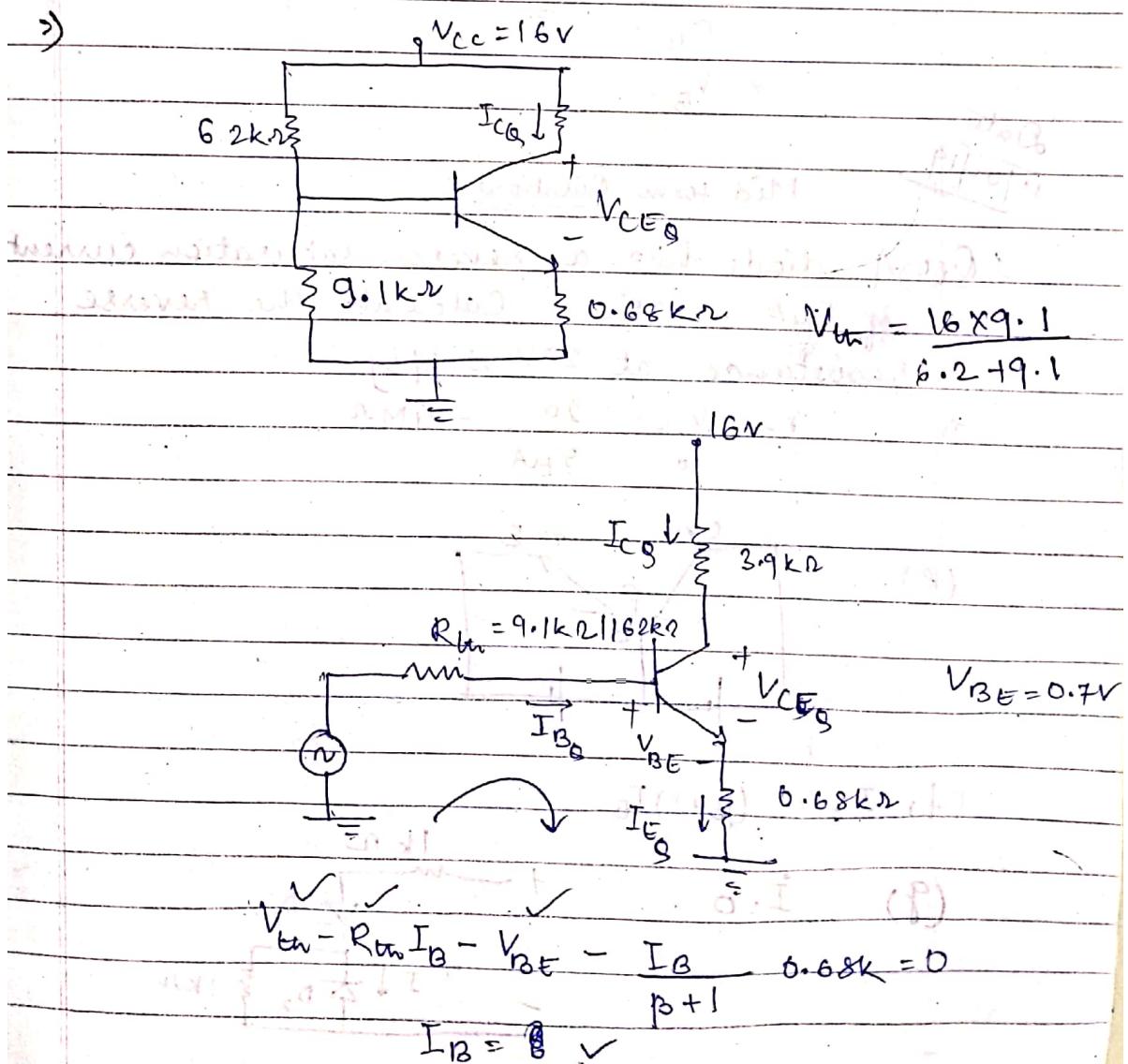
Q-point = (V_{CEQ}, I_{CQ})

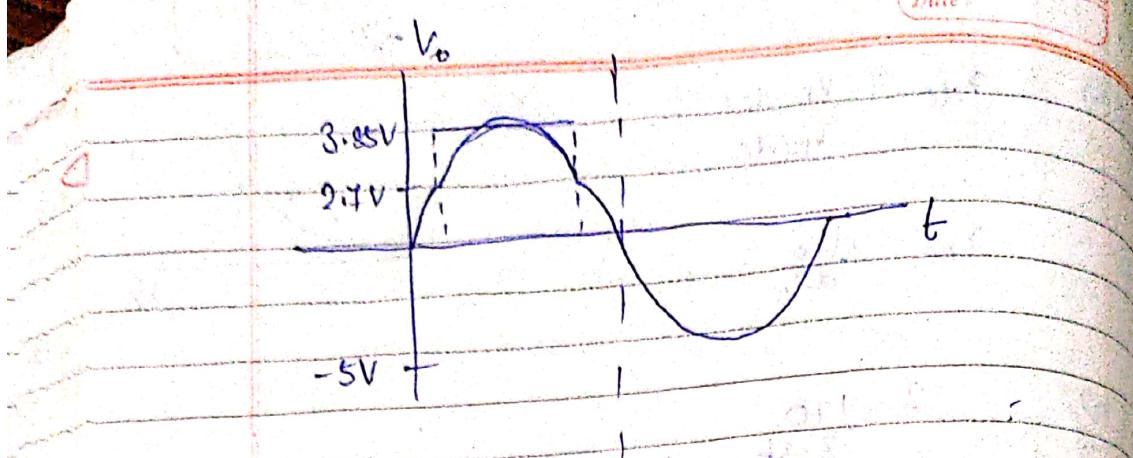
$$V_{CE} = V_C - V_E = V_C$$

Q.



→



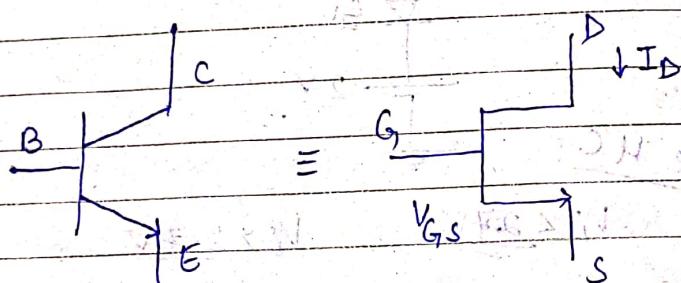


$$5(c) \quad R_{BE} \leq R_2$$

Date
14/10/19

Field Effect Transistor (FET) :-

It is a three terminal device (Gate, Source and Drain) in which output (I_D) current is controlled by S/P voltage (V_{GS}).



Advantages of FET over BJT :-

FET	BJT
i. Voltage controlled current source, i.e., $I_D = f(V_{GS})$ <div style="border: 1px solid black; padding: 2px; display: inline-block;"> $I_D = I_{DSS} (1 - \frac{V_{GS}}{V_P})^2$ </div> $I_D = I_{DSS} [1 - \frac{V_{GS}}{V_P}]^2$	i. Current controlled current source, i.e., $I_C = \beta I_B$ (O/P current controlled by S/P current)
ii. Input impedance of FET is very large compared to BJT (in the range of MΩ).	ii. Input impedance of BJT is smaller than FET (range of Ω or kΩ).

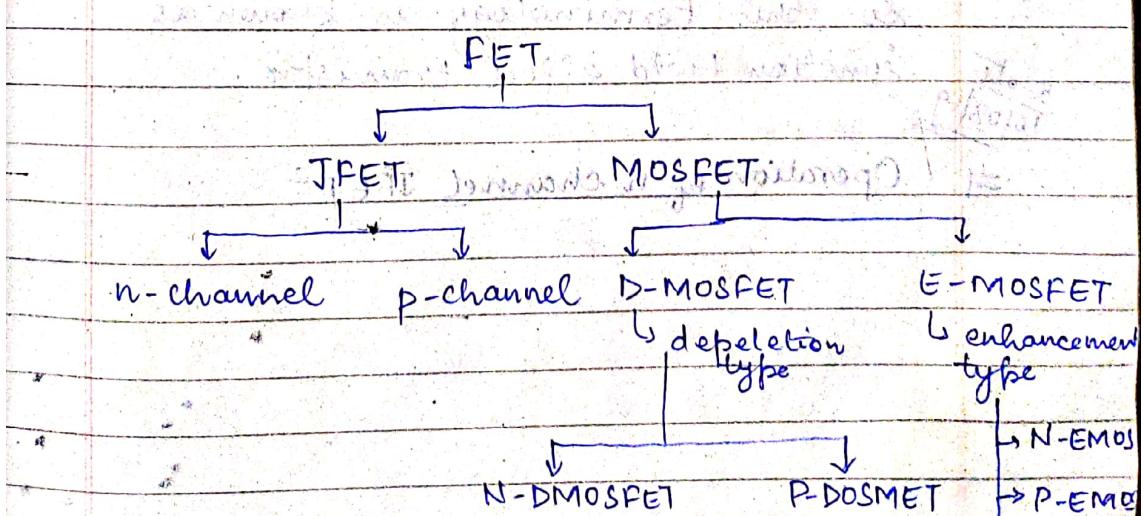
- iii. Output impedance of FET is very small.
 iv. FET is uni-polar device because conduction is due to only the majority carrier which are present in channel.
 v. The output signal is less noisy in FET.
 vi. Good signal chopper passer.
 vii. IC fabrication steps are easy.
- iii. Output impedance of BJT is larger than FET.
 iv. BJT is bipolar device because conduction is due to both majority and minority carrier.
 v. Output signal is noisy.
 vi. Not good signal passer compare to FET.
 vii. IC fabrication steps are complex.

Based on the isolation betⁿ the Gate, and channel, FET is classified into —

↓
 JFET MOSFET

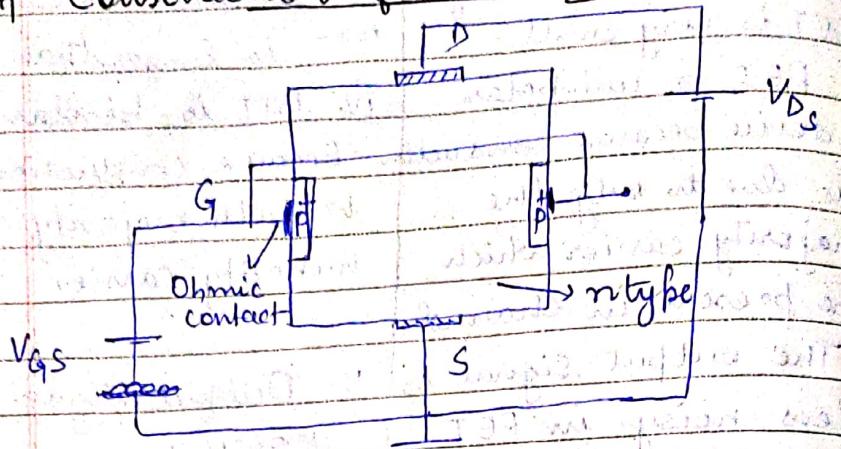
i. JFET = When the isolation betⁿ Gate and channel is done by the p-n junction, that class of FET is known junction field effect transistor.

ii. MOSFET = When the isolation betⁿ Gate and channel is done by SiO_2 , that class of FET is known as MOSFET (metal oxide semiconductor FET).



ohmic contact → used to connect conductor and semi-conductor
Date:

Construction of n-channel JFET :



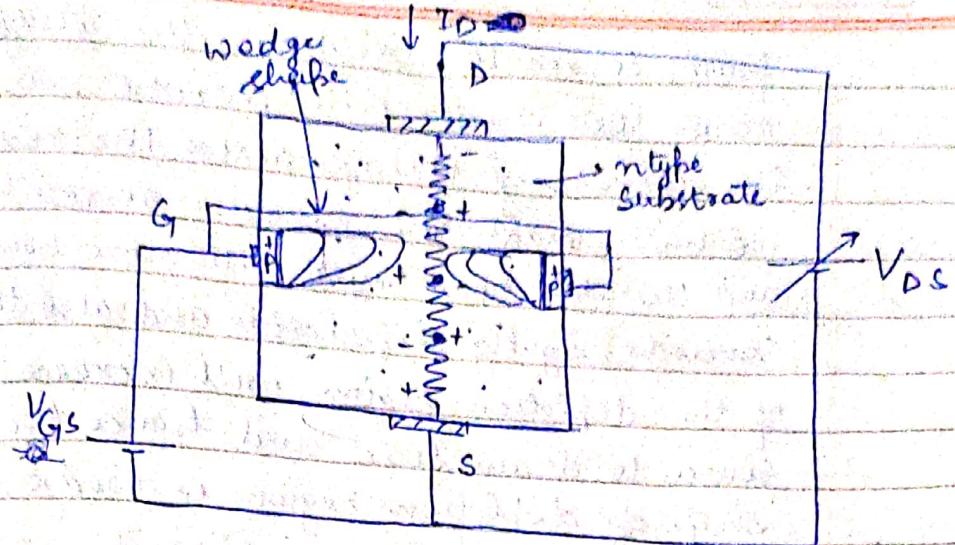
Consider n-type substrate which is lightly doped and heavily doped p-type semi-conductors are embedded on two sides of n type substrate.

On the top of n type substrate, drain terminal is connected through ohmic contact. Similarly, at the bottom n type substrate source is connected through ohmic contact. And gate is connected to p type substrate through ohmic contact. Gate terminals are internally short circuit.

Here, the isolation between channel and gate terminal is done by p-n junction so, this terminology is known as junction field effect transistor.

Date
16/03/19

Operation of n channel JFET :

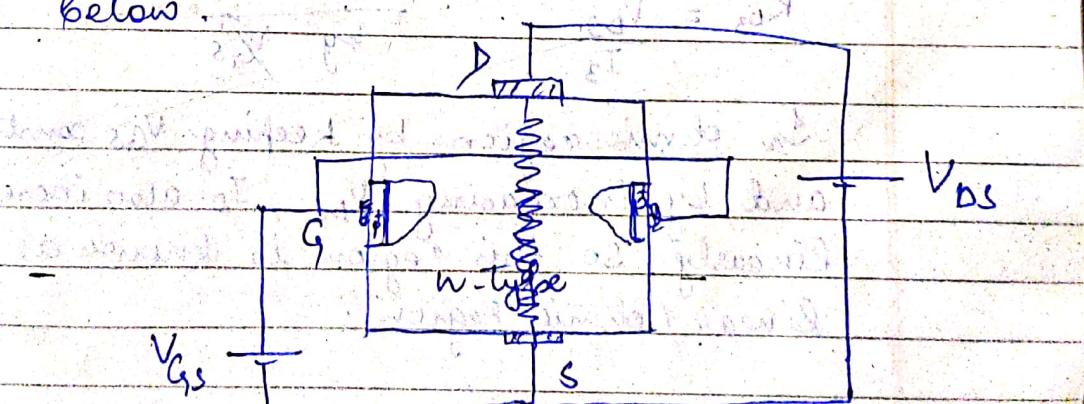


When $V_{GS} = 0V$ and $V_{DS} = 0V$, no current will flow, i.e. $I_D = 0$ amperes.

Keeping $V_{GS} = 0V$ and V_{DS} increasing positively, in the channel the majority carriers electrons will be repel from source terminal and attracted by the drain terminal as a result, the majority carrier electrons will flow from source to drain terminal in channel. So, there will be drain current which will flow from drain to source terminal.

At constant voltage V_{DS} (let $V_{DS} = 1V$), due to this V_{DS} , drain current I_D is flowing through the channel from drain to source.

Now, the entire n-type material where channel is present is behaving as a resistor and applied 1V V_{DS} , ~~wedge~~ will be divided across entire resistor which is shown below.

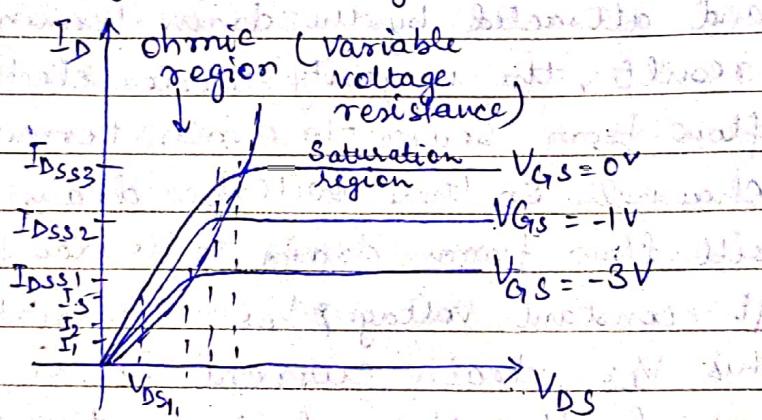


from source towards drain, the voltage drop across the resistor will increase, so by this increasing voltage across the resistor we will make the junction reverse bias and the depletion layer will more penetrate towards lightly doped side and also the shape of the depletion region will increase from source to drain side and hence the shape of depletion region is wedge shaped

Date
18/03/19

O/P VI characteristic (I_D vs JFET)

O/P characteristic curve is the curve between O/P voltage V_{DS} and O/P current I_D by keeping input voltage V_{GS} constant.



$$R_{O1} = \frac{V_{DS1}}{I_1}$$

$$R_{O2} = \frac{V_{DS2}}{I_2}$$

$$R_{O3} = \frac{V_{DS3}}{I_3}$$

$$R_{O1} > R_{O2} > R_{O3}$$

by V_{GS}

In Ohmic region by keeping V_{GS} const. and by increasing V_{DS} , I_D also increases linearly. So, this region is known as linear / ohmic region.

$$V_{GS(\text{off})} \equiv V_{GS} \text{ at which } I_D = 0$$

$$V_P = V_{DS} \text{ at } I_D \text{ becomes const.}$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

Sagar Kumar

• VVR :-

By keeping V_{DS} constant and by varying I/P voltage V_{GS} , output current is changing. So, in linear region there will be variable resistor by varying voltage V_{GS} , so it is called as voltage variable resistor, (Active region).

The region in which I_D current gets saturated or I_D current = const., that region is known as saturation region / active region.

Condition of Pinch-off :-

(2) The O/P voltage V_{DS} at which the I_D current gets saturated ($I_D = I_{DSS} = \text{const.}$) is known as pinch off cond.ⁿ.

or

(1) The value of V_{GS} at which $I_D = 0$ is known as pinch off cond.ⁿ.

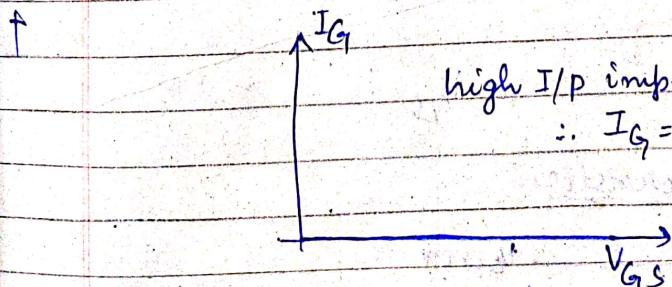
• NOTE :-

The value of V_{GS} at which $I_D = 0$ is known as pinch off voltage (V_P) / V_{GS} cut off voltage.

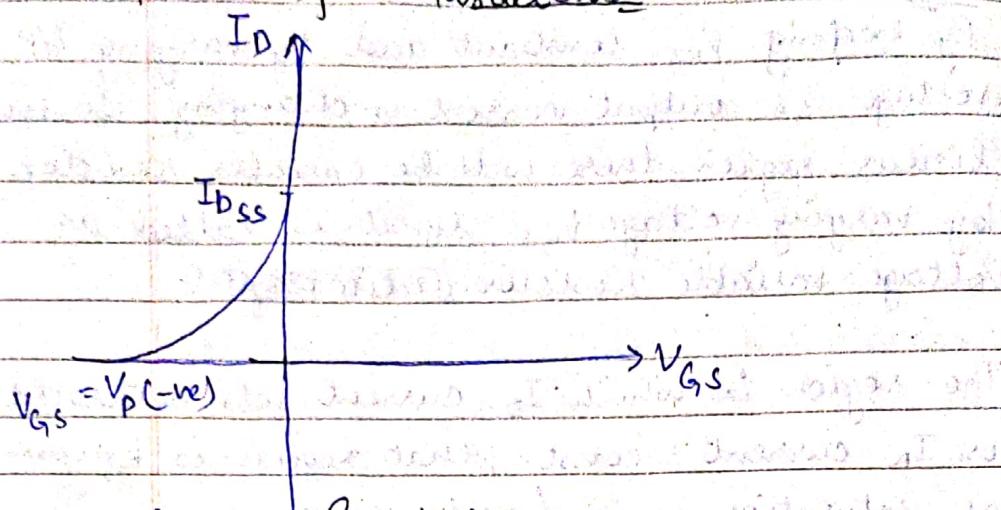
For n-channel JFET, V_P must be negative value.

For p-channel JFET, V_P must be +ve.

S/I characteristic :-



Transfer characteristic:

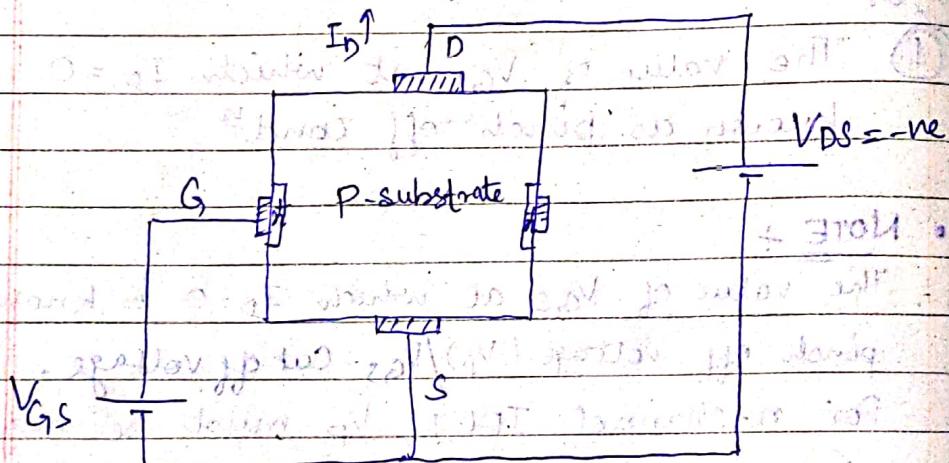
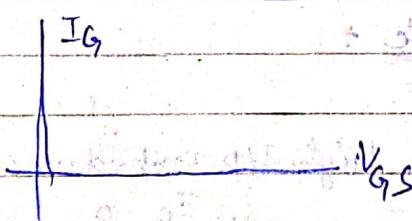
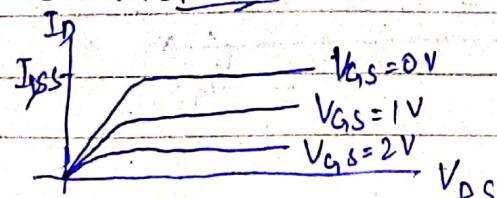


$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

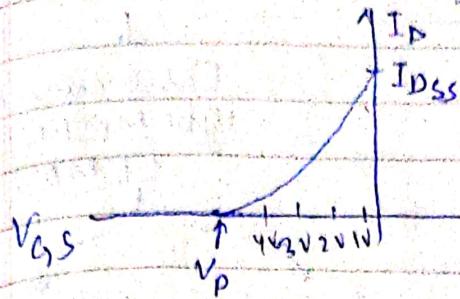
(Working in saturation)

Date
05/03/19

P-channel JFET:

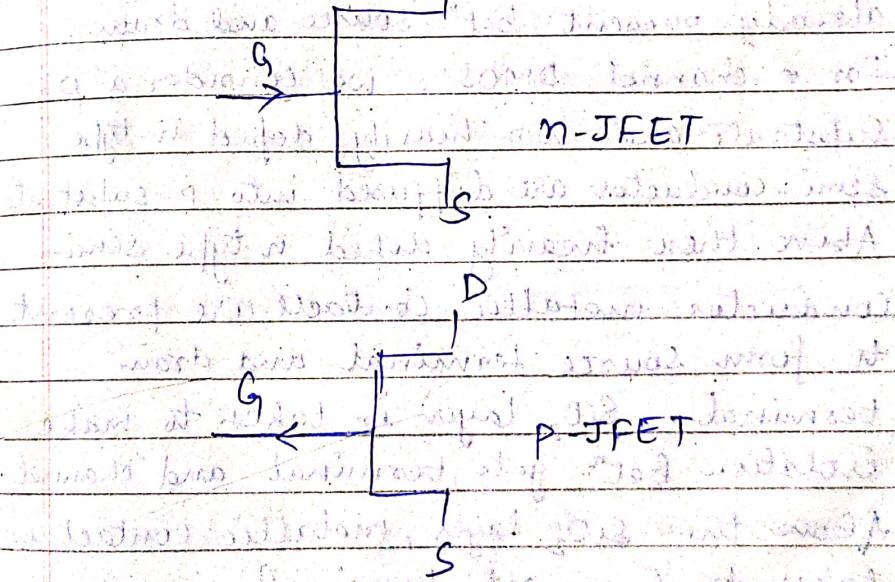
G/P characteristicsO/P characteristics

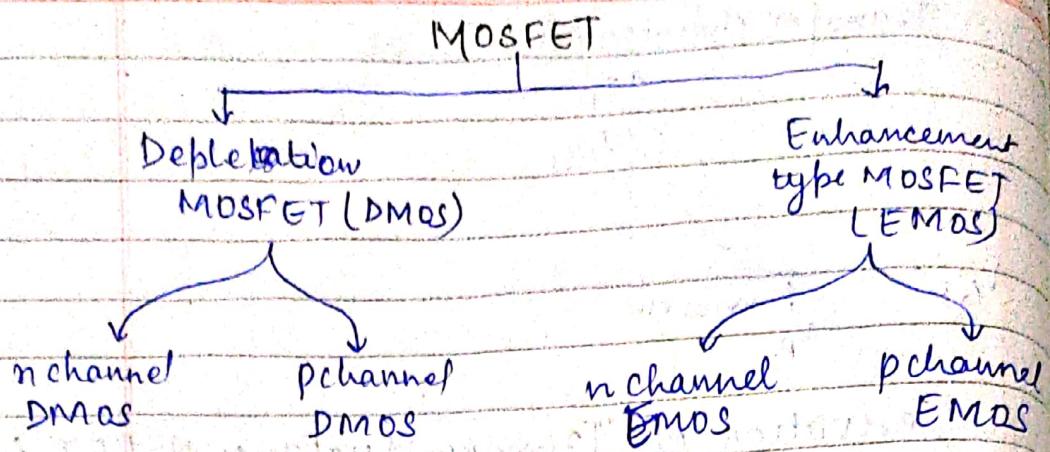
Transfer characteristics



Derivation of Transconductance of FET :

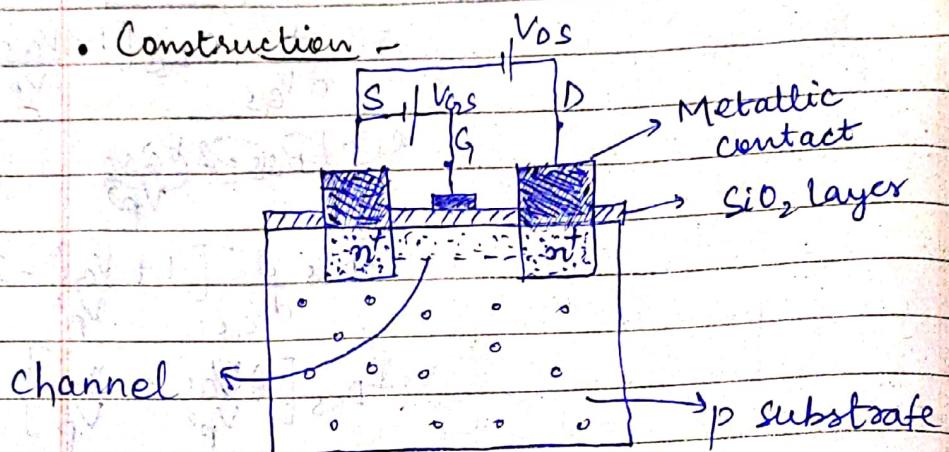
$$\begin{aligned}
 g_m &= \frac{\text{O/P current}}{\text{S/P voltage}} = \frac{dI_D}{dV_{GS}} \\
 &= \frac{d}{dV_{GS}} I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2 \\
 &\quad \cancel{\text{FBSD} \cdot 2 \frac{V_{GS}}{V_p}} \\
 &= I_{DSS} \frac{d}{dV_{GS}} \left[1 + \frac{V_{GS}^2}{V_p^2} - 2 \frac{V_{GS}}{V_p} \right] \\
 &= I_{DSS} \left[\frac{2V_{GS}}{V_p^2} - \frac{2}{V_p} \right] \\
 &= 2I_{DSS} \left[\frac{V_{GS}}{V_p} - 1 \right]
 \end{aligned}$$





n channel DMOS:

• Construction -



In depletion type MOSFET, the channel is already present betⁿ source and drain.

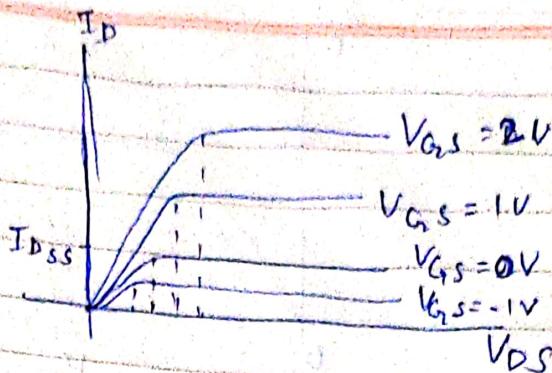
For n-channel DMOS, we consider a p-substrate and two heavily doped n-type semi-conductors are diffused into p-substrate. Above these heavily doped n-type semi-conductors metallic contacts are present to form source terminal and drain terminal. SiO₂ layer is taken to make isolation betⁿ gate terminal and channel.

Above the SiO₂ layer, metallic contact is taken to form gate terminal.

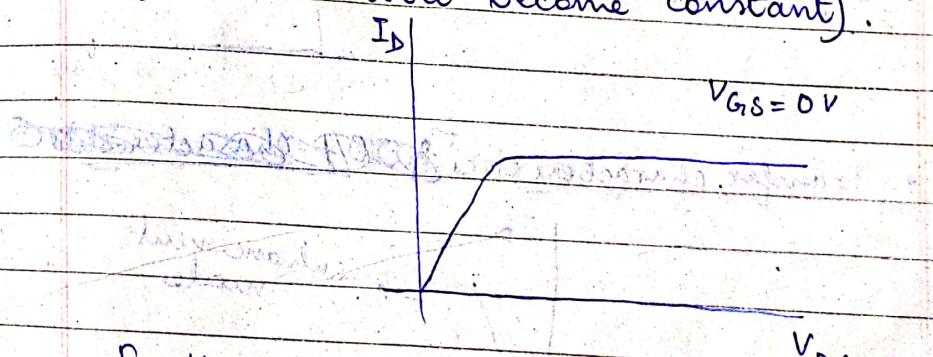
In channel, less no. of e⁻ present because they are minority carriers in p-substrate.

Operation :

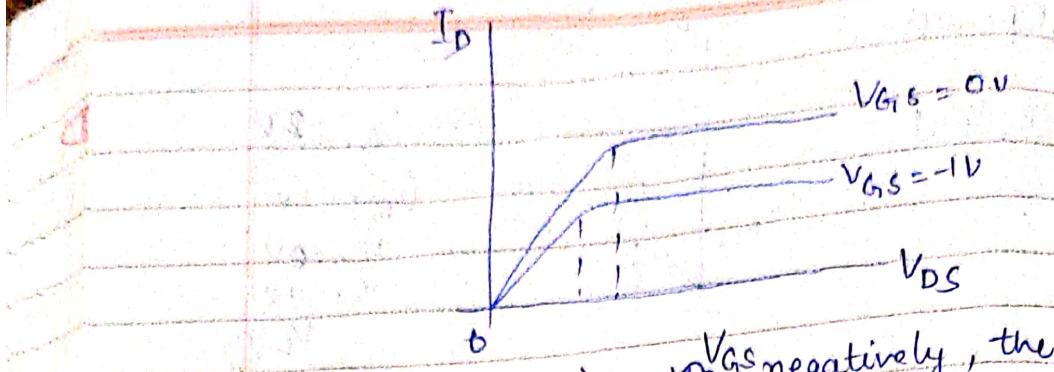
$$V_g = 0V, V_{DS} \uparrow$$



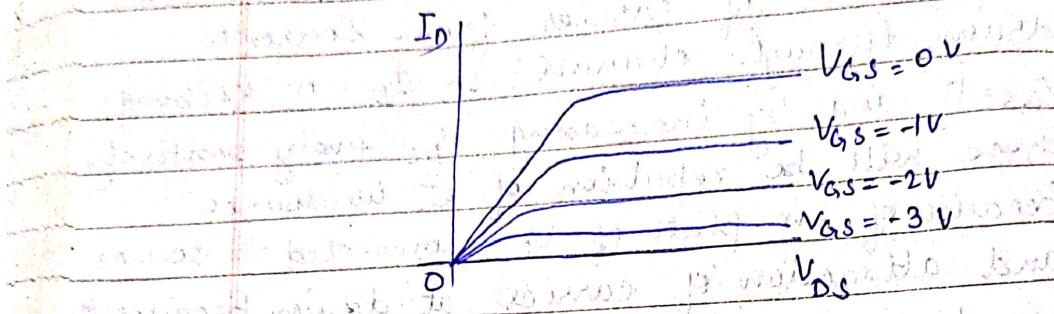
Considering $V_{GS} = 0V$ and $V_{DS} = 0V$, there will be no movement of carrier from source to drain through channel so $I_D = 0$. Keeping $V_{GS} = 0$ and by increasing V_{DS} ~~positively~~ positively there will be repulsion of e^- in source because of -ve plate of V_{DS} connected to source and attraction of carrier at drain because of +ve plate of V_{DS} connected to drain as a result there will be movement of the carrier from source to drain. Hence, there will be some I_D current. Further, increasing V_{DS} more no. of carriers will flow from source to drain through channel as a result I_D current increases. Further increasing V_{DS} , I_D current will not increase because channel is full. Hence, there will be pinch-off condition (I_D current will become constant).



Further taking $V_{GS} = -1V$ and keep on increasing V_{DS} , pinch-off will occur early compared to $V_{GS} = 0V$. Hence, characteristics curve will be -

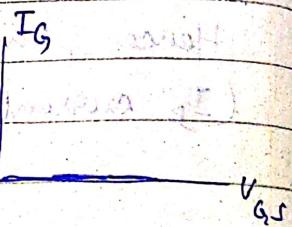


further increasing V_{GS} negatively, the VI characteristics curve will be -

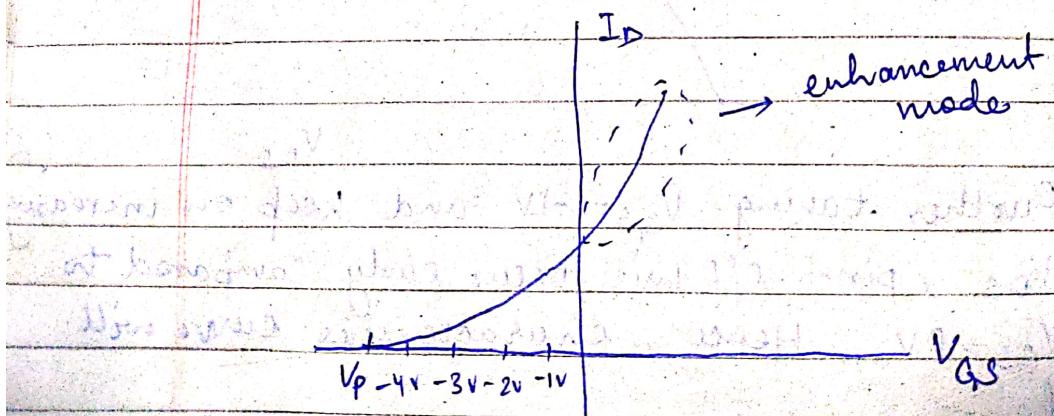


If we increase V_{GS} positively ($V_{GS} = 1V$) a large no. of carriers will pass through the channel and, hence I_D current will enhance and this mode of operation of depletion type n-channel MOSFET is called as enhancement mode.

- Input characteristics =



- Transfer characteristic



$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

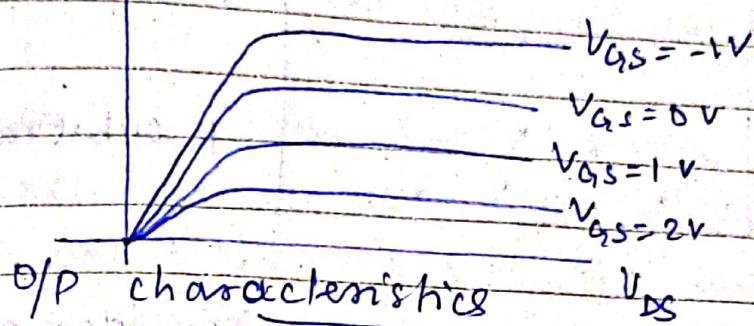
NOTE

for nchannel DMOS -

$$V_P = -ve$$

P-channel DMOS :-

I_D



O/P characteristics

V_{DS}

$V_{GS} = -1V$

$V_{GS} = 0V$

$V_{GS} = 1V$

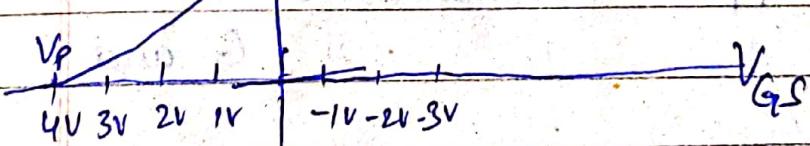
$V_{GS} = 2V$

I_G (Input characteristics)

S/I characteristics

I_D

enhancement mode



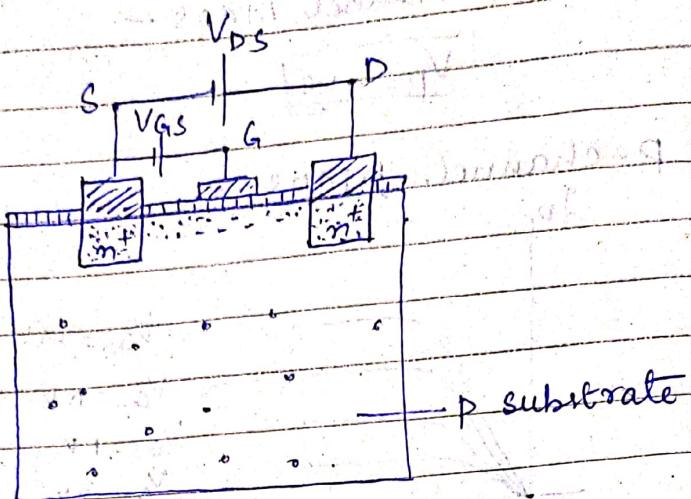
Transfer characteristics

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n channel enhancement type MOSFET

In case of enhancement type MOSFET, initially there is no channel between source and drain.



For n-channel EMOSFET, consider a p-type substrate and two heavily doped n-type semi-conductors are diffused on two sides of p-substrate and above the heavily doped n-type semi-conductor metallic contacts are used to form the source and drain terminal.

To make the isolation b/w gate and channel, SiO_2 layer is used and above it a metallic contact is used to cover the gate terminal.

V_{DS} is applied potential betw D and S

V_{GS} " " " " " G and S.

• Operation and VI characteristics :-

Initially, there is no channel so $I_D = 0$.

To establish the channel, we have to increase the V_{GS} positively. As a result, holes in p substrate below the gate region will be repelled and minority carriers electrons in p-substrate will be

attracted towards the gate terminal. As a result, there will be only e^- available underneath gate terminal forming channel. Value of V_{GS} at which the channel established between source and drain is called as threshold voltage, (V_{th})

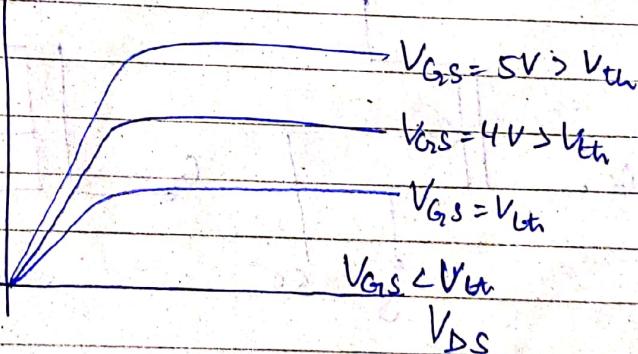
NOTE:

for n channel MOS, threshold voltage is +ve and corresponding p channel, V_{th} is -ve.

Once $V_{GS} > V_{th}$, i.e., channel established if we increase V_{DS} , the e^- in source will be repelled by negative terminal of V_{DS} and e^- in drain will be attracted by positive terminal of V_{DS} . As a result, e^- will flow from source to drain and hence there will be I_D current.

By increasing V_{DS} (keeping V_{GS} constant greater than V_{th}), I_D current increases linearly and further increasing V_{DS} , I_D current becomes constant.

O/P charac. = I_D



S/I P-char

Transfer char:

 I_D

$$\rightarrow I_D = k(V_{GS} - V_{th})^2$$

V_{GS} > V_{th}

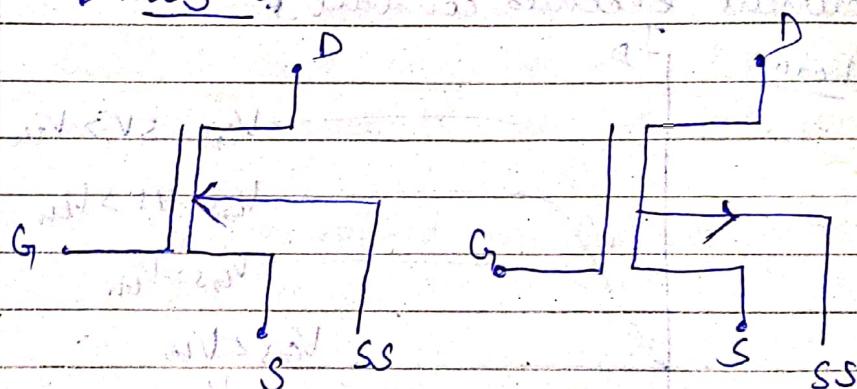
NOTE: here Shockley's eqⁿ is not satisfied for

the characteristic curve. So, new eqⁿ-

$$\boxed{I_D = k(V_{GS} - V_{th})^2}$$

(Schematic diagram):

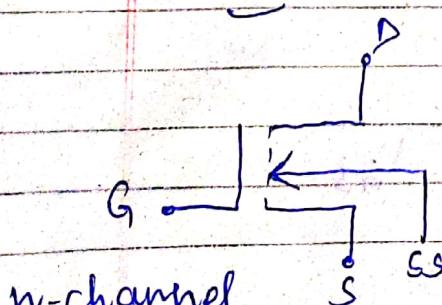
D MOS:



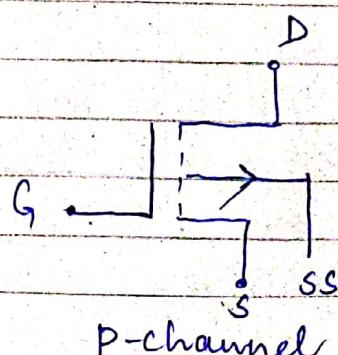
n-channel

p-channel

EMOS:



n-channel



p-channel

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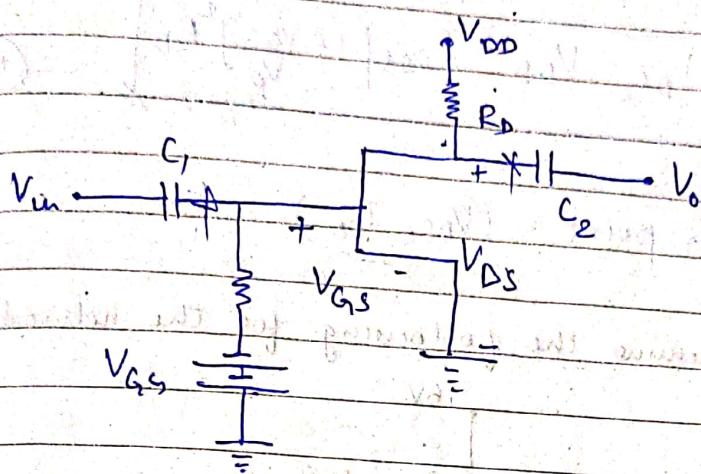
$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$I_D = k(V_{GS} - V_{th})^2$$

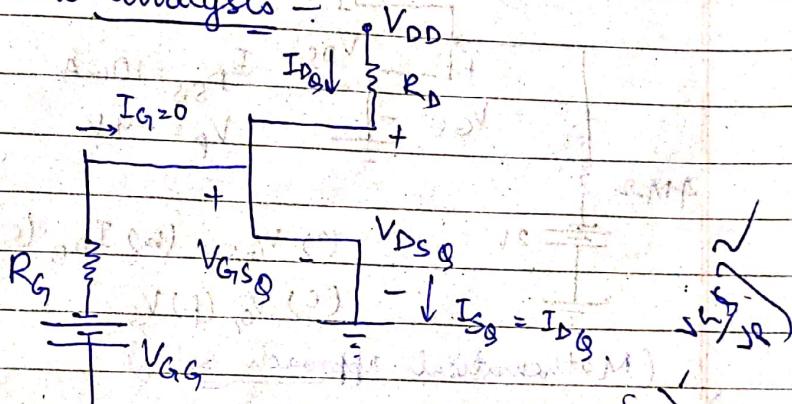
FET Biasing :-

Biasing is required for faithful amplification.
In case of FET, ~~as~~ as input impedance is very high, S/P current I_G is always zero.
As FET is uni-polar device $I_D = I_S$ ($I_G = 0$).

• Fixed bias :-



for dc analysis :-



applying KVL in S/P :-

$$-V_{GG} - V_{GSQ} = 0$$

$$V_{GSQ} = -V_{GG}$$

(1)

applying KVL at O/P :-

$$V_{DD} - I_{DSQ} R_D - V_{DSQ} = 0$$

(2)

$$V_{DSQ} = I_{DSQ} R_D$$

Applying Schokley's eqⁿ:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

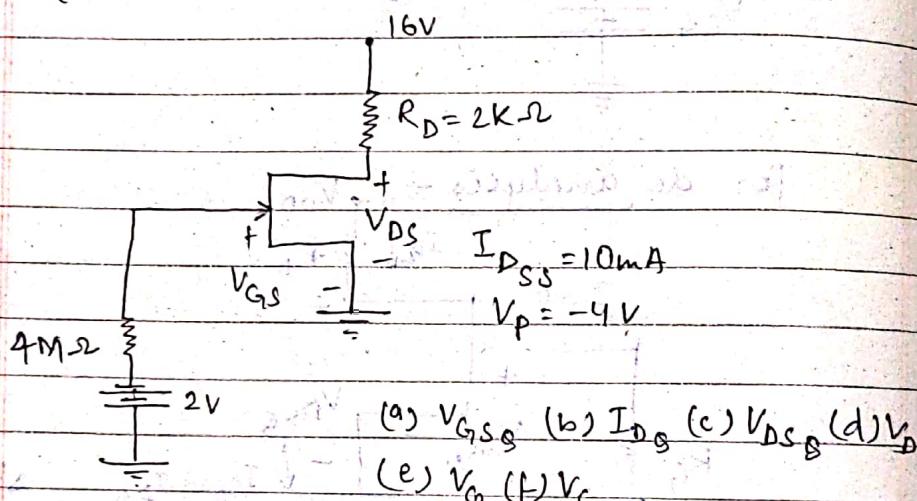
$$= I_{DSS} \left[1 + \frac{V_{GS}}{V_P} \right]^2 \quad \text{--- (3)}$$

putting I_D in eqⁿ (2) :

$$\boxed{V_{DSQ} = V_{DD} - I_{DSS} \left[1 + \frac{V_{GS}}{V_P} \right]^2 R_D} \quad \text{--- (4)}$$

Q point = (V_{DSQ}, I_{DQ}) .

Q. Determine the following for the network.



(Mathematical approach solⁿ)

$$\Rightarrow -2\text{V} - V_{GS} = 0$$

$$V_{GS} = -2\text{V}$$

$$I_{DQ} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$= 10\text{m} \left[1 + \frac{2}{-4} \right]^2$$

$$= 10\text{m} \left[1 - \frac{1}{2} \right]^2$$

$$= 10\text{m} \times \frac{1}{4} = 2.5\text{mA}$$

$$16 - 2.5m \times 2k - V_{DSQ} = 0$$

$$V_{DSQ} = 16 - 5$$

$$= 11V$$

$$V_{DS} = 11V$$

$$V_D - V_S = 11V$$

$$V_D = 11V$$

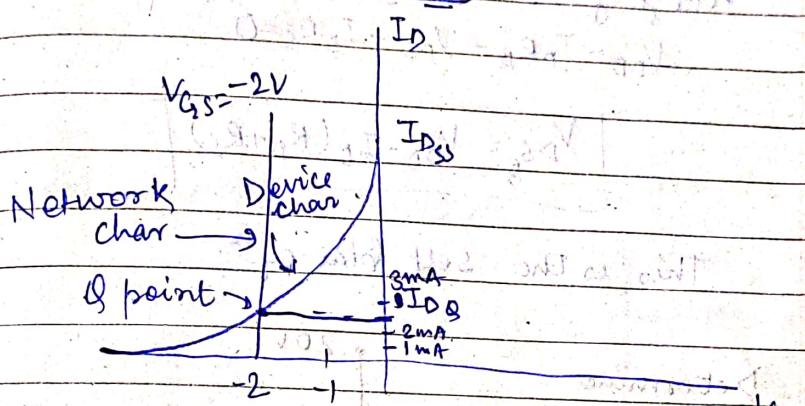
$$V_{GS} = -2V$$

$$V_G - V_S = -2V$$

$$V_G = -2V$$

$$V_S = 0V$$

(Graphical approach soln)



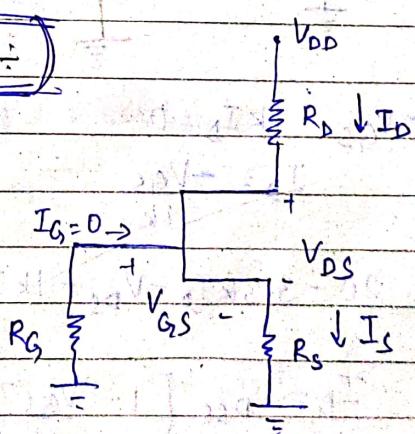
$$I_{DQ} = 2.5mA \text{ (from graph)}$$

Applying KVL at Q/P

$$\boxed{V_{GS} = -2V}$$

$$16 - I_D R_D - V_{DS} = 0.$$

Self biasing



Applying KVL at S/P \therefore

$$V_{DD} - I_D R_D - V_{GS} - I_D R_S = 0$$

$$V_{GS} = -I_D R_S$$

By Schotcky's eqⁿ:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\Rightarrow I_D = I_{DSS} \left[1 + \frac{I_D R_S}{V_P} \right]^2$$

Solving:

$$I_D = I_{D_1} \text{ and } I_D = I_{D_2}$$

Applying KVL at O/P \therefore

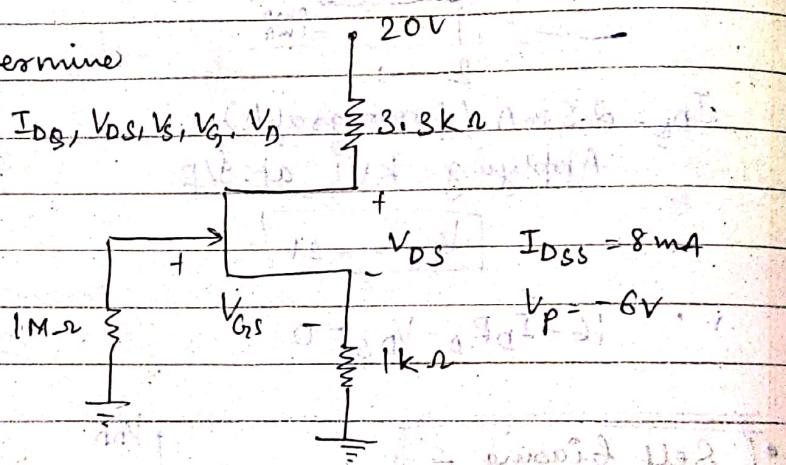
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

This is the self bias eqⁿ.

Q. Determine

$$V_{GS}, I_{Dg}, V_{DS}, V_S, V_D$$



$$\therefore -V_{GS} - 1k I_D = 0$$

$$I_D = -\frac{V_{GS}}{1k}$$

$$20 - 3.3k I_D - V_{DS} - 1k I_D = 0$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$-\frac{V_{GS}}{1k} = 8m \left[1 + \frac{V_{GS}}{6} \right]^2$$

$$\Rightarrow -V_{GS} = 8 \left[1 + \frac{V_{GS}}{6} \right]^2$$

$$\Rightarrow -V_{GS} = 8 \left[1 + \frac{V_{GS}^2}{36} + \frac{V_{GS}}{3} \right]$$

$$\Rightarrow -V_{GS} = 8 + \frac{V_{GS}^2}{36} + \frac{8V_{GS}}{3}$$

$$\Rightarrow \frac{28V_{GS}^2}{9} + \frac{14V_{GS}}{3} + 8 = 0$$

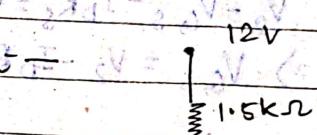
$$\Rightarrow 12V_{GS}^2 + 72V_{GS} + 72 = 0$$

$$\Rightarrow V_{GS} = -6V$$

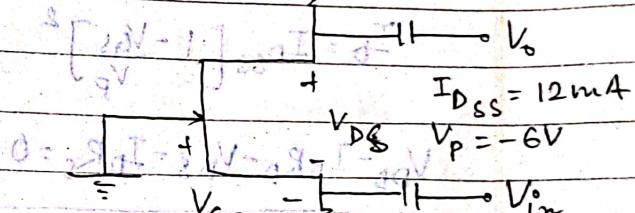
$$I_D = 2.6mA, 13.9mA$$

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Q. Determine the Q-point



\Rightarrow



$$12 - 1.5k I_D - V_{DS} - 680I_D^2 = 0 \quad (1)$$

$$-V_{GS} - 680I_D = 0 \quad (2)$$

$$V_{GS} = -680I_D$$

Also, using Schotckley's eqⁿ -

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$= 12m \left[1 + \frac{V_{GS}}{6} \right]^2$$

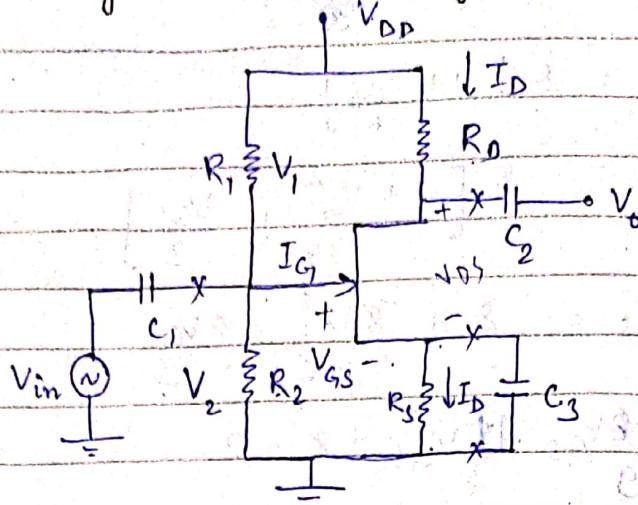
$$= 12m \left[1 - \frac{680I_D}{6} \right]^2$$

$$\therefore I_D = 3.83mA \text{ and } I_{D2} = 20mA$$

$$V_{DSn} = \underline{\underline{V}}$$

$$V_{DSn} = \underline{\underline{V}}$$

Voltage divider biasing



for dc analysis, capacitor will be open
here $I_G = 0$, so R_1 and R_2 are in series

$$\therefore V_2 = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_2 - V_{GS} - I_D R_S = 0$$

$$\Rightarrow V_{GS} = V_2 - I_D R_S$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

(Ansxt)

i. Determine the following

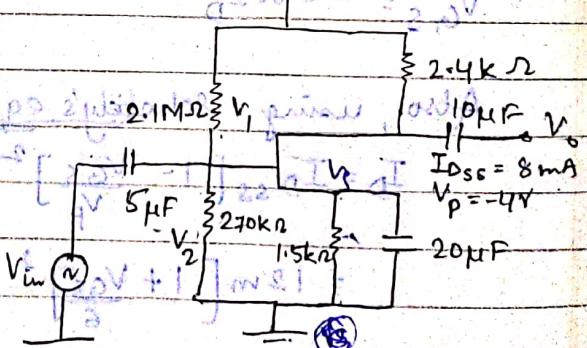
i. I_{DQ}, V_{GSQ}

ii. V_D

iii. V_S

iv. V_{GS}

v. V_{DG}



$$V_2 = \frac{16 \times 270k}{2.1M + 270k} = 1.82V$$

$$\begin{aligned} V_2 - V_{GS} - 1.5kI_D &= 0 \\ \Rightarrow 1.82 - V_{GS} - 1.5kI_D &= 0 \\ \Rightarrow V_{GS} &= 1.82 - 1.5kI_D \end{aligned}$$

$$I_D = I_{Dss} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

$$\Rightarrow I_D = 8m \left[1 + \frac{V_{GS}}{4} \right]^2$$

$$\Rightarrow I_D = 8m \left[1 + \frac{(1.82 - 1.5kI_D)^2}{16} + \frac{(1.82 - 1.5kI_D)}{2} \right]$$

$$I_D = 2.4mA$$

$$V_{GS} = 1.82 - 1.5kI_D$$

$$= 1.82 - 3.6$$

$$= 1.78V$$

$$\frac{V_S - 0}{1.5k} = I_D$$

$$\Rightarrow V_S = 3.6V$$

$$V_{GS} = V_G - V_S$$

$$\Rightarrow -1.78 = V_G - V_S$$

$$\Rightarrow V_G = 3.6 - 1.78 = 1.82$$

$$V_{DS} = V_D - V_S$$

$$\frac{16 - V_D}{2.4k} = \frac{2.4mA}{3.6} \Rightarrow V_D = 6.64V$$

$$\Rightarrow V_D = 16 - 5.76$$

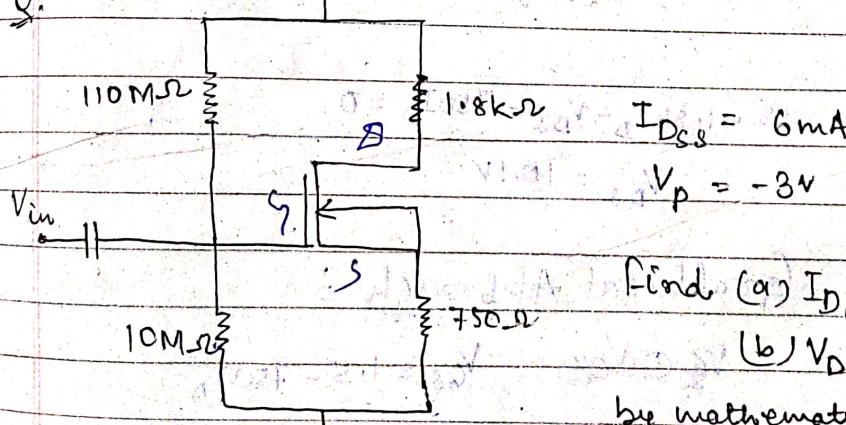
$$V_D = 10.24V$$

$$V_{DG} = V_D - V_G$$

$$= 10.24 - 1.82$$

$$= 8.42V$$

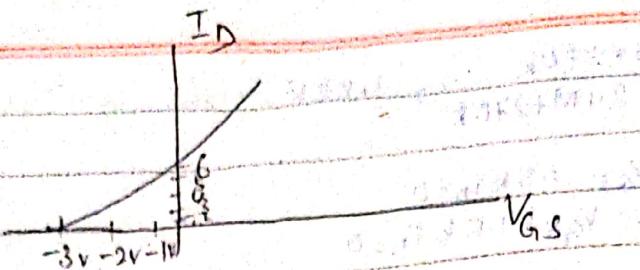
Q.



Find (a) I_{Dg}, V_{GSg}

(b) V_{DS}

by mathematical as well
as graphical approach.



⇒ Mathematical Approach -

$$V_2 = \frac{18 \times 10^3}{120 \mu\text{A}}$$

$$= \frac{3}{2} = 1.5 \text{ V}$$

$$V_2 - V_{GS} - 750 I_D = 0$$

$$V_{GS} = 1.5 - 750 I_D$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

$$= 6 \text{ mA} \left[1 + \frac{1.5 - 750 I_D}{3} \right]^2$$

$$= 6 \text{ mA} \left[1 + (1.5 - 750 I_D)^2 \right] \frac{2}{3} (1.5 - 750 I_D)$$

$$= 6 \text{ mA} \left[\frac{1}{3} (4.5 - 750 I_D)^2 \right]$$

$$= \frac{6 \text{ mA}}{9} \times [4.5^2 + (750 I_D)^2 - 2 \times 4.5 \times 750 I_D]$$

$$I_D = 3.1 \text{ mA}$$

$$V_{GS} = 1.5 - 750 \times 3.1 \text{ mA}$$

$$= -0.8 \text{ V}$$

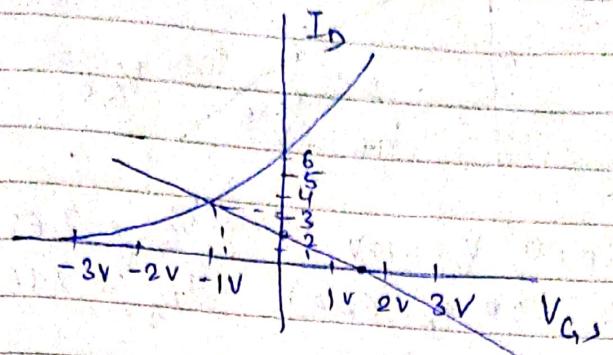
$$18 - 1.8k I_D - V_{DS} - 750 I_D = 0$$

$$V_{DS} = 10.1 \text{ V}$$

Graphical Approach :-

$$V_{GS} = 1.5 - 750 I_D$$

when $I_D = 0$, $V_{DS} = 1.5V$ (1.5, 0)
 when $V_{GS} = 0$, $I_D = 2mA$ (0, 2)



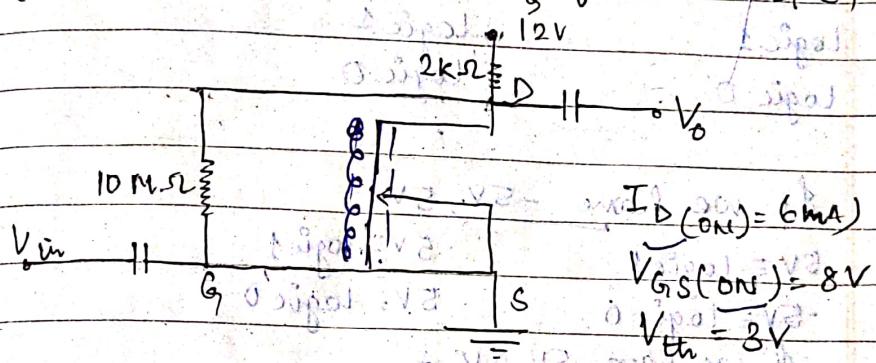
$$I_{Dg} = 3.1 \text{ mA} \quad (\text{from graph})$$

$$V_{G_{Sg}} = 0.8V \quad (1)$$

$$18 - 1.8k I_D - V_{DS} - 750 I_D = 0 \quad (\text{given})$$

$$V_{DS} = 10.1V$$

Q. Determine the I_{Dg} , V_{DSg} for E-MOSFET —



$$\Rightarrow V_S = 0V$$

$$12 - 2k I_D - V_{GS} = 0 \quad (\text{given})$$

at drain voltage 12V, current is zero at drain

$$\text{drain current } I_D = k(V_{GS} - V_{th})^2 \quad 0 \text{ Amp}$$

current zero at drain voltage 12V, current is zero at drain

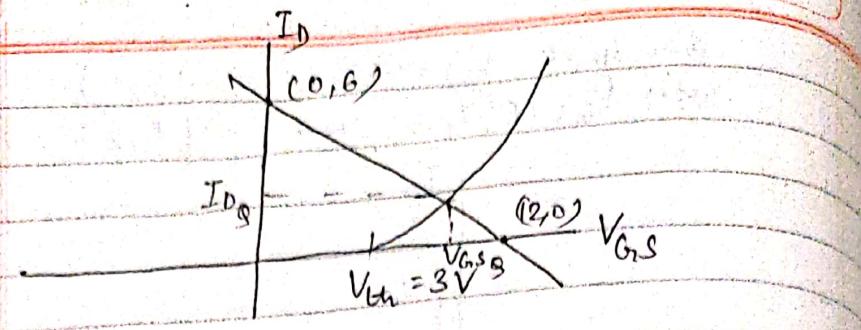
$$k = \frac{I_{D(\text{ON})}}{(V_{GS(\text{ON})} - V_{th})^2}$$

$$= 0.24 \times 10^{-3} \text{ A/V}^2$$

$$\therefore I_D = 0.24 \times 10^{-3} [12 - 2k I_D + 3]^2$$

$$I_D = 2.16 \text{ mA}$$

$$V_{DS} = 12 - 4.32$$

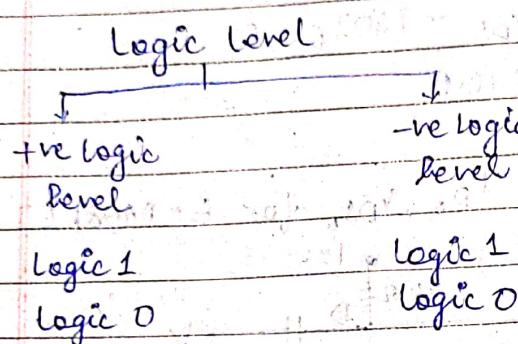


$$\Rightarrow I_D = 0, V_{GS} = 12V \quad V_{GSQ} = 7.68V \quad \{ \text{from graph} \}$$

$$V_{GS} = 0V, I_D = 6mA \quad I_{DQ} = 2.16mA \quad \{ \text{from graph} \}$$

Date
05/04/19

CMOS : (Complementary MOS)



If we have $-5V, 5V$

$5V \equiv \text{Logic 1}$ $-5V \equiv \text{Logic 1}$

$-5V \equiv \text{Logic 0}$ $5V \equiv \text{Logic 0}$

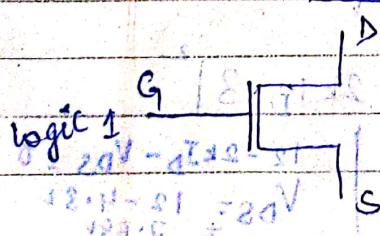
If we have $5V, 2V$

$5V \equiv \text{Logic 1}$ $2V \equiv \text{Logic 1}$

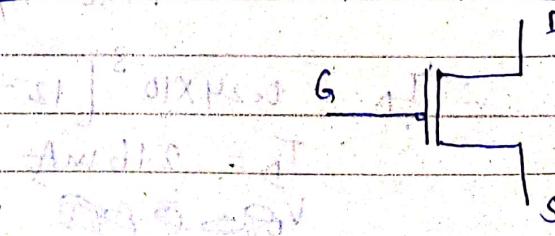
$2V \equiv \text{Logic 0}$ $5V \equiv \text{Logic 0}$

In positive logic level, the higher voltage level is logic 1 and lower voltage level is logic 0 and in case of a negative logic level, higher voltage is logic 0 and lower voltage is logic 1.

n-channel PMOS



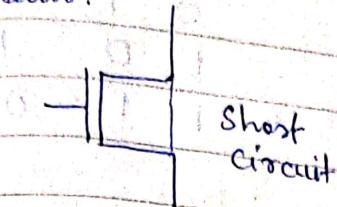
p-channel NMOS



for logic $1 \geq 5V$

$$V_{GS} > V_{th}$$

hence channel forms
betⁿ Source and
drain.



for logic $0 \leq -5V$

$$V_{GS} < V_{th}$$

no channel,
so open circuit

for logic $1 \geq 5V$

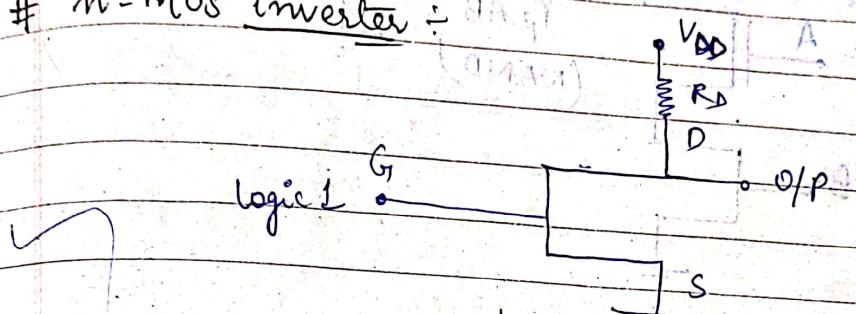
! no channel,
so open circuit

for logic $0 \leq -5V$

channel formed betⁿ
source and drain



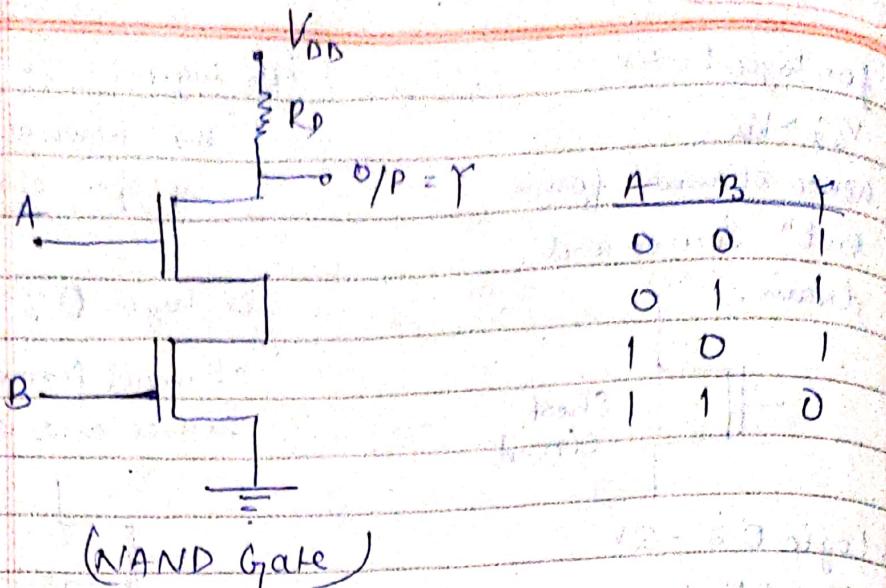
n-MOS inverter :



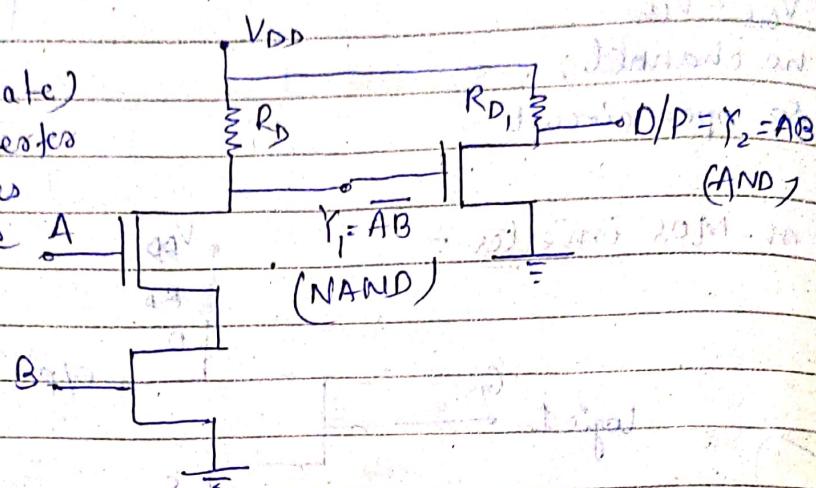
Logic 1 : Input G → Logic 0 → O/P = 0V → 0V → Logic 0

Logic 0 : Input G → Logic 1 → O/P = VDD → VDD → Logic 1

∴ Invertor is a device which takes 0V at its input and gives 0V at its output.

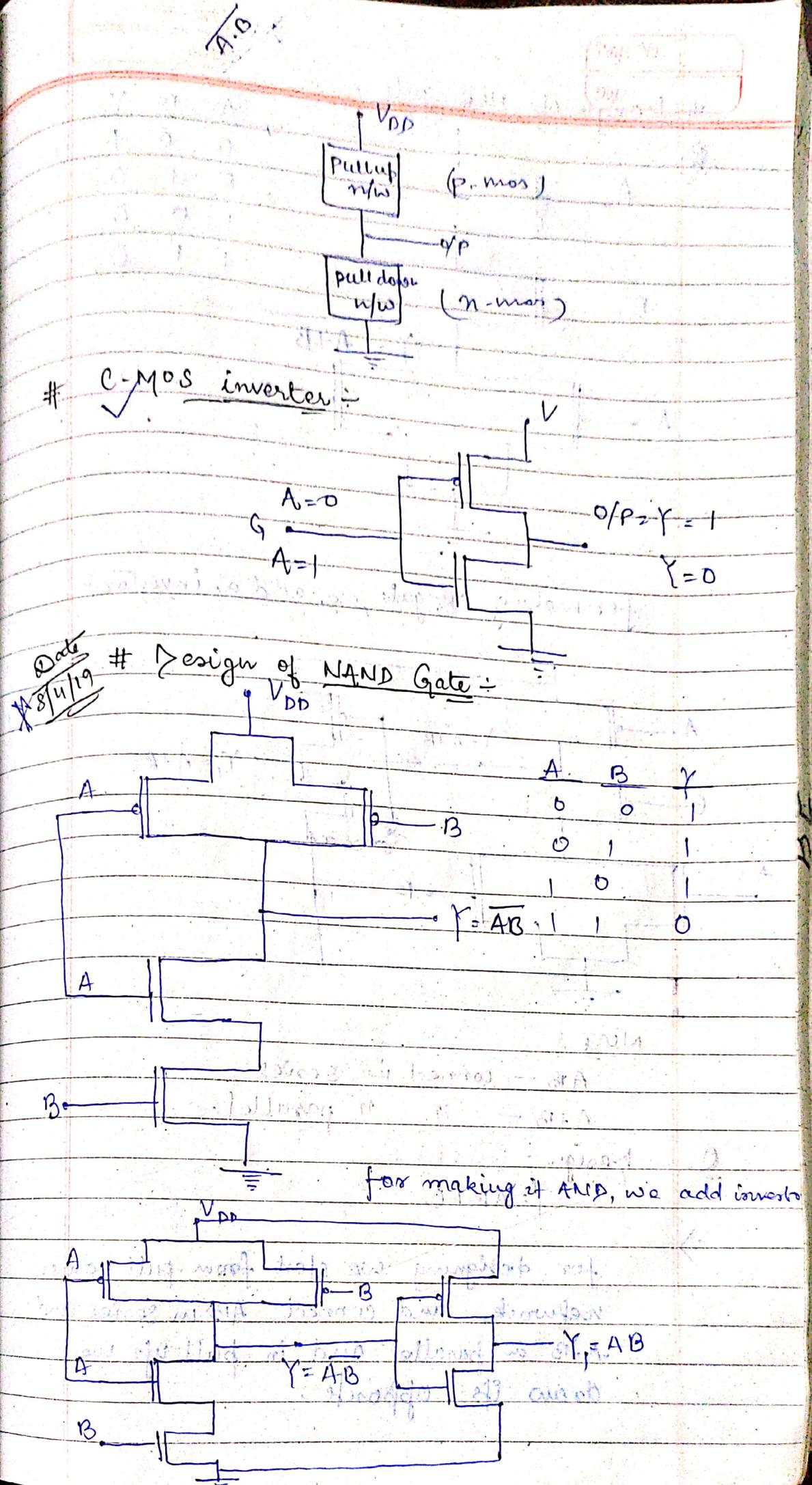


for
(AND Gate)
join a inverter
O/P becomes
opposite

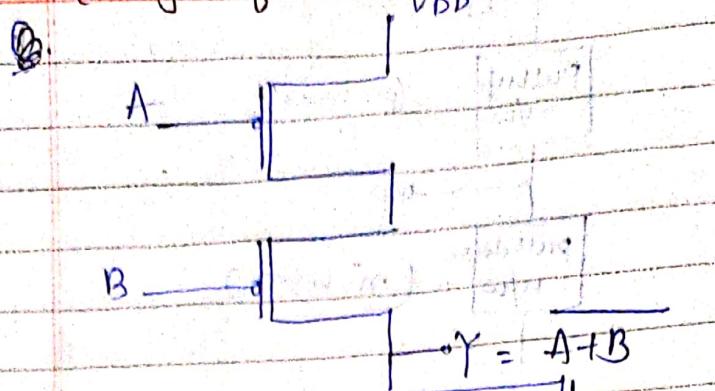


In n-MOS, logic 1 cannot send from source to drain. Similarly in p-MOS, logic 0 can't send from S to D, to avoid such inability of n-MOS (transmission of logic 1) and p-MOS (transmission of logic 0), we will go for CMOS technology.

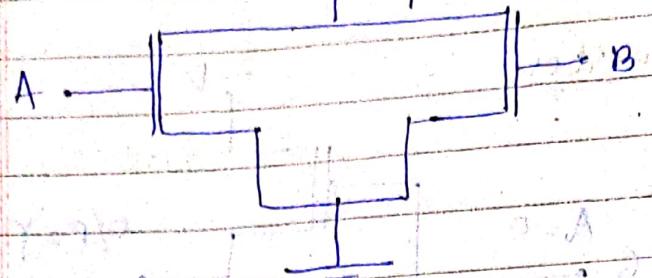
In CMOS technology there are two network; pull-up network and pull-down network. pull-down network is always grounded and which is controlled by only n-MOS and pull-up network is always connected to VDD and consists by only ~~only~~ p-MOS. In betⁿ these two, O/P is taken



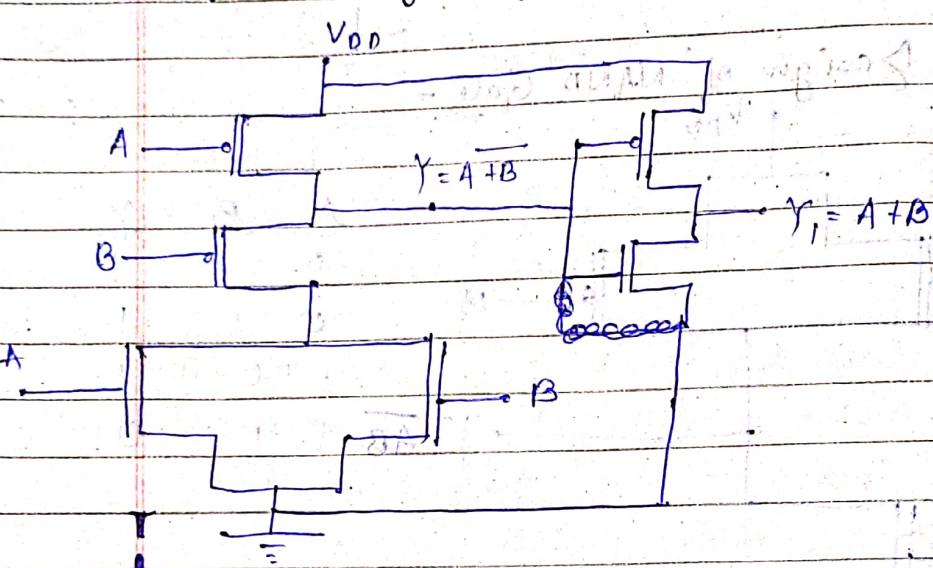
Design of NOR gate :-



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



for making OR gate, we add a inverter.



NOTE :-

A.B — connect in series

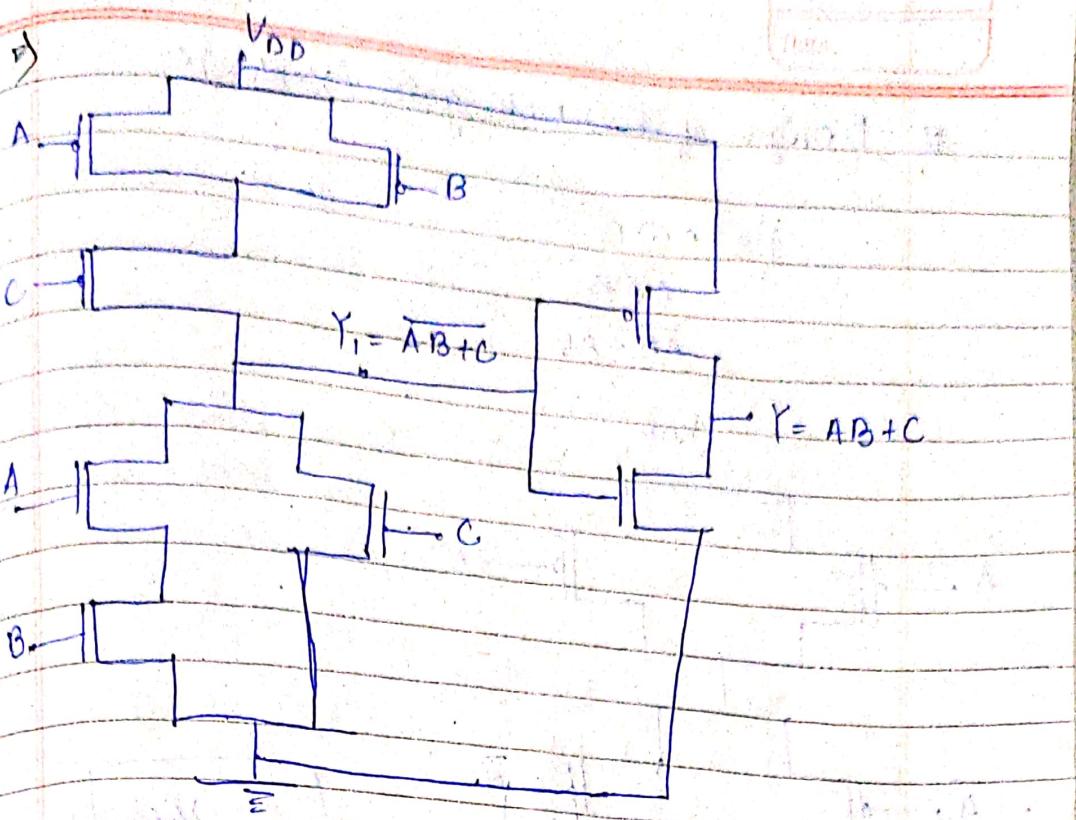
A+B — " " parallel.

Q. Design -

$$Y = A \cdot B + C$$

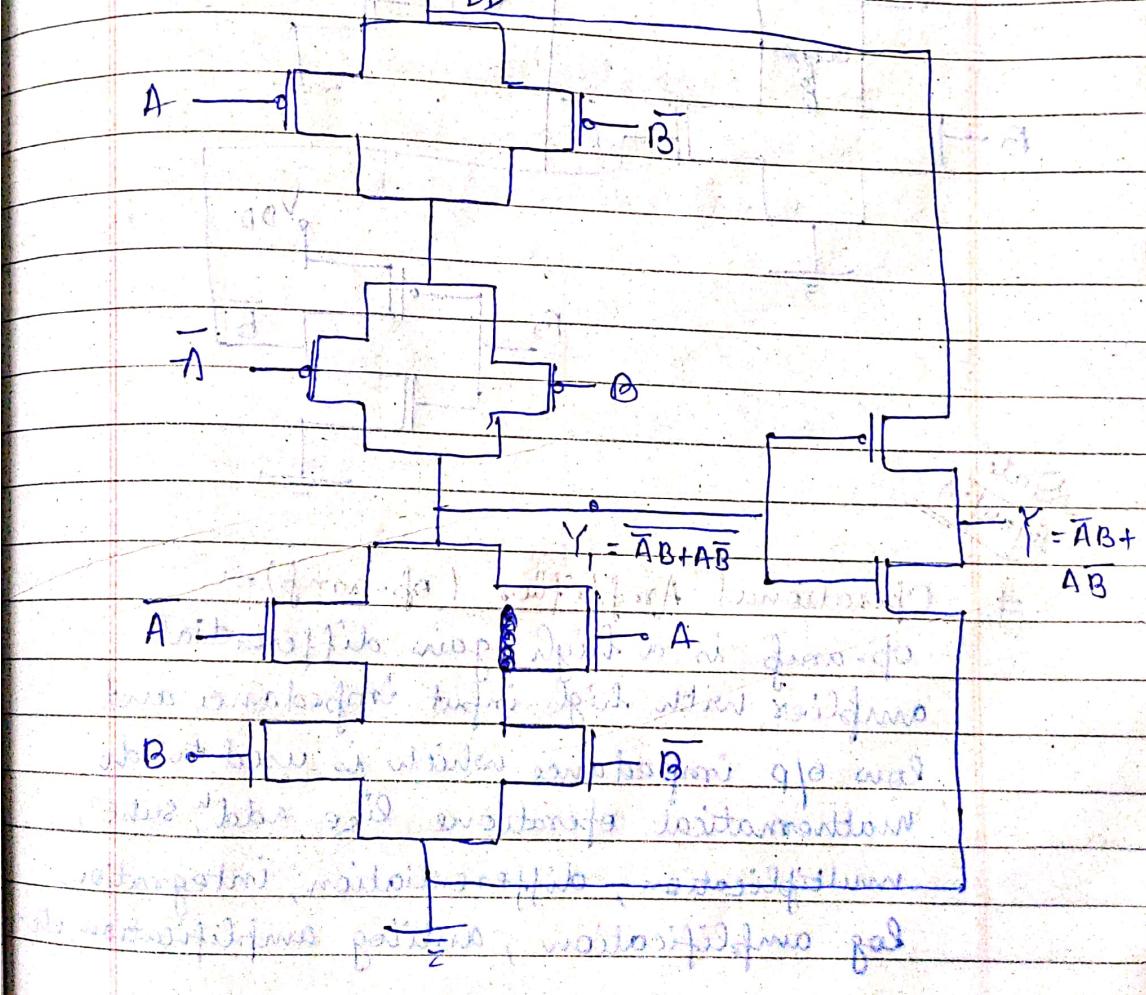
⇒

for designing we start from pull-down network and connect A.B in series and A+B in parallel and in pull up we draw E's / Opposite,



Design of Ex-OR (X-OR)

$$\begin{aligned} Y &= A \oplus B \\ &= A\bar{B} + \bar{A}B \end{aligned}$$

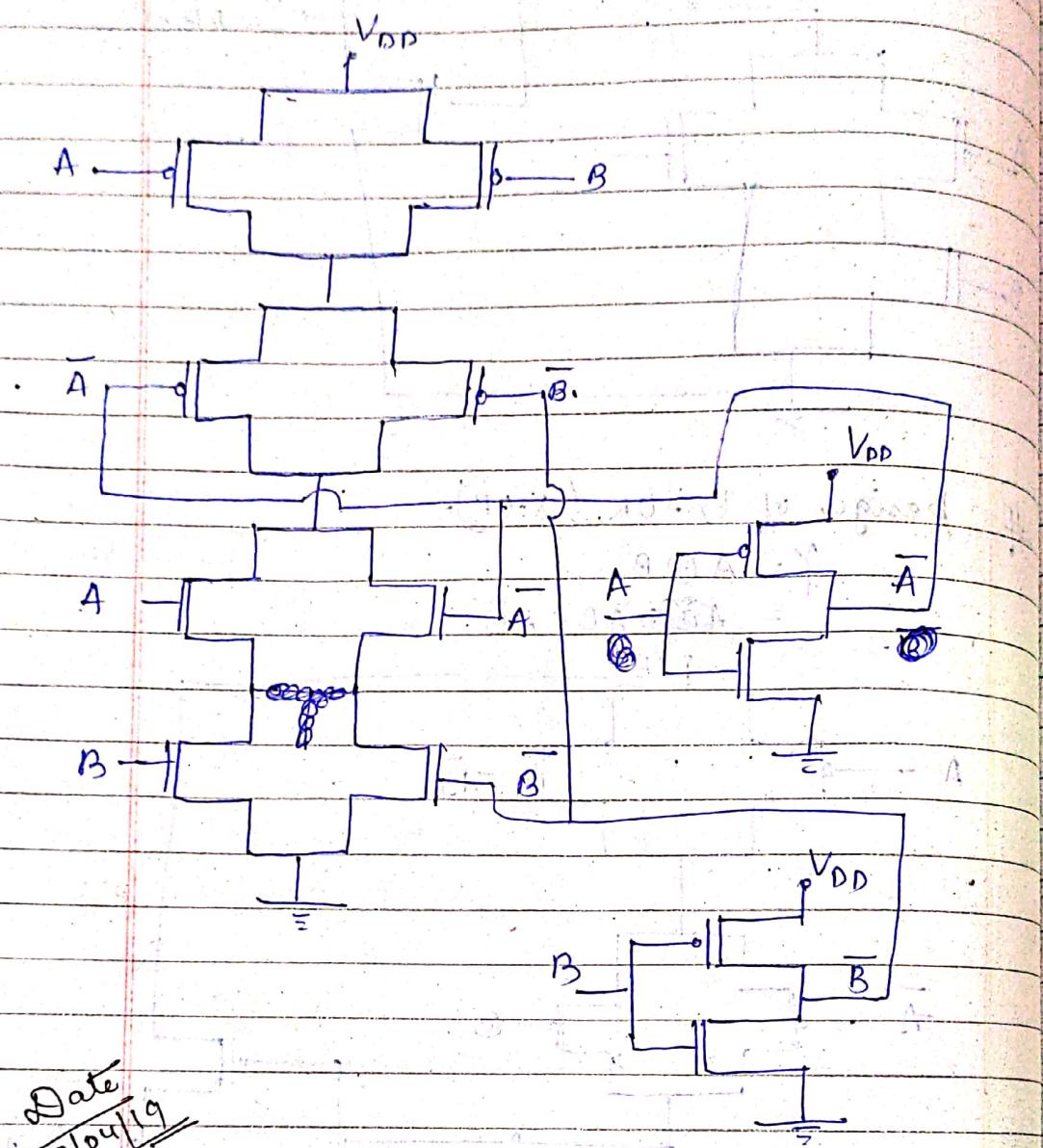


Design of Ex-NOR gate (X-NOR) :-

$$Y = A \odot B$$

$$= \overline{A \oplus B}$$

$$\therefore \overline{AB} + AB$$

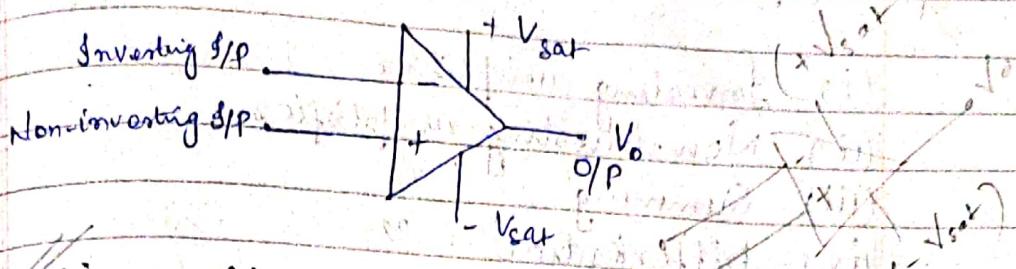


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Operational Amplifier (Op-amp) :-

Op-amp is a high gain differential amplifier with high input impedance and low o/p impedance which is used to do mathematical operations like add, sub, multiplication, differentiation, integration, log amplification, antilog amplification, etc.

Schematic diagram →



Pin configuration / Pin diagram →

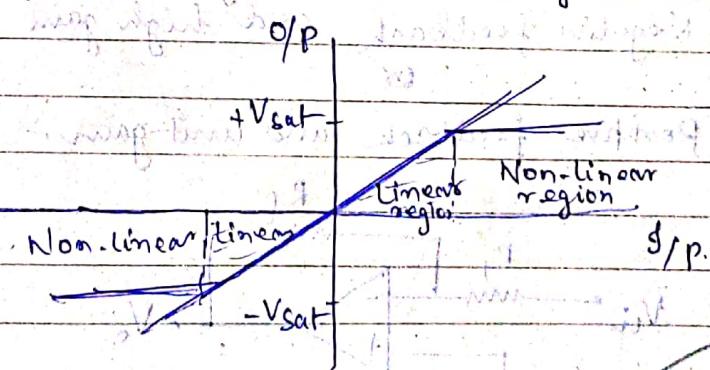
Op-amp is an integrated circuit (IC) - 741
It is a 8 pin IC.

Pin No.	Function	Pin No.	Function
8	No connection	1	Offset Null
7	+V _{sat}	2	741
6	O/P	3	
5	Offset Null	4	-V _{sat}

Transfer characteristic of op-amp →

Op-amp has two regions of operation -

linear and non-linear region



Characteristics of ideal op-amp →

i. I/P imp (Z_i) = ∞

ii. O/P imp (Z_o) = 0

iii. Voltage gain (A_v) = ∞

iv. CMRR (common mode rejection ratio) = ∞

v. Slew rate = 0

vi. No offset voltage.

Application of op-amp in linear region

- (i) Inverting amplifiers
- (ii) Non-inverting amplifiers
- (iii) Summing "
- (iv) Differential "
- (v) Integrator

Virtual Ground:

Potential on the ground at any point is always OV and bet' pot. diff. bet' any two point on the ground is OV but maxⁱⁿ current is going into the ground.

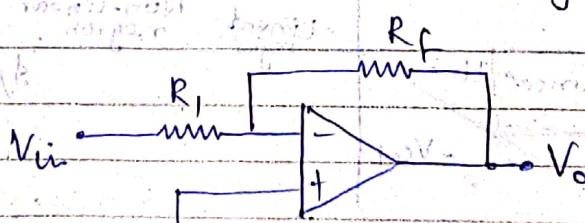
In case of virtual ground, potential at any point may be equal, (if may or may not equal to OV) but the pot. diff. bet' any two points on the virtual ground is always OV and current flowing through the virtual ground is always OA.

Condition for Virtual ground -

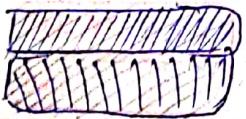
✓ Negative feedback and high gain

or

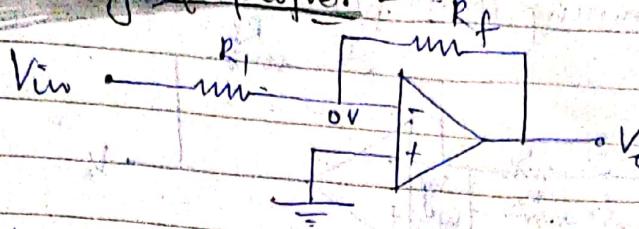
✓ Positive feedback and unit gain.



In the diagram there is a +ve feedback and op-amp is at high gain so, there is a virtual ground bet' for inverting and non-inverting terminals of op-amp.



Inverting Amplifier:



Applying Nodal Analysis at inverting terminal -

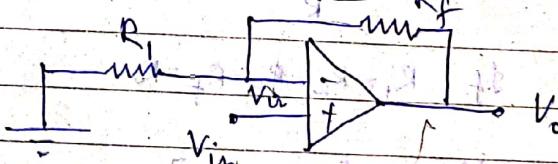
$$0 - V_{in} + \frac{0 - V_o}{R_f} + 0 = 0$$

$$\Rightarrow V_o = - \frac{R_f \cdot V_{in}}{R_i}$$

Phase diff. Betw V_{in} and V_o is 180° , so it is called as inverting amplifier.

$$[AV = \frac{V_o}{V_{in}} = -\frac{R_f}{R_i}]$$

Non-inverting amplifier:



$$V_{in} - 0 + V_{in} - 0 V_o = 0$$

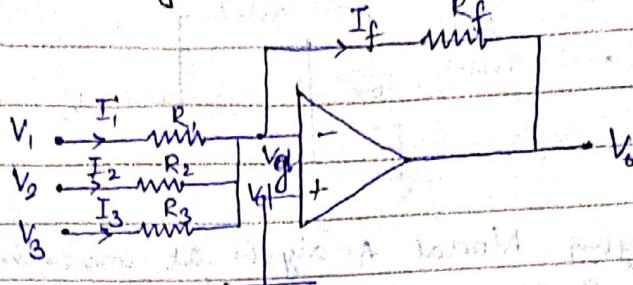
$$\Rightarrow V_{in} \cdot R_f \left[\frac{1}{R_i} + \frac{1}{R_f} \right] = V_o$$

$$V_o = V_{in} \left[1 + \frac{R_f}{R_i} \right]$$

$$AV = \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_i}$$

Phase diff. Betw V_{in} and V_o is 0° , so it is non-inverting amplifier.

C

(Part)Summing amplifier

$$V_d \approx 0$$

$$V^+ = V^-$$

$$\text{Assume } \frac{0-V_1}{R_1} + \frac{0-V_2}{R_2} + \frac{0-V_3}{R_3} + \frac{0-V_o}{R_f} = 0$$

$$\Rightarrow \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_o}{R_f}$$

$$\therefore V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

Case 1 \therefore If $R_1 = R_2 = R_3 = R_f$

$$\therefore V_o = -R_f \left[V_1 + V_2 + V_3 \right]$$

Case 2 \therefore If $R_1 = R_2 = R_3 = R_f = R$

$$\therefore V_o = -[V_1 + V_2 + V_3]$$

\therefore This circuit is known as summing amplifier.

Voltage follower/Unity gain amplifier —



It acts as a buffer circuit.

Here voltage gain is unity.

In an non-inverting op-amp -

$$V_o = \left[1 + \frac{R_f}{R_i} \right] V_i$$

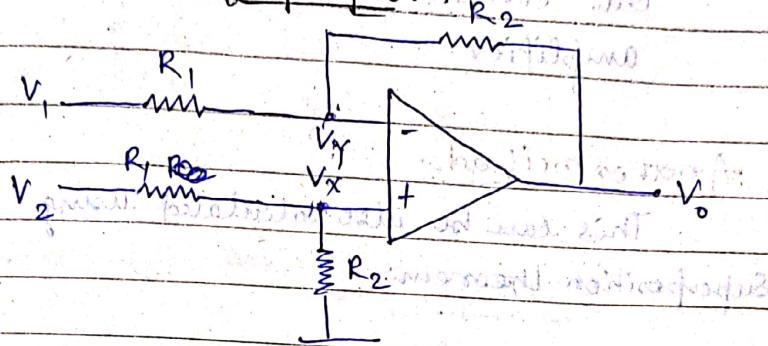
but here $R_f = 0$

$$\therefore V_o = V_i$$

$$\Rightarrow \frac{V_o}{V_i} = 1$$

$$\therefore A_v = 1$$

Difference Amplifier



for virtual ground $\therefore V_x = V_y$

$$\boxed{V_x = V_y}$$

$$\frac{V_1 - V_y}{R_1} = \frac{V_p - V_o}{R_2}$$

$$\Rightarrow \frac{V_p}{R_1} + \frac{V_p}{R_2} = \frac{V_1 + V_o}{R_1 + R_2}$$

$$\Rightarrow V_p \left[\frac{1}{R_1} + \frac{1}{R_2} \right] = \frac{R_2 V_1 + R_1 V_o}{R_1 + R_2}$$

$$\Rightarrow V_p = \frac{R_2 V_1 + R_1 V_o}{R_1 + R_2}$$

$$\Rightarrow V_p = \frac{R_2 V_1 + R_1 V_o}{R_1 + R_2}$$

$$\boxed{V_p = \frac{V_1 R_2 + V_o R_1}{R_1 + R_2}}$$

Similarly

$$V_x = V_p$$

$$\boxed{V_x = \frac{V_1 R_2}{R_1 + R_2}}$$

$$\therefore V_x = V_y$$

$$\Rightarrow \frac{V_1 R_2 + V_0 R_1}{R_1 + R_2} = \frac{V_2 R_2}{R_1 + R_2}$$

$$\Rightarrow V_0 = \frac{(V_2 - V_1) R_2}{R_1}$$

$$\text{If } R_1 = R_2 = R$$

$$V_0 = V_2 - V_1$$

\therefore this circuit is known as difference amplifier.

Another method:-

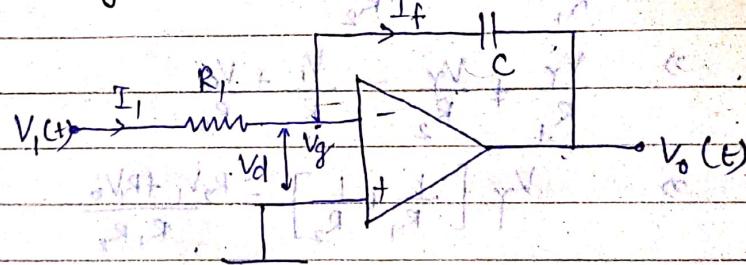
This can be also calculated using Superposition theorem.

$V_o = \text{voltage due to } V_1$ and $V_o = \text{voltage due to } V_2$

$$V_2 = 0$$

$$V_1 = 0$$

Integrator amplifier



$$\frac{0 - V_1(s)}{R_1} + \frac{0 - V_0(s)}{Y_{CS}} + 0 = 0$$

$$Y_{CS} = \frac{V_0(s)}{V_1(s)}$$

$$\Rightarrow V_1(s) = C s V_0(s)$$

$$\Rightarrow V_0(s) = -\frac{1}{R C} \frac{V_1(s)}{s}$$

$$V_0(t) = -\frac{1}{R C} \int V_1(t) dt$$

$$Q = CV$$

$$\frac{dQ}{dt} = C \frac{dV}{dt}$$

$$I = \frac{C dV}{dt}$$

$$\frac{0-V_1}{R_1} + \cancel{\text{cancel}} \cdot \frac{C dV}{dt} \frac{(0-V_0)}{R_2} = 0$$

$$\Rightarrow \frac{V_1}{R_1} = -C \frac{dV_0}{dt}$$

$$\Rightarrow -\int \frac{V_1}{R_1} dt = \int dV_0$$

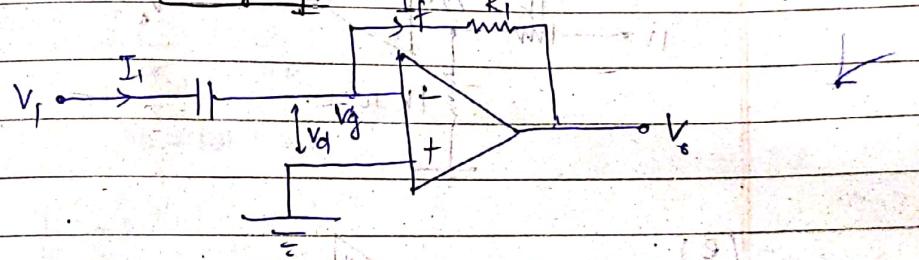
$$Q = CV$$

$$\frac{dQ}{dt} = C \frac{dV}{dt}$$

$$I = \boxed{\frac{dV}{dt}}$$

$$\Rightarrow \boxed{V_0 = -\frac{1}{RC} \int V_1 dt}$$

Differential amplifier :-



$$\cancel{\text{cancel}} \quad C \frac{d}{dt} (V_1 - 0) = \frac{0 - V_0}{R_1}$$

$$\Rightarrow \boxed{V_0 = -R_1 C \frac{dV_1}{dt}}$$

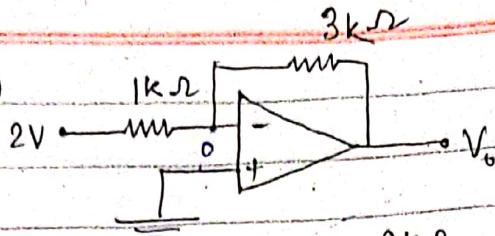
~~cancel~~

$$\frac{0 - V_0}{R_1} + C \frac{d}{dt} (0 - V_1) = 0$$

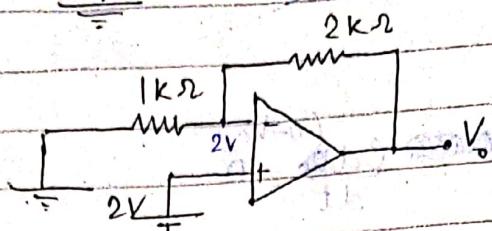
$$\Rightarrow -\frac{V_0}{R_1} + \cancel{\frac{C dM_1}{dt}} = 0$$

$$\Rightarrow \boxed{V_0 = -R_1 C \frac{dV_1}{dt}}$$

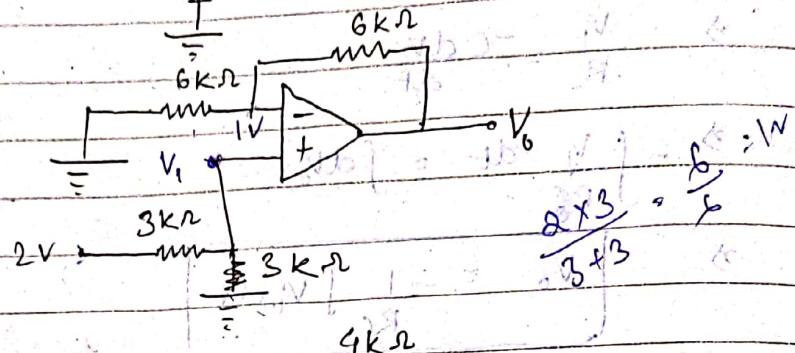
Q. (a)



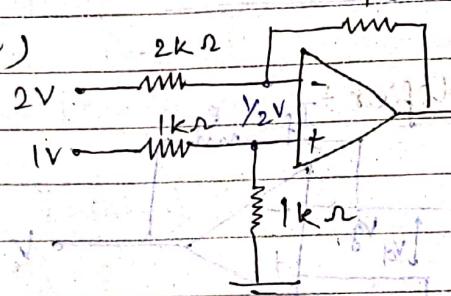
(b)



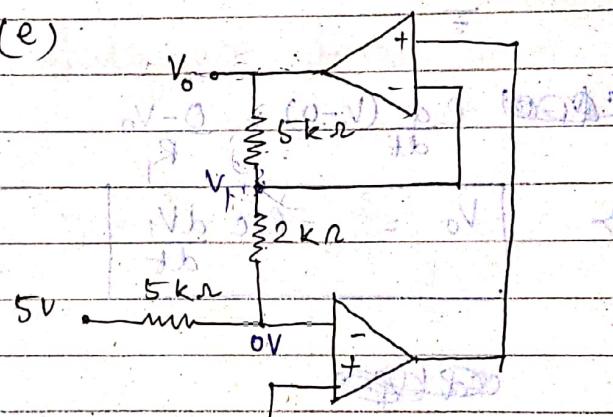
(c)



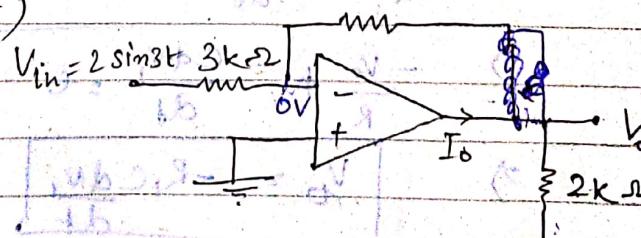
(d)



(e)



(f)



$$V_o = ? , I_o = ?$$

Applying nodal ab inverting terminal :-

(a) $\frac{6-0}{1k} + \frac{0-V_o}{3k} + 0 = 0$

$$\Rightarrow \frac{V_o}{3k} = -2m$$

$$V_o = -6V$$

~~V_o = I_o~~

(b) $\frac{2-0}{1k} + \frac{2-V_o}{2k} + 0 = 0$

$$\Rightarrow \frac{V_o-2}{2k} = 2m$$

$$\Rightarrow V_o = 6V$$

(c) $V_i = \frac{2V \times 3k}{6k}$

$$= 1V$$

$$\frac{1-0}{6k} + \frac{1-V_o}{6k} + 0 = 0$$

$$\Rightarrow \frac{V_o-1}{6k} = \frac{1}{6k}$$

$$V_o = 2V$$

~~V_o = JR~~

(d)

$$\frac{\frac{1}{2}-2}{2k} + \frac{V_2-V_o}{4k} = 0$$

$$I = \frac{V}{R}$$

$$\frac{V_o-V_2}{4k} = \frac{\frac{1}{2}-2}{3k}$$

$$\Rightarrow \frac{V_o-V_2}{2} = \cancel{-1} \frac{1-4}{2}$$

$$\Rightarrow V_o = \cancel{-3} \frac{1}{2} + V_2$$

$$V_o = \frac{5}{2}V$$

(e) $V_i = \frac{5 \times 5}{5+4} = \frac{25}{12}V$

$$\frac{25}{12} - \frac{5}{7k} + \frac{V_2-V_o}{5k} = 0$$

$$\Rightarrow V_o - \frac{25/12}{5k} = \frac{25-60}{12 \times 7k}$$

$$\Rightarrow 12V_o - 25 = \cancel{-38} \frac{5}{5k}$$

$$\Rightarrow 12V_o = \cancel{25}$$

$$\Rightarrow \frac{12V_o - 25}{12 \times 5k} = \frac{25-60}{12 \times 7k}$$

(e) KCL at node 0

$$\frac{0-V_0}{5k} + \frac{0-V_0}{7k} = 0$$

$$\frac{V_0}{7k} = -\frac{5}{5k}$$

$$V_0 = -7V$$

(f) $0 - \frac{2 \sin 3t}{3k} + \frac{0-V_0}{5k} = 0$

$$\frac{V_0}{5k} = -\frac{2 \sin 3t}{3k}$$

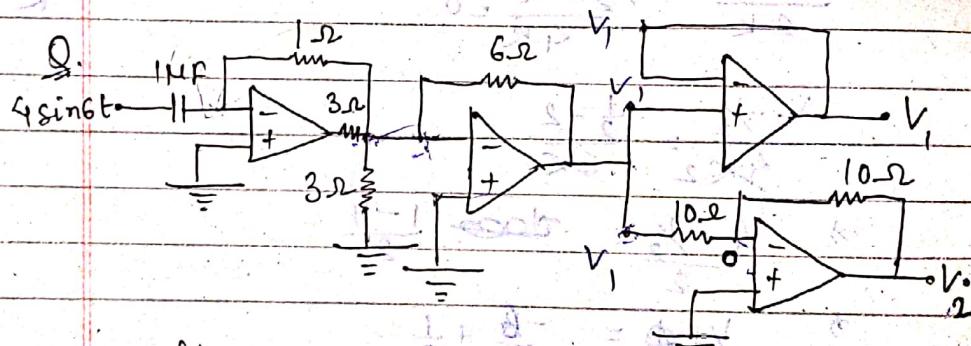
$$V_0 = -\frac{10 \sin 3t}{3}$$

$$\frac{V_0-0}{2k} - I_0 + \frac{V_0-0}{5k} = 0$$

$$\Rightarrow \frac{7V_0}{10k} = I_0$$

$$\Rightarrow I_0 = \frac{7}{10} \times -\frac{10 \sin 3t}{3}$$

$$I_0 = -\frac{7}{3} \sin 3t \text{ mA}$$

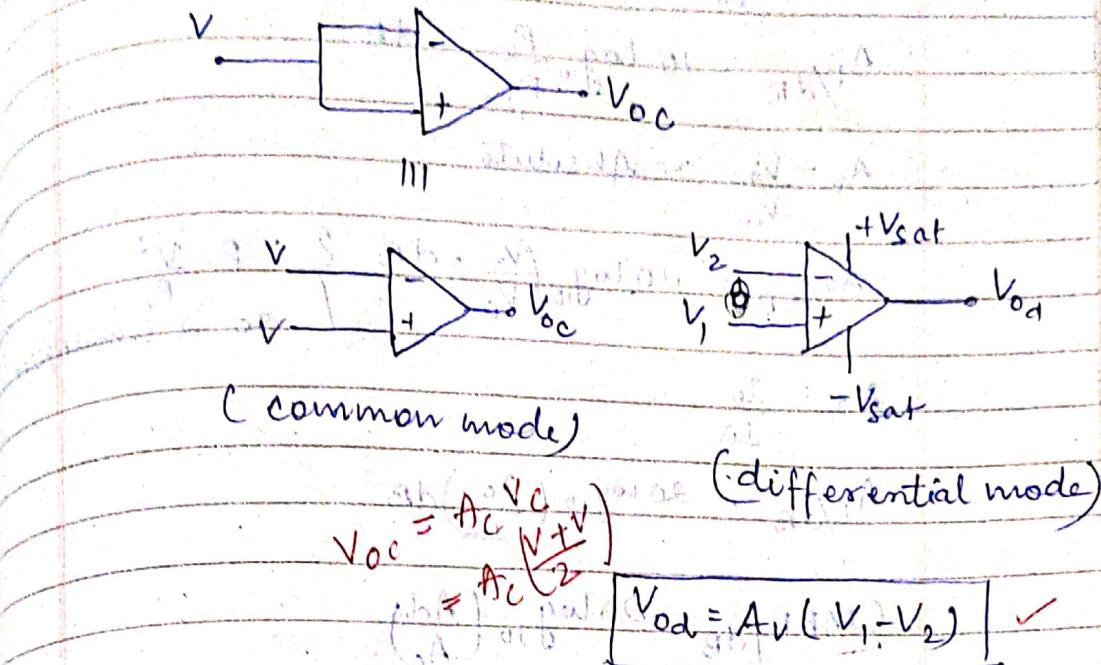


find relation bet' V_1 and V_2 .

$$\frac{0-V_1}{10} + \frac{0-V_2}{10} = 0$$

$$V_1 = -V_2$$

B. # Common mode Rejection Ratio (CMRR) :-



- One of the important feature of operational amplifier is it greatly amplifies the differential input applied at inverting and non-inverting terminal and it also slightly amplifies the signal that are common to both inverting and non-inverting terminal.
- So, total O/P in operational amplifier is due to both diff. S/P as well as common S/P.
- Since the amplification of differential input is much greater than the common mode S/P then there is a change of rejection of common mode O/P (V_{oc}) with respect to differential O/P.
- This rejection is described by a numerical factor which is called as Common mode rejection ratio. CMRR is defined as the ratio of differential gain to the common mode gain.

$$CMRR \triangleq \frac{A_d}{A_c}$$

$$A_p = \frac{P_o}{P_{in}} \rightarrow \text{Absolute scale}$$

$$A_p/dB = 10 \log_{10} \frac{P_o}{P_{in}} dB$$

$$A_v = \frac{V_o}{V_{in}} \rightarrow \text{Absolute}$$

$$A_v/dB = 20 \log_{10} \left(\frac{V_o}{V_{in}} \right) dB \quad \left\{ \begin{array}{l} P = \frac{V^2}{R} \\ \text{so } 2 \text{ is multiplied} \end{array} \right.$$

$$A_I = \frac{I_o}{I_{in}}$$

$$A_I/dB = 20 \log_{10} \left(\frac{I_o}{I_{in}} \right) dB$$

$$\therefore CMRR/dB = 20 \log_{10} \left(\frac{Ad}{A_c} \right)$$

Q If an op-amp with diff. gain = 10^6 dB and
CMRR is 20 dB, determine common mode gain
if $CMRR = 20$ dB is half its original

$$\Rightarrow 20 \log_{10} \left(\frac{Ad}{A_c} \right) = 20 \text{ dB}$$

This represents about 20 times diff. input

$$\Rightarrow \frac{10^6}{A_c} = 10^6 \text{ provides more}$$

Common mode gain A_c is 10^6

$$\text{In mode of diff. } A_c = \frac{10^6}{10} = 10^5$$

Q Repeat above question with $Ad = 20$ dB,
determine A_c .

$$\Rightarrow \text{Given, } CMRR = 20 \text{ dB. if reduced to 10 dB.}$$

$$\Rightarrow 20 \log_{10} \left(\frac{Ad}{A_c} \right) = 10 \text{ dB at 10 dB}$$

Half the output of original given (10) above

$$\Rightarrow \cancel{20} \cancel{20} \log_{10} \left(\frac{Ad}{A_c} \right) = 1$$

Assume Ad is not affected by A_c first

then we have $Ad = 20$ dB. as indicated earlier

$$\Rightarrow 20 \log Ad = 20 \text{ (data unchanged)}$$

Initial output for other gain is given as 20 dB

Now change A_c from 10 to 20

$\therefore A_c = 20$ dB

$$P_d = \frac{V_o}{V_{in}}$$

$$\therefore \log_{10} \left(\frac{10}{A_C} \right) = 1$$

$$\Rightarrow A_C = 1$$

Total O/P in op-amp = diff. O/P + common mode O/P

$$V_o = V_{od} + V_{oc}$$

$$\Rightarrow V_o = A_d V_d + A_c V_c$$

where $V_d = \text{diff. S/P, } V_1 - V_2$

$$V_c = \text{common mode S/P} \\ = \frac{V_1 + V_2}{2}$$

$$V_o = A_d (V_1 - V_2) + A_c \left(\frac{V_1 + V_2}{2} \right)$$

$$= \left(A_d + \frac{A_c}{2} \right) V_1 - \left(\frac{A_c}{2} - A_d \right) V_2 \\ = A_1 V_1 + A_2 V_2$$

$$\text{where } A_1 = A_d + \frac{A_c}{2}$$

$$A_2 = \frac{A_c - A_d}{2}$$

$$\Rightarrow A_c = A_1 + A_2$$

$$A_d = \frac{A_1 - A_2}{2}$$

$$A_1 = \frac{V_o}{V_1, V_2 = 0}$$

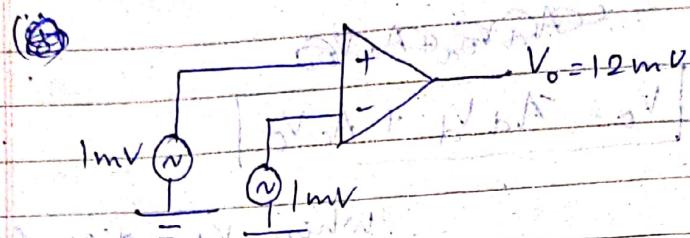
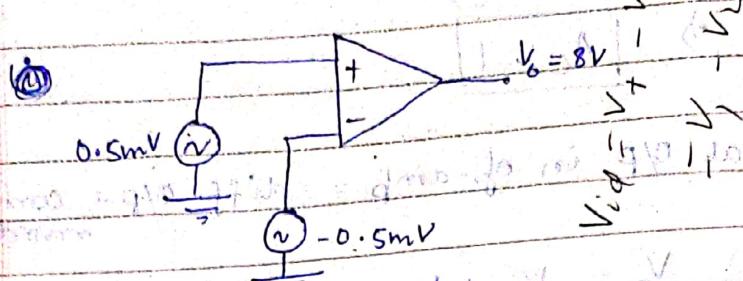
$$A_2 = \frac{V_o}{V_2, V_1 = 0}$$

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Q Calculate CMRR -



$$A_d = \frac{V_{od}}{V_{id}} = \frac{V_{od}}{V_1 - V_2} = \frac{8}{(0.5 + 0.5)m} = 8000$$

$$A_c = \frac{V_{od}}{V_{ic}} = \frac{12m}{V_1 + V_2} = \frac{12}{2m}$$

$$CMRR = \frac{A_d}{A_c} = \frac{8000}{12}$$

$$CMRR \text{ in } dB = 20 \log_{10} \left(\frac{A_d}{A_c} \right) \text{ dB}$$

$$= 20 \log \left(\frac{8000}{12} \right) \text{ dB}$$

Q Determine the o/p voltage of an op-amp for the s/p voltage $V_{i_1} = 200\mu V$ and $V_{i_2} = 140\mu V$. The amplifier has the differential gain 6000 and $CMRR = 200$.

$$\Rightarrow A_d = \frac{V_{od}}{V_{id}}$$

$$\Rightarrow 6000 = \frac{V_{od}}{V_{i_1} - V_{i_2}} = \frac{V_{od}}{(200 - 140)\mu}$$

$$\therefore V_{od} = (6000 \times 60)\mu$$

$$V_{od} = 360000\mu V$$

$$CMRR = \frac{A_d}{A_c}$$

$$\Rightarrow 200 = \frac{6000}{A_c}$$

$$A_c = 30$$

$$\Rightarrow \frac{V_{oc}}{V_{ic}} = 30$$

$$\Rightarrow \frac{V_{oc}}{\frac{V_1 + V_2}{2}} = 30$$

$$\Rightarrow \frac{V_{oc}}{170} = 30$$

$$V_{oc} = 5100 \text{ mV}$$

$$= 0.0051 \text{ V}$$

$$V_o = V_{od} + V_{oc}$$

$$= 0.3651 \text{ V}$$

Slew Rate

Slew rate is defined as the \max^m rate of change of O/P for any possible S/I P. signal of an op-amp, i.e., the \max^m slope of O/P of an op-amp



$$\text{Slew rate} = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

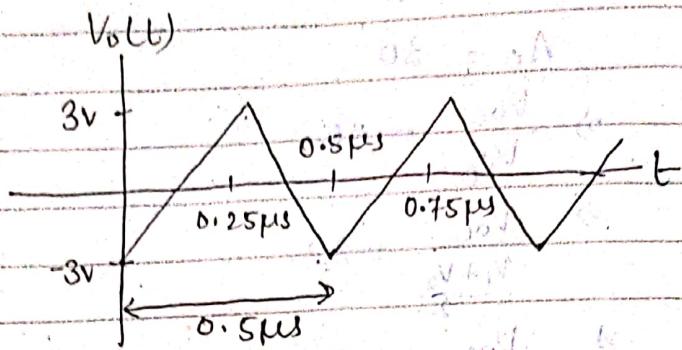
Unit: $(V/\mu s)$

for a signal, $V_o(t) = V_m \sin \omega f t$

$$\frac{dV_o}{dt} = V_m \cdot 2\pi f \cos \omega f t$$

$$\therefore \left. \frac{dV_o}{dt} \right|_{\text{max}} = 2\pi V_m f$$

Q. Determine the slew rate of the given O/P for op-amp which is shown below -



$$\Rightarrow \text{Slew rate} = \left. \frac{dV_o}{dt} \right|_{\text{max}}$$

$$f = \frac{1}{T} = \frac{1}{0.5 \mu s} = 2 \text{ MHz}$$

$$\text{Slew rate} = 2 \times \pi f m$$

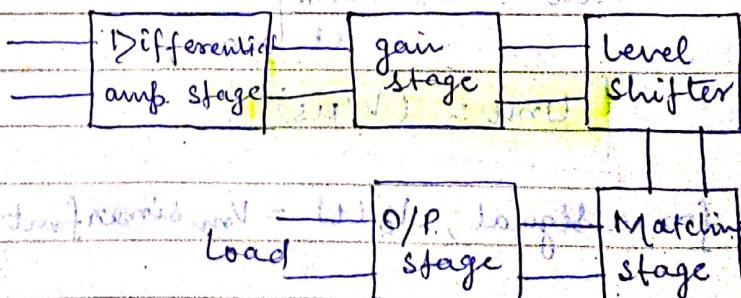
$$= 2 \times \pi \times 2 \times 10^6$$

$$\frac{dV_o}{dt} = 12 \text{ V/μs}$$

$$\frac{dV_o}{dt} \Big|_{\text{max}} = \frac{3 - (-3)}{0.25 \mu s} = 24 \text{ V/μs}$$

$$= 24 \text{ V/μs}$$

Block diagram of op-amp :-



Date
07/04/19

29th April) Assign - Ch-10

Q(1 to 15), 25 (Op-amps)

24 Ch-11

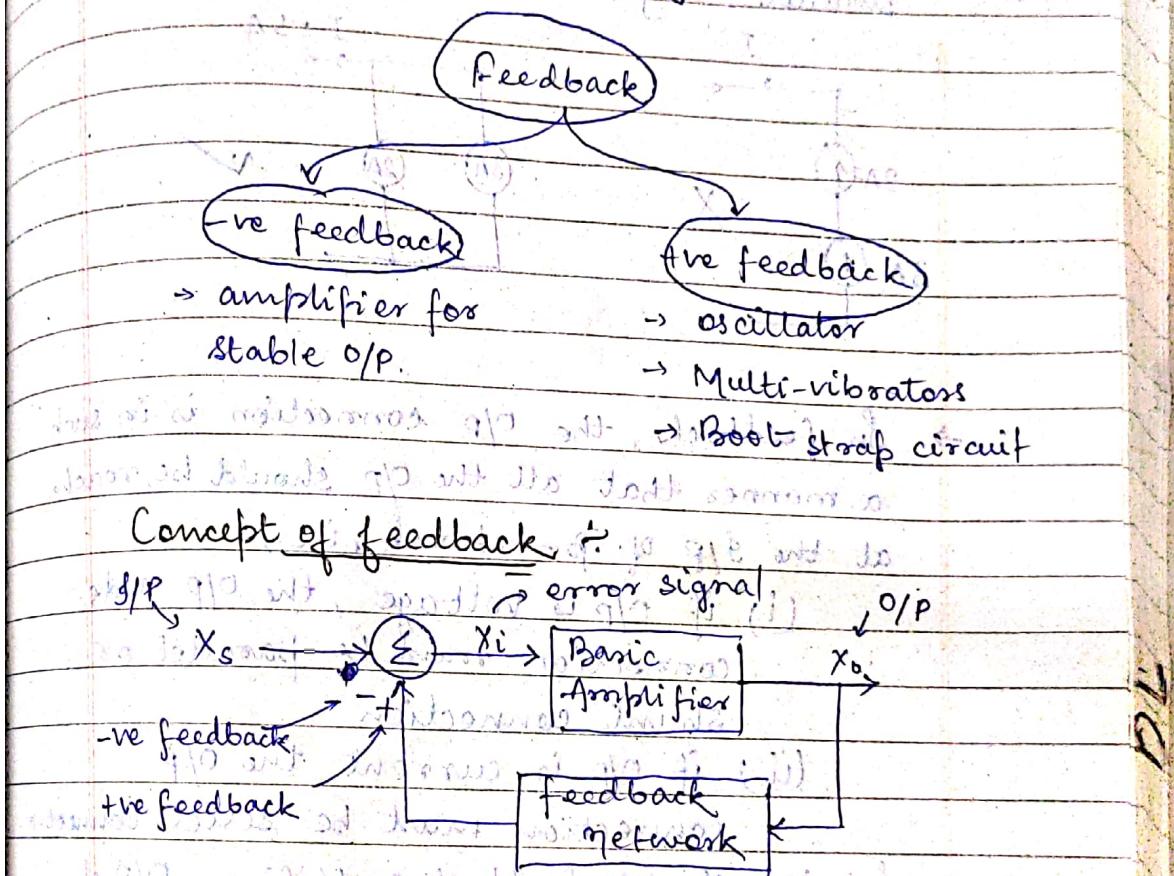
(Op-amp app),
Q. 1 to 13

Feedback :-

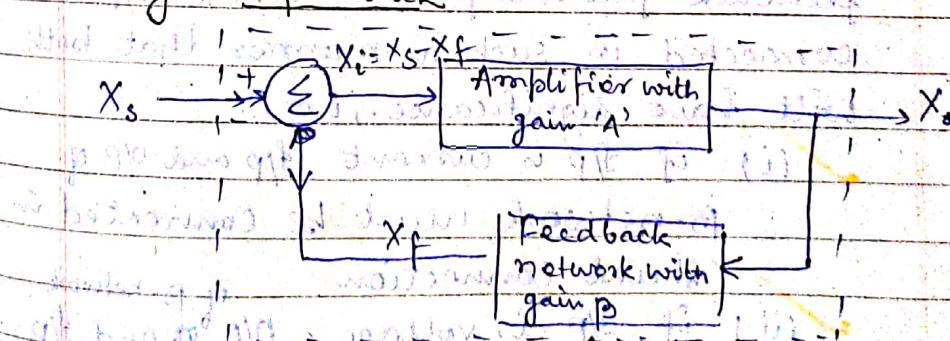
Feedback is used to control the output of the system to fulfill the requirement.

There are two types of feedback -

- Negative feedback
- Positive feedback



Negative feedback -

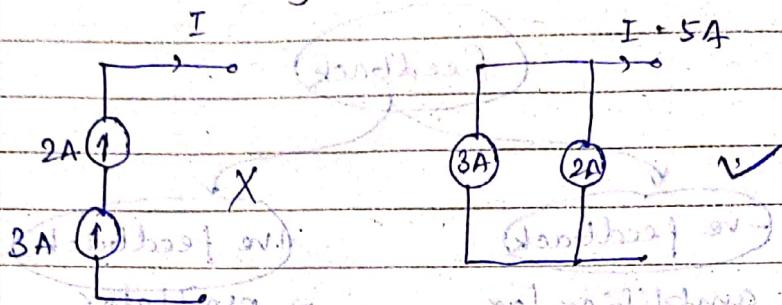


$$X_i = X_s - X_f$$

Fig. -ve feedback amplifier
(-ve X_f for -ve feedback)

NOTE -

- ① Two different ideal current source never be connected in series, they must be connected in parallel.
- ② Two ideal voltage source never be connected in parallel, they must be connected in series.



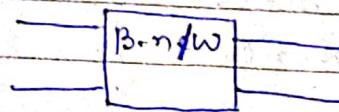
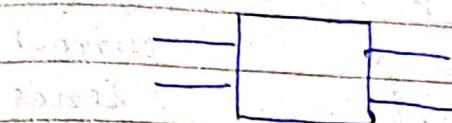
→ In feedback, the O/P connection is in such a manner that all the O/P should be reach at the S/P of β -network, i.e.,

- (i) if O/P is voltage, the O/P side connection must be parallel or shunt connection.
 - (ii) if O/P is current, the O/P side connection must be series connection.
- In S/P of -ve feedback amplifier, O/P of feedback feedb amp network, the S/P are connected in such a manner that both will have significance, i.e.,
- (i) if S/P is current, S/P and O/P of β -network must be connected in shunt connection.
 - (ii) if S/P is voltage, O/P and S/P must be connected in series.

i. Types of feedback amplifier :-

i. Voltage amplifier :-

<u>S/P</u>	<u>O/P</u>
Voltage	Voltage (sampling)
S/P connection = series	O/P connection = shunt



- Voltage series feedback amplifier
- Series-shunt feedback amplifier

ii. Current -amplifier :-

<u>S/P</u>	<u>O/P</u>
Current	Current
Shunt	Series

- Current - shunt feedback amplifier.
- Shunt - series feedback amplifier.

iii. Trans impedance amplifier :-

$$\text{Trans.} = \frac{\text{O/P}}{\text{S/P}}$$

$$\text{impedance} = \frac{\text{voltage}}{\text{current}}$$

<u>S/P</u>	<u>O/P</u>
current	voltage
shunt	shunt

- Voltage shunt feedback amplifier
- Current shunt shunt II II

iv. Transconductance \rightarrow

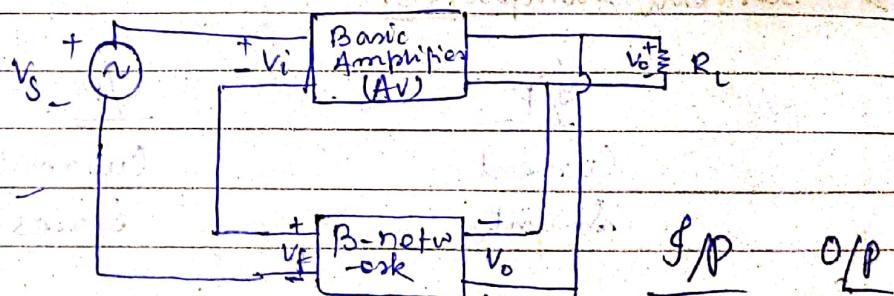
Transconductance = $\frac{\text{O/P current}}{\text{S/P voltage}}$

S/P O/P
voltage current
series series

- Current series feedback amplifiers
- Series series II

Topology of feedback amplifier -

Voltage series / voltage amp. (Series-Shunt
series shunt)



Applying KVL at S/P =

$$V_s - V_i - V_f = 0$$

$$\text{gain } V_i = V_s - V_f$$

Voltage without feedback -

$$A_V = \frac{V_o}{V_i}$$

Voltage gain with feedback =

$$A_{V_f} = \frac{V_o}{V_s}$$

$$\begin{aligned}
 \Rightarrow A_{vf} &= \frac{V_o}{V_i + V_f} \\
 &= \frac{V_o / V_o}{V_i / V_i + V_f / V_i} \\
 &= \frac{A_v}{1 + \frac{V_f}{V_i}} \\
 &= \frac{A_v}{1 + \frac{V_f \times V_o}{V_o / V_i}}
 \end{aligned}$$

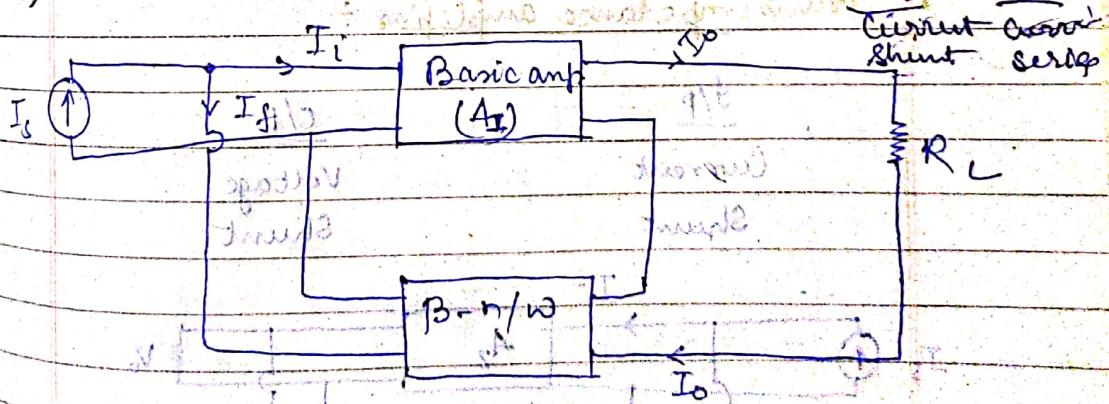
$$\boxed{A_{vf} = \frac{A_v}{1 + \beta A_v}} \quad \boxed{A_f = \frac{A}{1 + A\beta}}$$

Effect of input and output impedance with feedback:

$$Z_{in_f} = Z_{in} (1 + A\beta)$$

$$\checkmark \boxed{Z_{of} = \frac{Z_o}{1 + A\beta}}$$

Current amplifier (current-shunt)



Applying nodal at G/P:

$$I_s = I_i + I_f$$

$$\Rightarrow I_i = I_s - I_f$$

$$A_I = \frac{I_o}{I_i}$$

$$\beta = \frac{I_f}{I_o}$$

$$A_{If} = \frac{I_o}{I_s}$$

$$= \frac{I_o}{I_i + I_f}$$

$$= \frac{I_o / I_i}{1 + I_f / I_i}$$

$$= A_I$$

$$= \frac{1 + \frac{I_f \times I_o}{I_o / I_i}}{1 + \frac{I_f \times I_o}{I_o / I_i}}$$

$$A_{If} = \frac{A_I}{1 + \beta A_I}$$

S/P connection is shunt

so Z_{inf} decrease due to feedback

$$Z_{inf} = \frac{Z_{in}}{1 + AB}$$

O/P connection is series

so Z_{of} increases

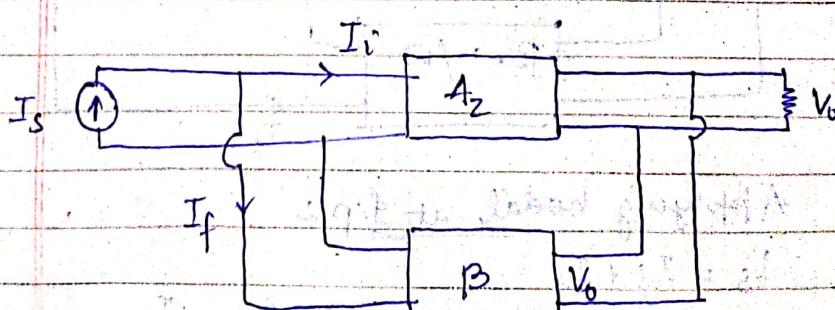
$$Z_{of} = (1 + AB) Z_o$$

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Transimpedance amplifier :-

S/P
Current
Shunt

O/P
Voltage
Shunt



$$A_Z = \frac{V_o}{I_i}, \quad B = \frac{I_f}{V_o}$$

$$A_{zf} = \frac{V_o}{I_s}$$

Applying nodal at S/P \Rightarrow

$$I_s = I_i + I_f$$

$$A_{zf} = V_o \cdot \frac{I_i + I_f}{I_i}$$

$$= \frac{V_o}{I_i} \cdot \frac{A + A_B}{1 + A_B}$$

$$\boxed{A_{zf} = \frac{A_Z}{1 + A_B}}$$

$$\Rightarrow A_{\text{eq}} \boxed{A_{zf} = \frac{A}{1 + A_B}}$$

$Z_{in} \downarrow, Z_{op} \downarrow$ (niedriges Z_{in} und hoher A)

$$Z_{in} = \frac{Z_{in, \text{biased}}}{1 + A_B}, \quad Z_{op} = \frac{Z_0}{1 + A_B}$$

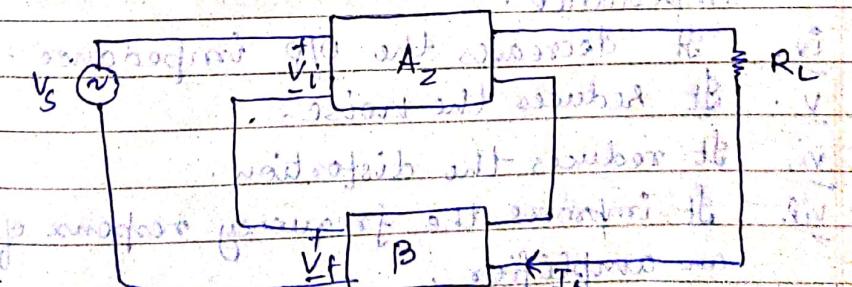
~~using $Z_{in} = Z_{in, \text{biased}} / (1 + A_B)$ and $Z_{op} = Z_0 / (1 + A_B)$~~

Transconductance amplifier \rightarrow Transistor

S/P (input) \rightarrow O/P (output)

Voltage to Current amplifiers \rightarrow Current source

Series input \rightarrow Series output



$$A_Z = \frac{V_f}{V_i}, \quad B = \frac{V_f}{I_o}, \quad A_{zf} = \frac{V_f}{V_S} \cdot \frac{I_o}{V_i}$$

$$V_S = V_i + V_f$$

$$A_{zf} = \frac{V_o}{V_i} = \frac{I_o}{V_i + V_f} \times \frac{V_f}{V_f}$$

$$= \frac{I_o / V_i}{1 + V_f / V_i}$$

$$= \frac{A_z}{1 + V_f / V_i} \times \frac{I_o}{V_i}$$

$$A_{zf} = \frac{A_z}{1 + \beta A_z}$$

$$Z_{in} \uparrow, Z_{in} = Z_{in} (1 + \beta A_z)$$

$$Z_{of} \uparrow, Z_{of} = Z_{of} (1 + \beta A_z)$$

~~Ques~~ # Advantages of Negative feedback -

- i. Negative feedback provides 'stable' gain, i.e., provides ~~unstable~~ o/p.
- ii. For any amplifier, product of gain and bandwidth is always constant.
$$\text{Gain} \times \text{BW} = \text{const}$$
- iii. Negative feedback enhances the bandwidth.
- iv. It decreases the o/p impedance.
- v. It reduces the noise.
- vi. It reduces the distortion.
- vii. It improves the frequency response of an amplifier.

Q. Determine the voltage gain, input and output impedance with feedback for voltage series feedback having $A = -100$, $R_i = 10\text{k}\Omega$, $R_o = 20\text{k}\Omega$ for feedback of -

$$(a) \beta = -0.1 \checkmark$$

$$(b) \beta = -0.5 \checkmark$$

$$\Rightarrow (a) A_{vf} = \frac{A}{1+Ap} = \frac{-100}{1+(100 \times 0.1)} = \frac{-100}{1+10} = \frac{-100}{11}$$

$$Z_{if} = Z_i(1+Ap)$$

$$= 10\text{k} \left[1 + (-100 \times -0.1) \right] \approx 10\text{k} [1+10] \quad | A = -100$$

$$= 110\text{k}\Omega$$

$$Z_{of} = \frac{Z_{o\text{out}}}{1+Ap}$$

$$= \frac{20\text{k}}{1 + (-100 \times -0.1)} = \frac{20\text{k}}{1+10} = \frac{20\text{k}\Omega}{11}$$

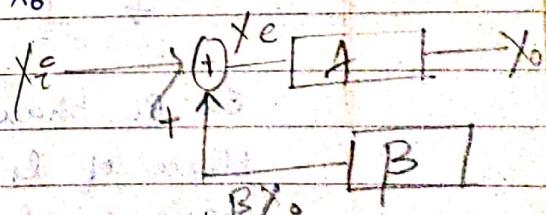
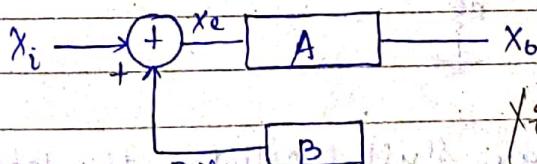
(b) Similarly for $\beta = -0.5$

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$(x_e \rightarrow \text{error signal})$

Positive feedback :-

$x_e \rightarrow \text{error signal}$



$$x_e = x_i + \beta x_o$$

$$x_o = Ax_e = A(x_i + \beta x_o)$$

$$= Ax_i + \beta Ax_o$$

$$\Rightarrow x_o - \beta Ax_o = Ax_i$$

$$\Rightarrow \frac{x_o}{x_i} = \frac{A}{1-AB}$$

~~Ques~~

Barkhausen's criterion (principle) for sustained oscillation:

$$\frac{X_B}{X_i} \rightarrow \infty$$

$$\Rightarrow 1 - A_{PB} = 0$$

$$\Rightarrow A_{PB} = 1 = 1 \angle 0^\circ$$

i. Magnitude of $A_{PB} = 1$

$$\Rightarrow |A_{PB}| = 1$$

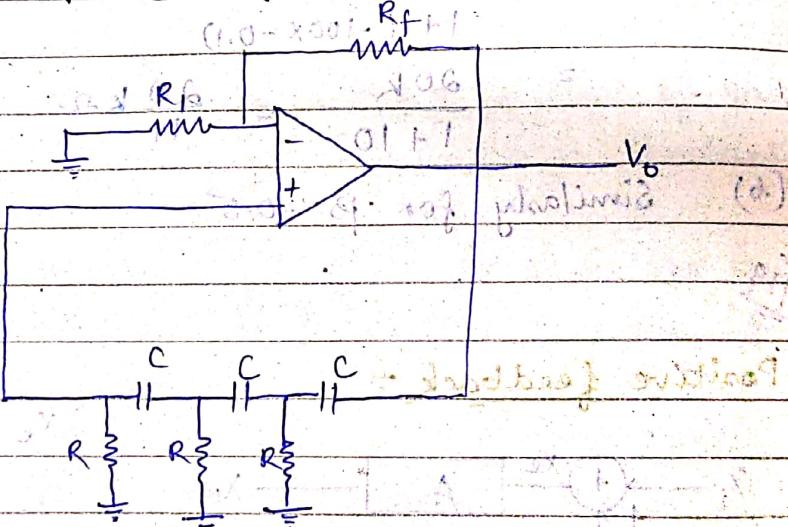
ii. Phase of $A_{PB} = 0^\circ$ or 360°

$$\angle A_{PB} = 0^\circ \text{ or } 360^\circ$$

NOTE: A_{PB} is called loop gain.

- for oscillator, we use positive feedback.

* # RC phase shift oscillator:

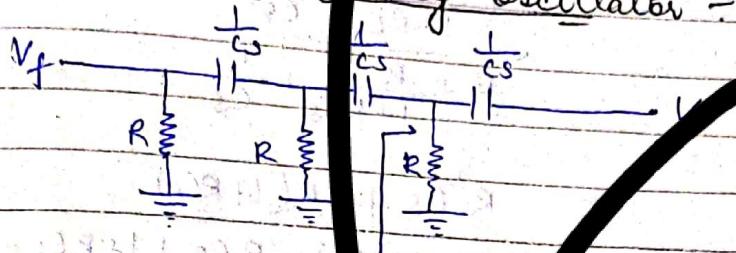


In RC phase shift oscillator, the total phase of loop gain is 360° and the basic amplifier produces 180° as phase shift and remaining 180° phase shift is produced by 3 section of RC (each section of RC produces 60° as phase shift).

To the oscillator, no i/p is applied but o/p to oscillator is noise which is automatically available.

$$\beta = \frac{V_f}{V_o}$$

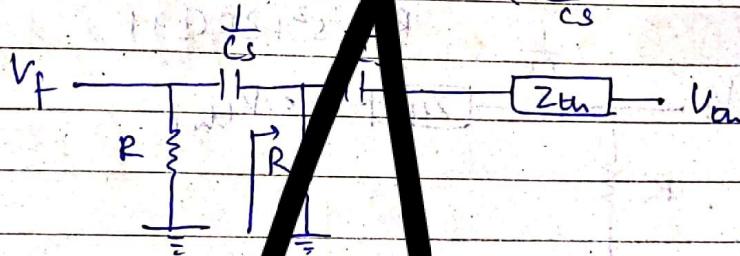
* Derivation of frequency of oscillator :



V_{th}

$$V_{th} = \frac{V_o \times R}{R + \frac{1}{Cs}} = V_o R C_s$$

$$Z_{th} = R \parallel \frac{1}{Cs} = \frac{R \times \frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{R}{1 + R C_s}$$



Z_{th}

G_m

$$V_{th_1} = \frac{V_{th} \times R}{(Z_{th} + \frac{1}{Cs}) + R}$$

$V_{th} \times R$

$$\frac{R}{1 + R C_s} + \frac{1}{Cs} + R$$

$$V_{th} \times R \times C_s (1 + R C_s)$$

$$R C_s + 1 + R + R C_s (1 + R C_s)$$

$$= V_{th} \cdot R C_s (1 + R C_s)$$

$$R^2 C_s^2 + R C_s + R C_s + R C_s + 1$$

$$V_{th} \cdot R C_s (1 + R C_s)$$

$$R^2 C_s^2 + 3 R C_s + 1$$

$$Z_{th1} = \left(Z_{th1} + \frac{1}{Cs} \right) // R$$

$$= \frac{R \left(Z_{th1} + \frac{1}{Cs} \right)}{R + Z_{th1} + \frac{1}{Cs}}$$

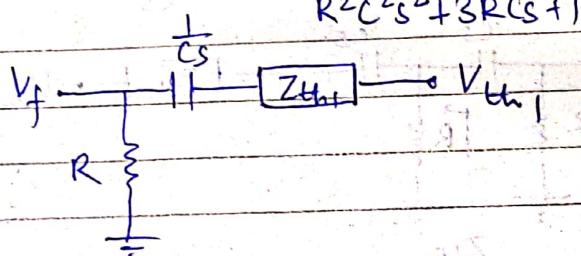
$$= \frac{R \left(\frac{R}{1+Rcs} + \frac{1}{Cs} \right)}{R + \frac{R}{1+Rcs} + \frac{1}{Cs}}$$

$$= \frac{R^2 Cs + R(1+Rcs)}{Cs(R+R^2 Cs) + Rcs + 1+Rcs}$$

$$= \frac{R^2 Cs + R + R^2 Cs}{Rcs + R^2 C^2 S^2 + 2Rcs + 1}$$

$$= \frac{2R^2 Cs + R}{R^2 C^2 S^2 + 3Rcs + 1}$$

$$= \frac{R(2Rcs + 1)}{R^2 C^2 S^2 + 3Rcs + 1}$$



$$V_f = \frac{V_{th1} \times R}{\frac{1}{Cs} + Z_{th1} + R}$$

$$= \frac{Rcs(1+Rcs)V_o Rcs \cdot R}{(R^2 C^2 S^2 + 3Rcs + 1)1+Rcs}$$

$$= \frac{\frac{1}{Cs} + R + R(2Rcs + 1)}{R^2 C^2 S^2 + 3Rcs + 1}$$

$$= \frac{V_o R^3 C^2 S^2}{R^2 C^2 S^2 + 3Rcs + 1 + Rcs(R^2 C^2 S^2 + 3Rcs + 1)}$$

$$= \frac{V_o R^3 C^2 S^2}{R^2 C^2 S^2 + 3Rcs + 1 + R^2 C^2 S^2 + 3Rcs + Rcs(2Rcs + 1)}$$

$$= \frac{V_o R^3 C^2 S^2}{R^2 C^2 S^2 + 3Rcs + 1 + R^3 C^3 S^3 + 3R^2 C^2 S^2 + Rcs \cdot 2R^2 C^2 S^2 + Rcs}$$

$$\Rightarrow V_f = - \frac{V_o R^3 C^2 s^2 \cdot C_s}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1}$$

$$= \frac{V_o R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1}$$

putting $s = j\omega$, $s^2 = -\omega^2$, ~~$s^3 = -j\omega^3$~~

$$\begin{aligned} \beta = \frac{V_f}{V_o} &= \frac{R^3 C^3 s^3}{R^3 C^3 s^3 + 6R^2 C^2 s^2 + 5RCs + 1} \\ &= \frac{-j R^3 C^3 \omega^3}{-j R^3 C^3 \omega^3 - 6R^2 C^2 \omega^2 + j 5RC\omega + 1} \\ &= \frac{R^3 C^3 \omega^3 + 6j R^2 C^2 \omega^2 - 5RC\omega + j}{R^3 C^3 \omega^3 + 6R^2 C^2 \omega^2 - 5RC\omega + 1} \end{aligned}$$

for freq. of oscillation =

$$B_{inj} = 0$$

$$6j R^2 C^2 \omega^2 + 1 = 0$$

$$\omega^2 = \frac{1}{6R^2 C^2}$$

$$\Rightarrow \omega = \sqrt{\frac{1}{6R^2 C^2}}$$

$$\Delta = \sqrt{6R^2 C^2}$$

$$\therefore f_r = \frac{1}{\Delta}$$

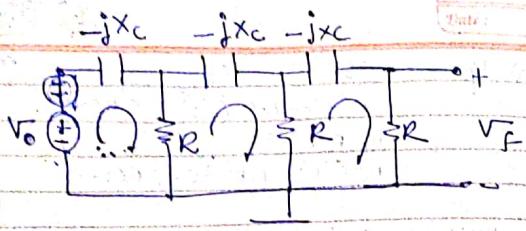
$$\Delta = (\sqrt{3}X - 2\pi RC)\sqrt{6}$$

X Condition for oscillation:

$$A_{B\text{ real}} = 1$$

$$\Rightarrow R_f = 2g R_i$$

$$A = \frac{R_f}{(g R_i X)} = \frac{(g R_i X)}{(g R_i X) - (g R_i X)}$$



$$V = IR$$

$$\Rightarrow \begin{bmatrix} R - jX_C & -R & 0 \\ -R & 2R - jX_C - R & 0 \\ 0 & -R & 2R - jX_C \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_0 \\ 0 \\ 0 \end{bmatrix}$$

$I_3 = \frac{\Delta_2}{\Delta}$

$$\Rightarrow (R - jX_C) \left\{ (2R - jX_C)^2 - R^2 \right\} + R \left\{ -R(2R - jX_C) - 0 \right\} = \Delta$$

$$\Rightarrow (R - jX_C) \left\{ 4R^2 + (-1)X_C^2 - j4RX_C - R^2 \right\} + \left\{ -2R^3 + jX_C R^2 \right\} = \Delta$$

$$\Rightarrow 4R^3 - X_C^2 R - j4R^2 X_C - R^3 - j4R^2 X_C + jX_C^3 + (-1)jRX_C^2 + jX_C R^2 - 2R^3 + jX_C R^2 = \Delta$$

$$\Rightarrow R^3 - 5RX_C^2 - jRX_C R^2 + jX_C^3 = \Delta$$

$$\Rightarrow (R^3 - 5RX_C^2) - j(6X_C R^2 - X_C^3) = \Delta \quad \text{---(1)}$$

$$\Delta_3 = V_0 R^2$$

$$V_f = I_3 \times R$$

$$= V_0 R^3$$

$$(R^3 - 5RX_C^2) - j(6X_C R^2 - X_C^3)$$

$$6X_C R^2 = X_C^3$$

$$\frac{X_C^2}{R^2} = 6 \Rightarrow X_C = \sqrt{6}R$$

$$\omega_{nfc}$$

$$f = \frac{1}{2\pi\sqrt{RC}}$$

$$V_f = \sqrt{V_0 R^3}$$

$$\Rightarrow \beta = \frac{R^3 - 5RX_C^2}{1}$$

$$= \frac{1}{1 - 5X_C^2/R^2} = \frac{1}{1 - 5 \times 6} = -\frac{1}{29}$$

$$|AB| = 1$$

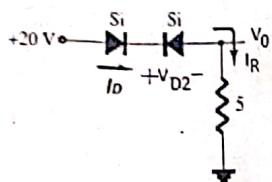
$$|A| = \frac{1}{29} \left| \frac{1+29}{1-1} \right| = 29$$

Duration: 01:30

Full Marks: 25

1 Answer All

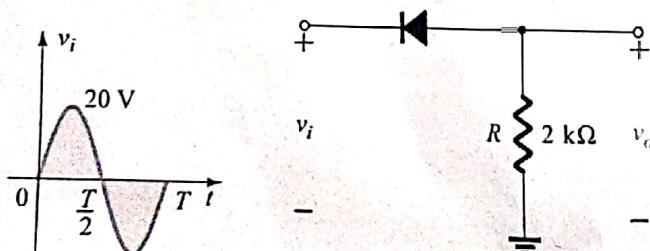
- a* State under which biasing condition PN Junction diode behaves as ON switch and justify it. 1
- b A transistor has an emitter current of 10 mA and a collector current of 6.5 mA. Calculate its base current. 1
- c What is the PIV rating of a diode? 1
- d Explain why a transistor should be biased. 1
- e Determine I_D , V_{D2} , and V_o for the circuit given below. 1



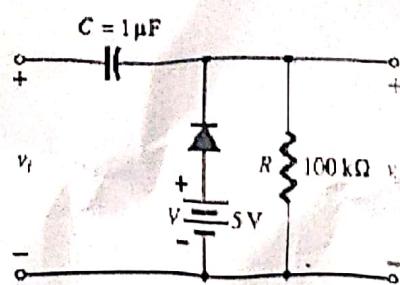
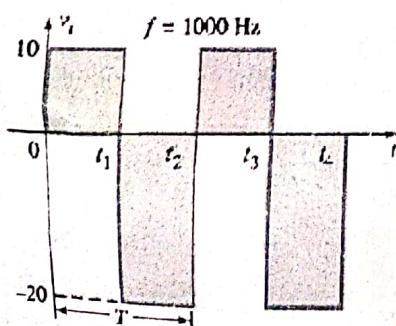
2 Answer any Two

- a* With a neat diagram calculate the PIV rating of a diode of a bridge rectifier and that of a center-tap rectifier. Find the relationship between the two PIVs. 2

- b Sketch the output v_o and determine the dc level of the output for the network (i) The diode is an ideal diode (ii) Recalculate with a Silicon diode 2



- c Determine v_o for the network shown below with the input indicated. 2



[P. T. O.]

3 Answer any Two

- a If the emitter current of a transistor is 8 mA and I_B is 1/100 of I_C , determine the values of I_C and I_B . 2

- b The reverse saturation current of an NPN transistor in common base is $12.5 \mu A$. For an emitter current of 2 mA, the collector current is 1.97 mA. Determine the current gain and base current. 2

- c Draw the fixed bias circuit and write down the expression for I_B , V_{CE} . 2

4 Answer any Two

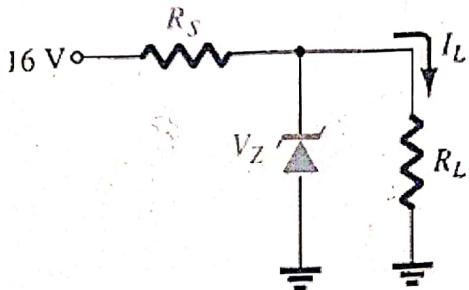
- a With a neat diagram, explain the working principle of a PN junction diode. Draw the V-I characteristics of it. 4

- b For half-wave rectification, a crystal diode of internal resistance $r_f = 10 \Omega$ is used. If the applied voltage $v = 30 \sin \omega t$ and load resistance $R_L = 750 \Omega$: 4

(i) I_m , $I_{d.c.}$, I_{rms}

(ii) Efficiency of Rectification

- c For the network shown, the load current (I_L) varies from 0 mA to 200 mA. Determine R_S and V_Z (Zener breakdown voltage) such that the load voltage V_L is maintained at 12 V. 4



5 Answer any One

- a Compare the characteristics of transistors in different configurations. 4

- b From the given information in the figure below determine 4

- (a) I_C , (b) R_C , (c) R_B , (d) V_{CE} .

