Square Wave Generator with Variable Frequency

Special Assignment and Lab Project Report

2EC202CC23 - FPGA based System Design

Submitted by:

23BEC173 [Nishit Satapara]

Department of Electronics and Communication Engineering,
Institute of Technology,
Nirma University,
Ahmedabad 382 481

[March - 2025]

1.Abstract

Abstract

In digital and analog systems, a square wave generator is a fundamental circuit used for signal processing, pulse-width modulation (PWM), and clock generation. Using a Finite State Machine (FSM), this project generates a square wave generator that lets the frequency fluctuate according to input data. Verilog HDL is used to write the circuit, which may be tested using an FPGA or simulators such as ModelSim. Applications requiring flexible frequency adjustment can benefit from the fine control that FSM provides over the wave's ON and OFF times.

2.Introduction

A square wave generator is a crucial component in digital electronics, utilized for various applications such as producing clock signals, generating pulses, and managing different digital devices. Square waves find extensive use in microcontrollers, communication systems, and signal processing.

This project aims to develop a variable frequency square wave generator through Finite State Machine (FSM) modeling in Verilog. Unlike conventional methods such as 555 timers or microcontrollers, this design offers enhanced frequency control and is particularly suited for FPGA applications.

The primary objective is to construct a programmable waveform generator that allows users to define the ON time (P_ON) and OFF time (P_OFF). By adjusting these parameters, the frequency of the square wave can be modified as required. The system employs a state-based methodology, ensuring that the waveform generation process is both straightforward and efficient.

This report details the FSM design, including the state diagram, flowchart, operational method, and the limitations of existing technologies. The project is executed in Verilog HDL, and the resulting waveform can be evaluated using simulators such as ModelSim or on actual hardware like FPGA boards.

Incorporating FSM into this design enhances the accuracy, flexibility, and control of the square wave generator compared to traditional circuits.

3.Keywords

Square Wave Generator, Finite State Machine, Verilog, FPGA, Digital Signal Processing, Clock Generation, Variable Frequency.

4.Literature Survey

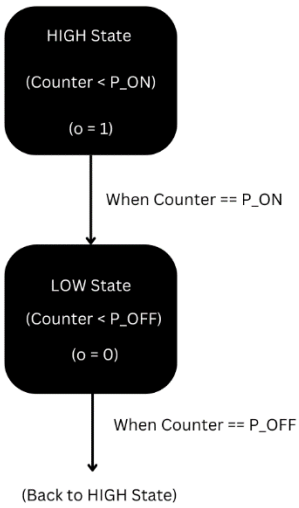
Square wave generators are usually built using timers, microcontrollers (like Arduino, 8051), or digital circuits.

Traditional methods, such as 555 timers and microcontrollers, can generate square waves, but they do not provide accurate frequency control unless extra components are used.

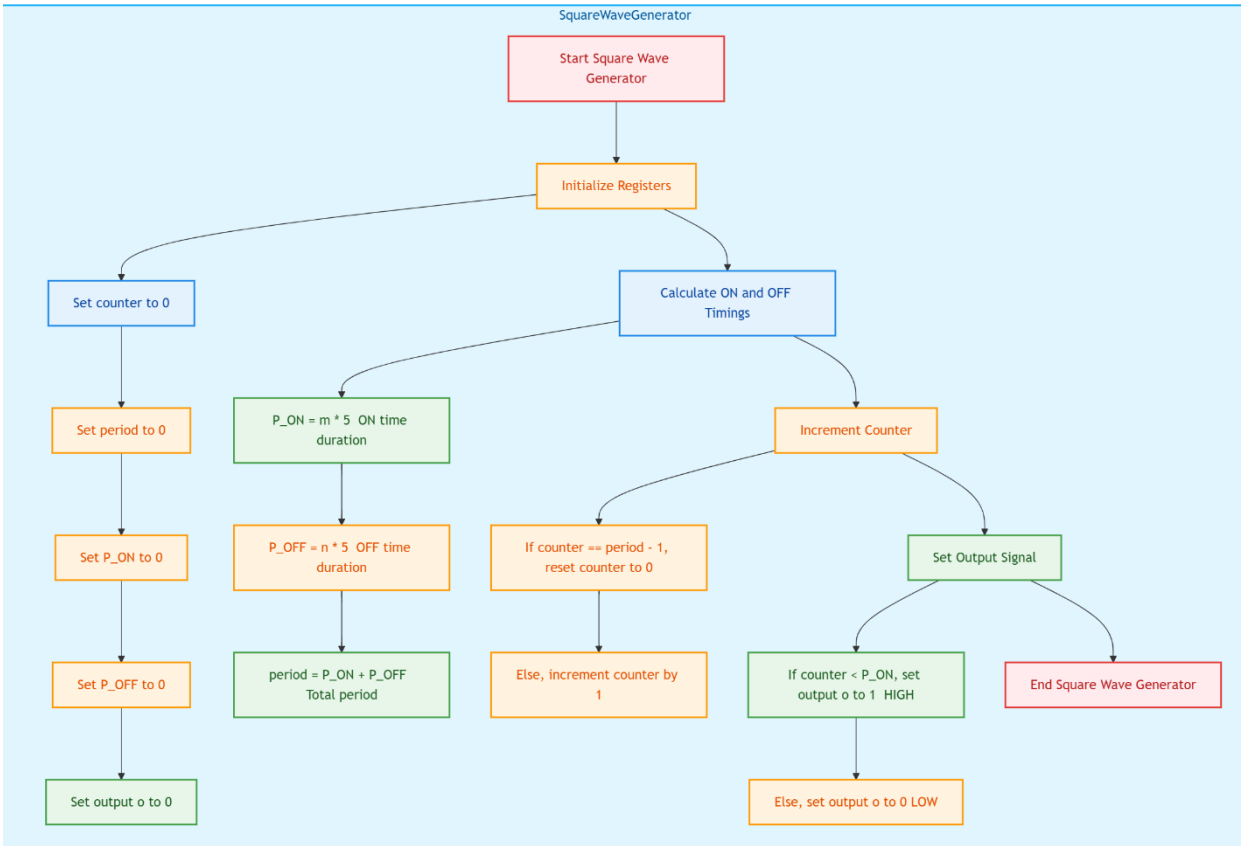
In this project, the Finite State Machine (FSM) approach is used to control the waveform systematically. This method ensures better frequency accuracy and makes the design more suitable for digital applications.

Studies have shown that using FSM on FPGA for waveform generation gives higher precision and more flexibility compared to software-based techniques.

5.Block Diagram & Circuit Diagram



6.Flow Chart



7. LIMITATIONS OF CURRENTLY AVAILABLE TECHNOLOGY

1. Fixed Frequency Output:
Traditional square wave generators (555 timers, fixed-frequency clocks) do not provide easy frequency adjustment.
2. Lack of FSM Modeling:
Many designs use direct combinational logic without FSM, reducing flexibility.
3. Higher Power Consumption:
Some microcontroller-based solutions continuously run in a loop, consuming more power.
4. Limited Digital Control:

Analog-based waveform generators require additional components for precise frequency control.

8. METHODOLOGY (Finite state machine modeling)

The square wave generator is modeled using a Finite State Machine (FSM) with two primary states:

1. **HIGH State:** The output remains HIGH (o = 1) for P_ON cycles.
2. **LOW State:** The output remains LOW (o = 0) for P_OFF cycles.

The FSM transitions between these states based on a counter that tracks the ON and OFF durations.

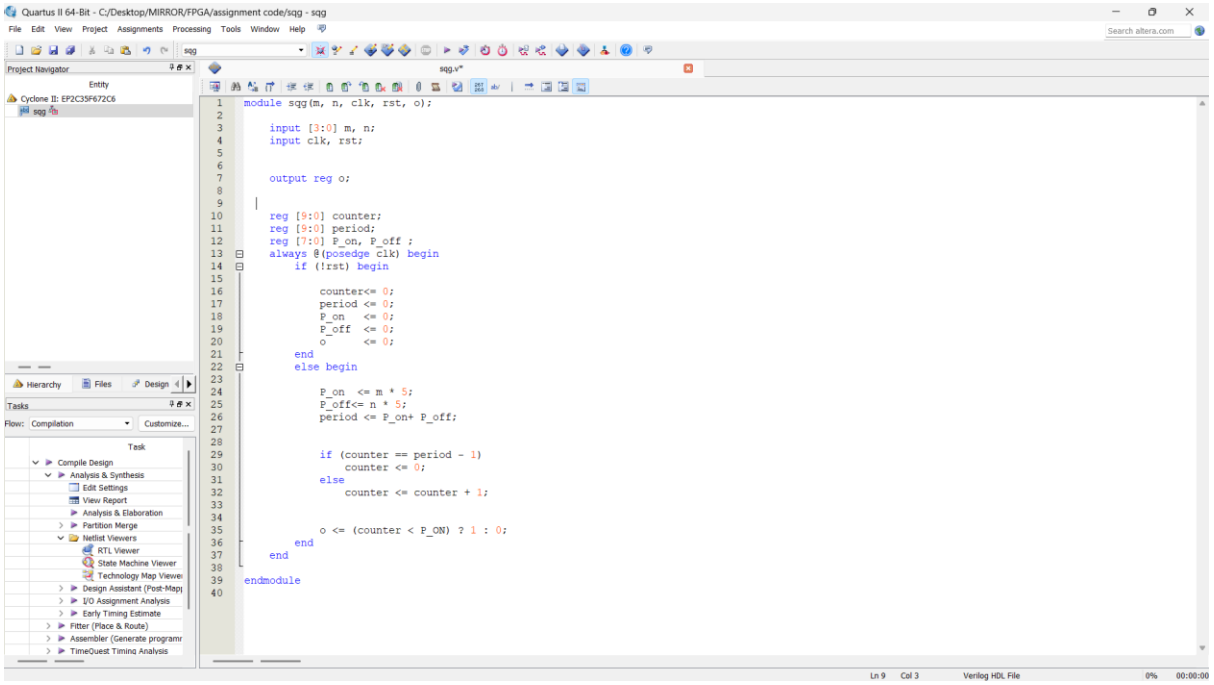
The design is implemented using Verilog HDL and simulated for various values of `m` and `n`, where:

- P_ON = m * 5 (on time)
- P_OFF = n * 5 (off time)
- Period = P_on+ P_off

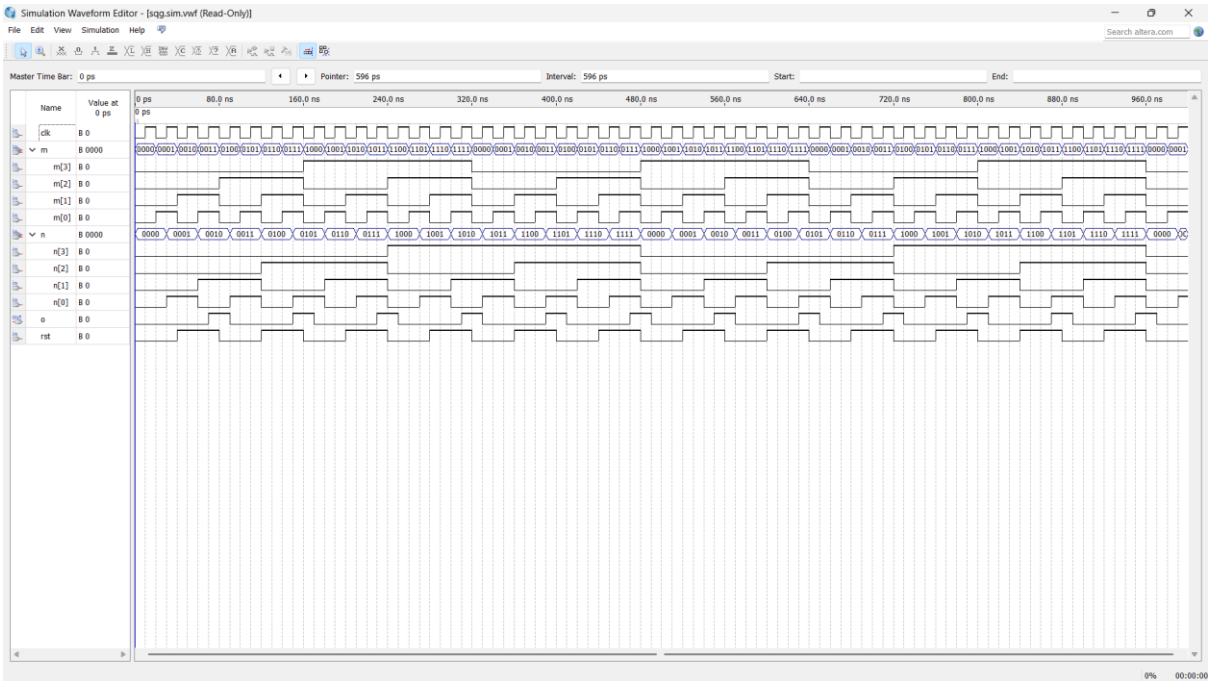
9. Conclusion

This project successfully uses FSM modeling to produce a square wave generator with an adj ustable frequency.
The FSM approach is more dependable than traditional methods because it provides precise c ontrol over the waveform.
The architecture is highly suited for digital signal processing and FPGA applications because it is implemented in Verilog.
Future improvements might incorporate duty cycle management and allow for user-inputted real-time frequency modifications.

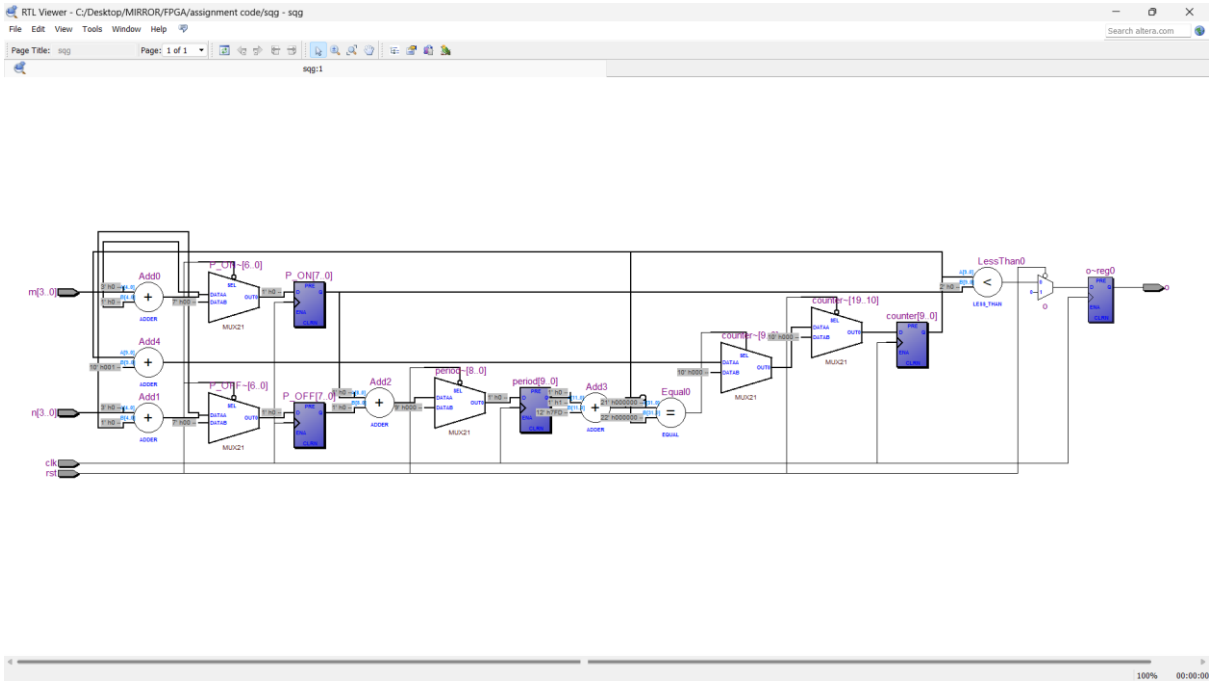
10. Code



11. waveforms



12. simulation-RTL



13. TTL