CERTIFICATE

OF COMPLETION

PV1124D0054 **March 15, 2025**

This is to certify that

KARRI NISHITHA

has successfully attended and completed the 3 Day Advanced SystemVerilog and UVM Verification Workshop, gaining hands-on experience in:

- *SystemVerilog Testbench Development*
- *Coverage-Driven Analysis*
- *Assertion-Based Verification*
- *Protocol Verification at SoC & IP Level*

Presented with recognition of dedication and excellence in VLSI Verification.

Prasanthi Chanda
Founder & CEO of ProV Logic