EC 311: PROJECT

TOPIC 5: DIGITAL CLOCK

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INTRODUCTION

Implemented of a **24-hour digital clock** (HH:MM:SS) displayed on the FPGA 7-segment display.

Extra Credit: A switch that moves from 24-hour clock display **to 12-hour clock display.**

INPUTS

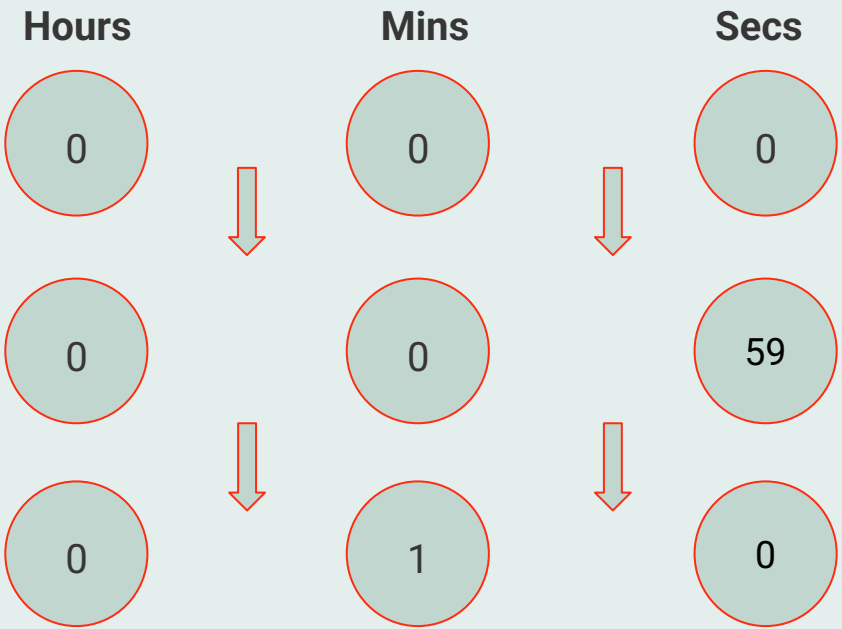
1. 1 Hz clock (**clk**)
2. Reset (**rst** to 00:00:00) button
3. **clock_select** (switch 24->12 or 12->24)

OUTPUTS

1. Cathode (7 bits) for FPGA
   7-segment display

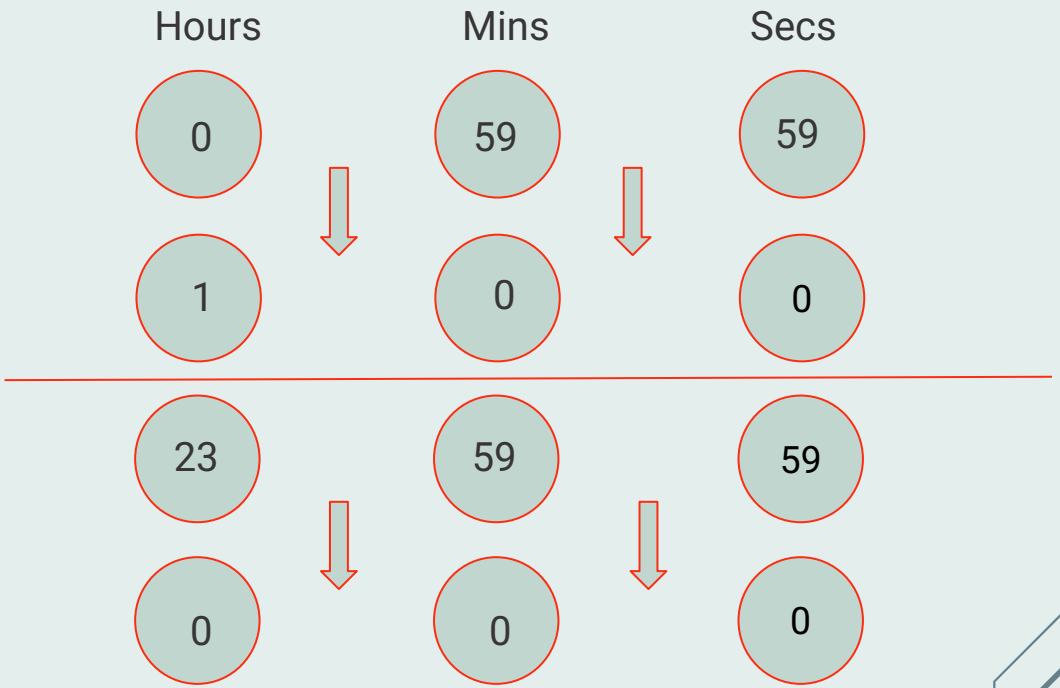
STATE DIAGRAM

24-hour clock

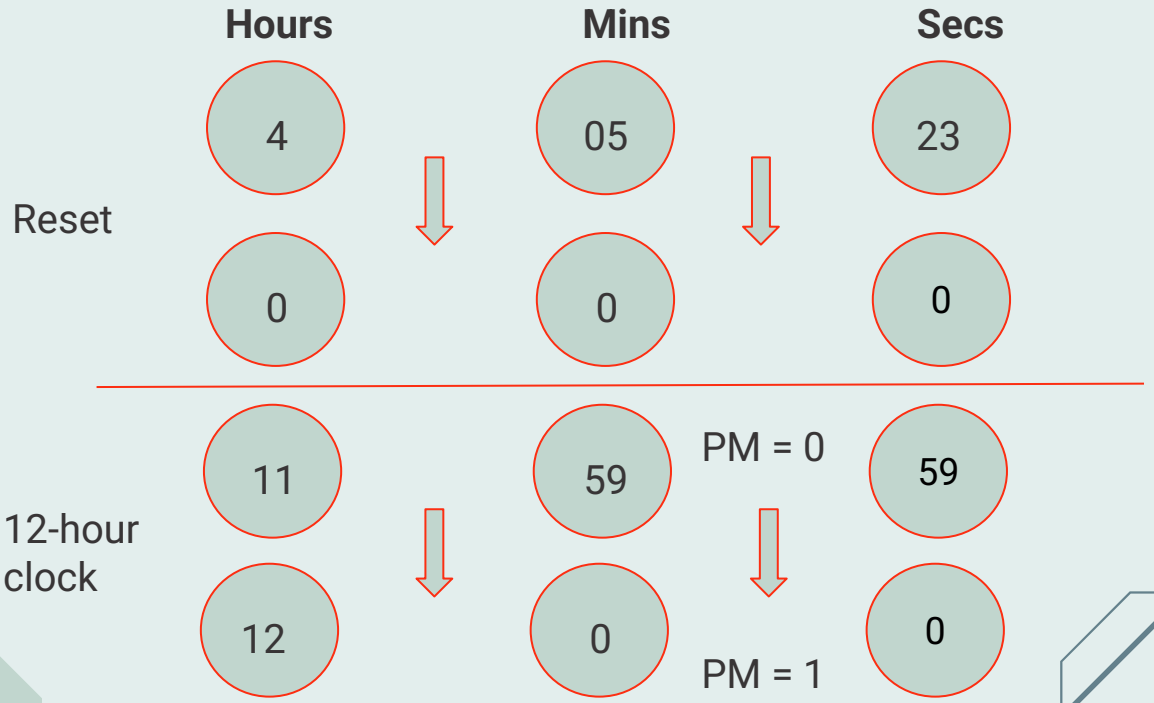


STATE DIAGRAM

24-hour clock



STATE DIAGRAM



CONCEPTS USED

1. Clk_divider
2. Combinational logic
3. Sequential logic
4. BCD, binary, decimal
5. Decoder

IMPLEMENTATION STEPS

01

clk_divider

Using appropriate parameter toggle_values

02

counter logic + reset logic

Incrementing HH:MM:SS and resetting to 00:00:00

03

conversion logic

24-hour to 12-hour switch + AM/PM addition

04

7-segment display logic

anode + cathode

UNIQUE IMPLEMENTATIONS

01

conversion

Instantiating both 12-hour and 24-hour clocks in a top conversion module

02

AM/PM for 12-hour

Including an indicator for AM(0) and PM(1) for the 12-hour clock

CHALLENGES

01

clk_divider

100MHz (default) and 25MHz (FSM) clock

02

FPGA

Implementing the 7-segment display

03

conversion

Converting between 24-hour and 12-hour clocks

THANK YOU!