Lab-4 (6th and 7th September)

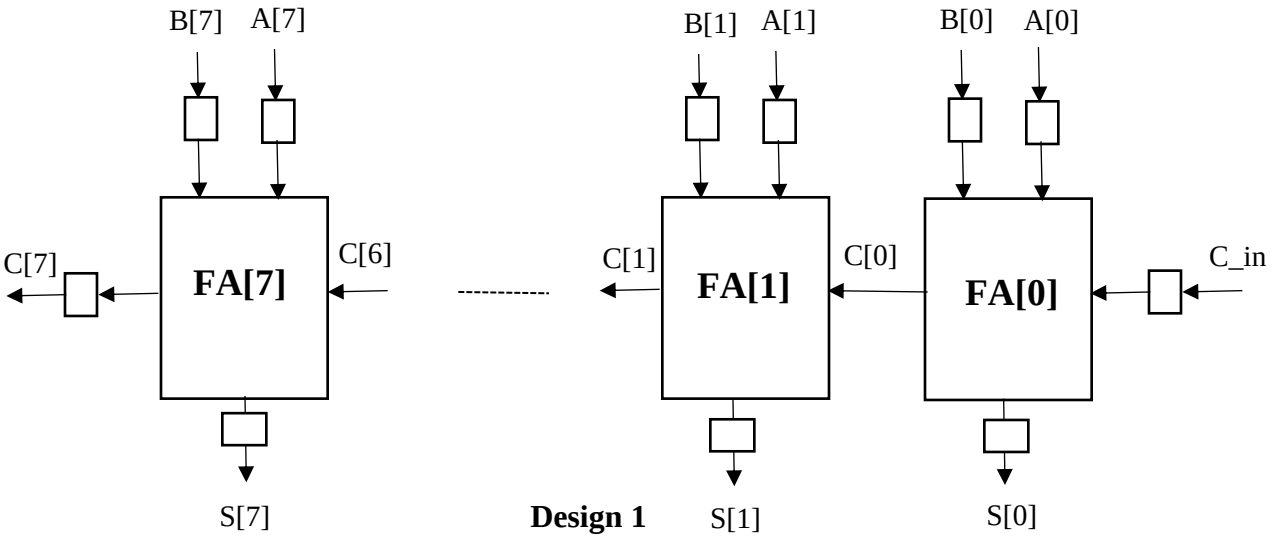
ECE270 - Embedded Logic Design

Tasks to be performed in this lab with homework

Board: Basys 3 Board, Xilinx Artix – 7 FPGA (XC7A35T-1CPG236C)

PART 1: Pipelining

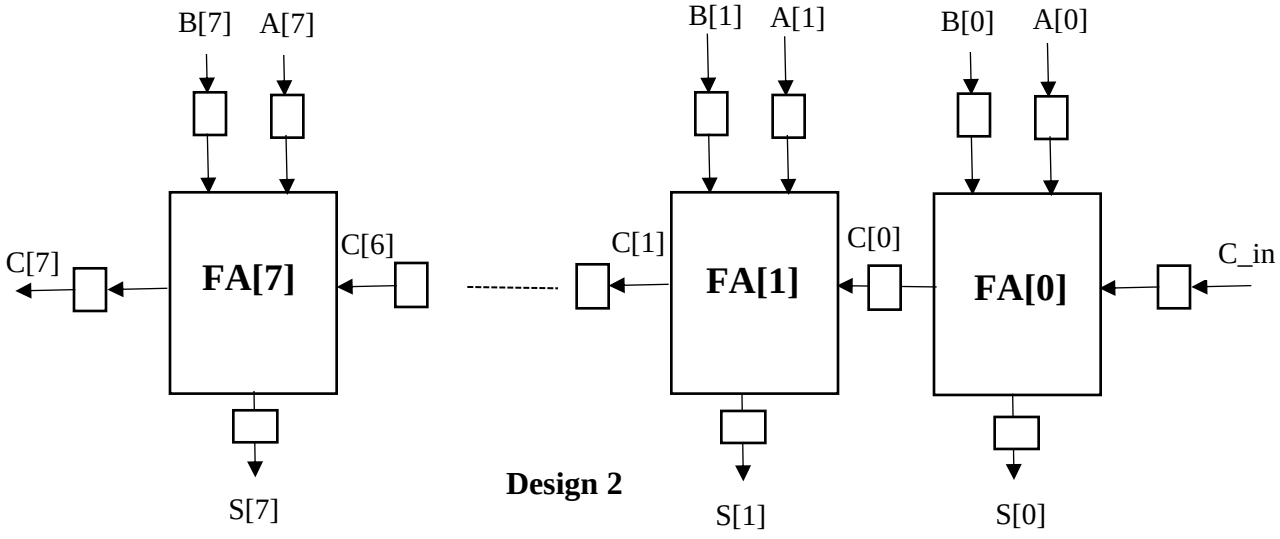
1. Design and implement an 8-bit full adder. Pass both 8-bit inputs and outputs through flip flops.



Design 1

2. With the help of timing constraints, determine the maximum clock frequency of design 1 that meets timing constraint.

3. Introduce the pipelining in the design 1 by placing the flip flops at the input of each Carry.

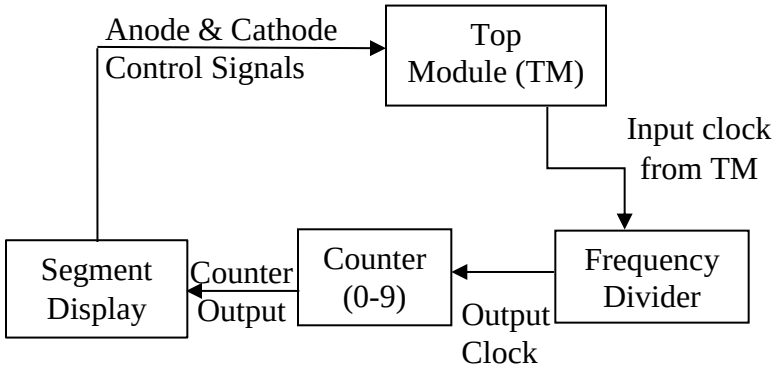


Design 2

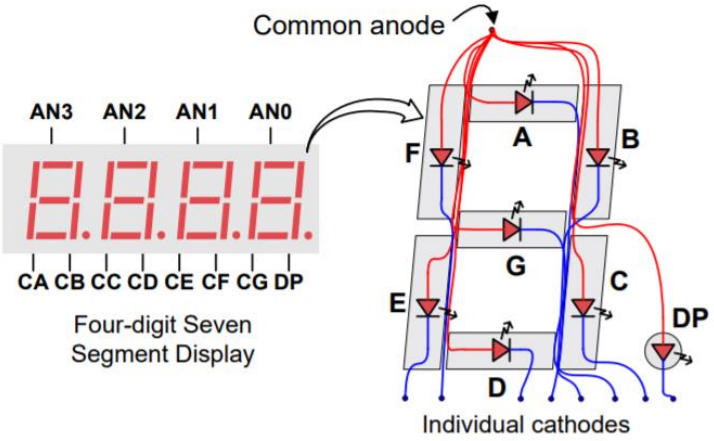
4. Determine the maximum clock frequency of design 2 that meets the timing constraints. Compare it with design 1.

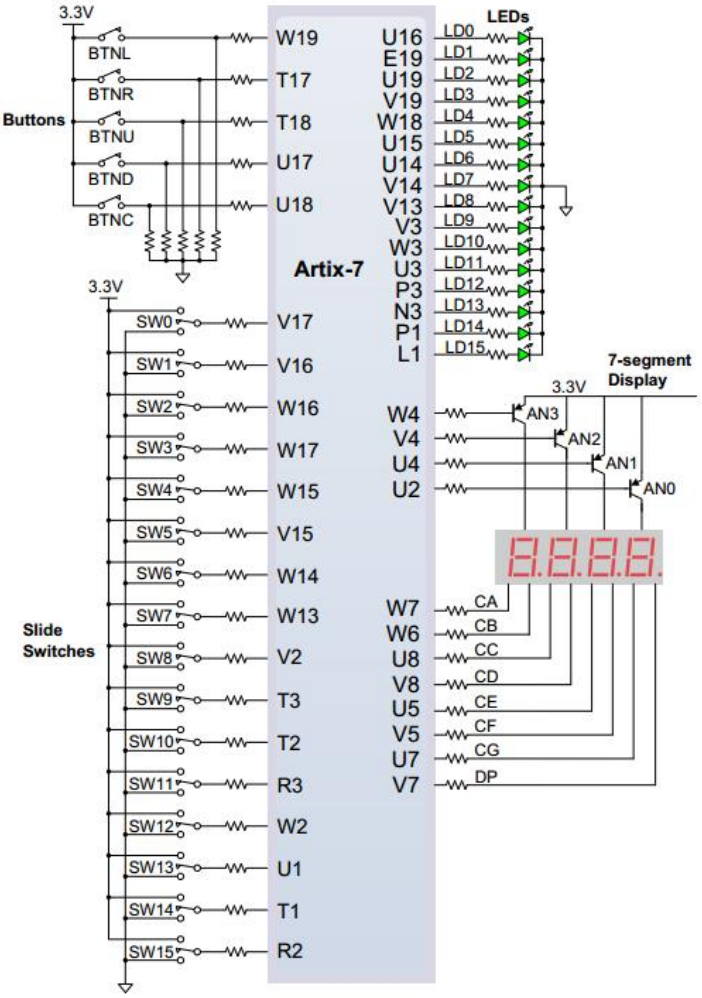
PART 2: Seven Segment Display

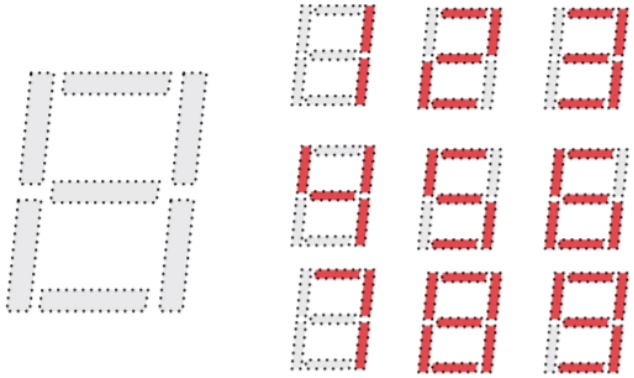
5. Design a counter that counts from 0 to 9. Display the count on seven segment display of Basys 3 board. Note that frequency divider will divide the input clock by 2^25.



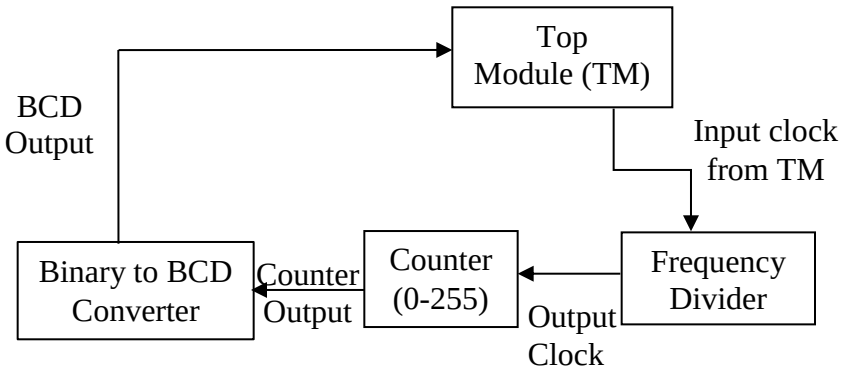
7-Segment Display





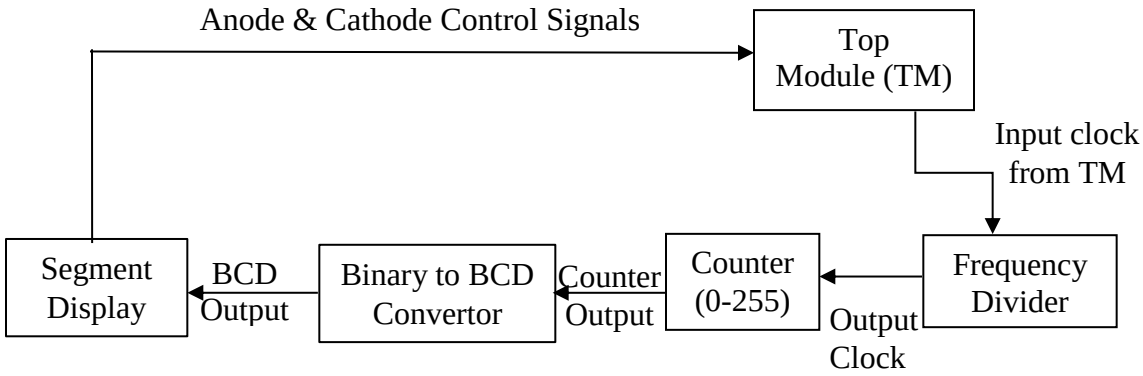


6. Design and implement an 8-bit binary to BCD converter. Note that frequency divider will divide the input clock by 2^25.



Reference: http://www.tkt.cs.tut.fi/kurssit/1426/S12/Ex/ex4/Binary2BCD.pdf

7. Design a counter that counts from 00000000 to 11111111. Convert this 8-bit binary number to a BCD number. Display the count from 0 to 255 on the seven segment display. Note that the frequency divider will generate a clock of 1Hz. (Hint: Use time multiplexing to display different digits at different decimal position.)



Reference: https://reference.digilentinc.com/_media/basys3:basys3_rm.pdf