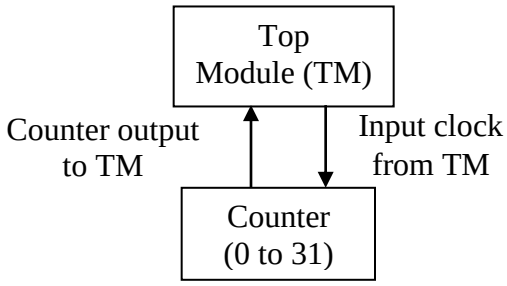
Lab-3 (28th and 30th August)

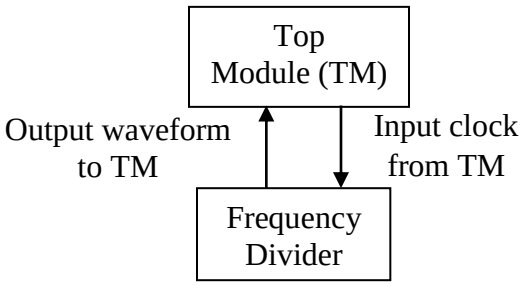
ECE270 - Embedded Logic Design

Tasks to be performed in this lab with homework

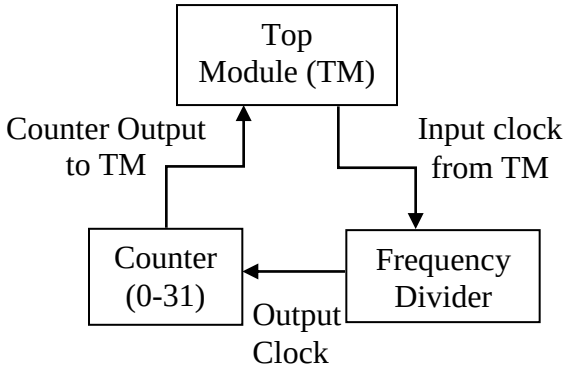
1. Design and implement a counter that count continuously from 0 to 31. Input clock should be taken from zedboard and output of a counter should be displayed on the LEDs.



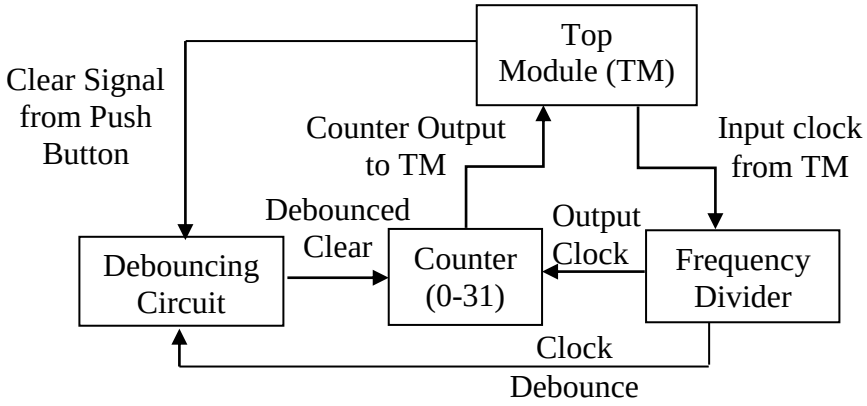
2. Design and implement a frequency divider on the Zedboard. Input clock frequency needs to be taken from the Zedboard which works at a rate of 100MHz. The frequency of the output waveform should be 2^25 times lower than the clock frequency of Zedboard.



3. Design and implement a counter on the Zedboard. The counter should count continuously from 0 to 31 at frequency generated in question 2. Display the output of the counter on the LEDs



4. Generate a clear signal to clear the counter designed in the previous step. The clear signal should be generated by a push button. Note that the push button has bouncing characteristics, i.e. single press appears to be multiple presses. You need to design a debouncing circuit for the clear signal and implement the above counter for the debounced clear signal.



5. Design and implement a counter on Zedboard. The counter should continuously count from 0 to 31. The output of the counter can be displayed on the LEDs of Zedboard at a rate of 1, 2, 4 or 8 seconds. The speed is to be decided by the user (use switches for this task). The counter should be able to clear itself whenever the clear button is pressed.

   (Hint: First calculate how many clock cycles will be required to generate a clock of 1 second by using the default clock of Zedboard. Then use the 1 second clock to generate clocks with lower frequency).