Lab-5 (13th and 14th September)

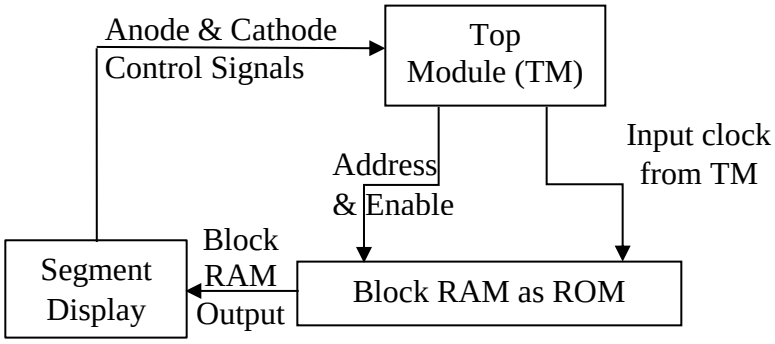
ECE270 - Embedded Logic Design

Tasks to be performed in this lab with homework

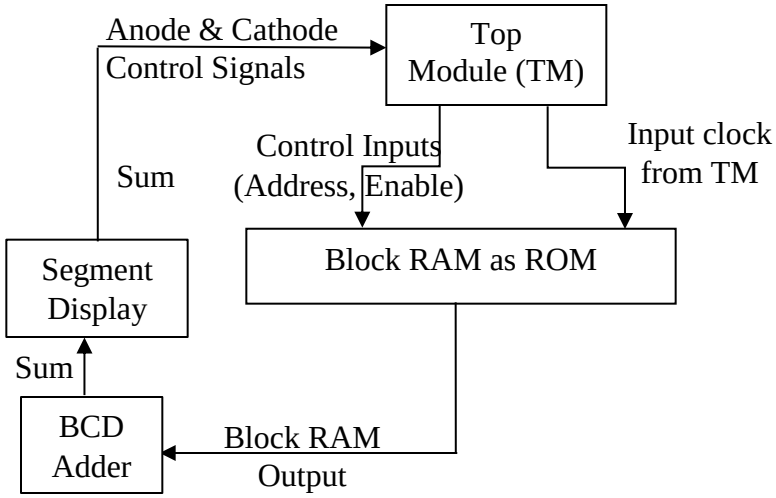
Board: Basys 3 Board, Xilinx Artix – 7 FPGA (XC7A35T-1CPG236C)

1. Write a testbench for a counter that counts from 0 to 100.

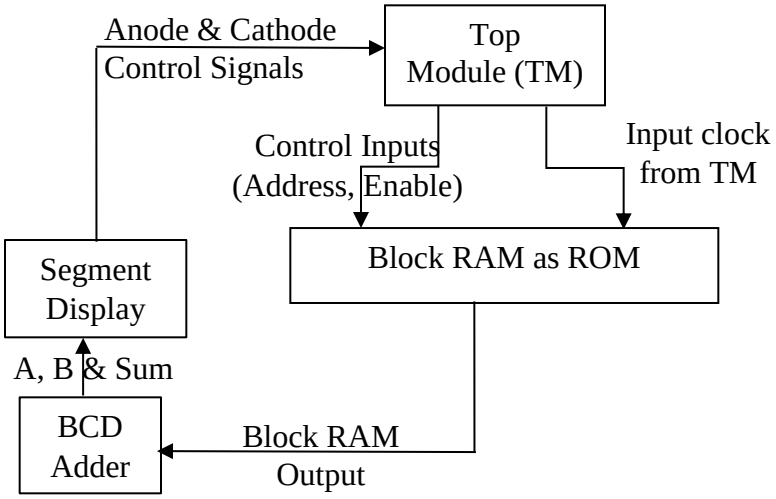
2. Design a ROM using Block RAM. Display the contents of the ROM on the seven segment display one-by-one. The ROM is storing numbers from 0 to 9.



3. Design and implement a BCD adder. The numbers to be added are stored in the ROM. Display the sum and contents of the ROM on the LEDs. Also display ones digit on the 7-segment display.



4. Design and implement a BCD adder which adds two numbers A and B ranging from 0 to 9. Display A on the rightmost digit of the 7 segment display and B on the leftmost digit. Output of the BCD adder should be displayed on the middle two digits of 7-segment display.



5. Design an 8-bit SIPO shift register. Shift the binary data into the shift register using 2 push buttons. One push button passes 0 and another passes 1. Display the content of shift register on the seven segment display in the BCD format.