Lab-8 (11th and 12th September)

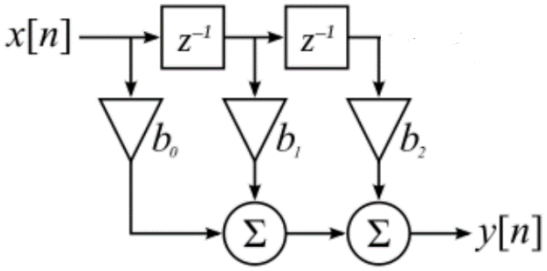
ECE270 - Embedded Logic Design

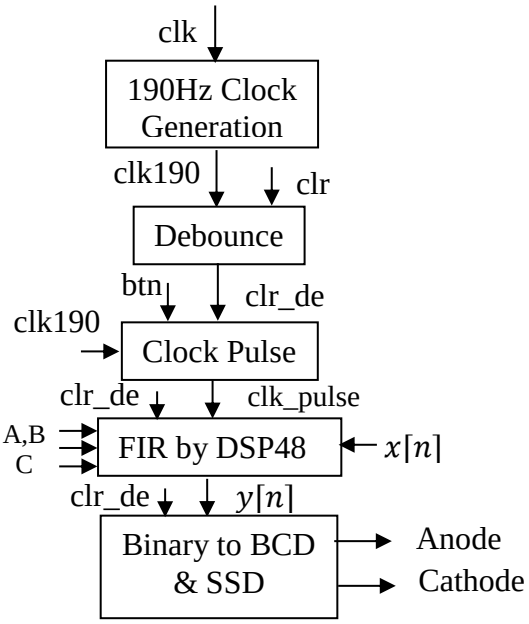
Tasks to be performed in this lab with homework

Board: Basys 3 Board, Xilinx Artix – 7 FPGA (XC7A35T-1CPG236C)

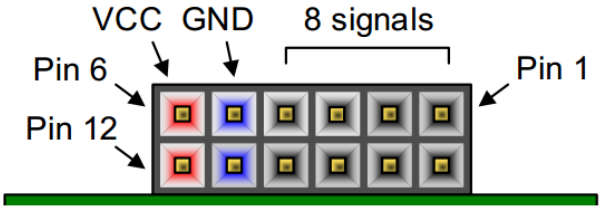
1. Design and implement a 3-tap FIR filter with following specifications:
   - The value of $x[n]$ is to be taken from switches, sw[2:0].
   - To perform addition operation, the weights b_0, b_1 and b_2 are taken as 1. Therefore, $y[n] = x[n] + x[n-1] + x[n-2]$
   - The flip flops should work on a clock pulse.

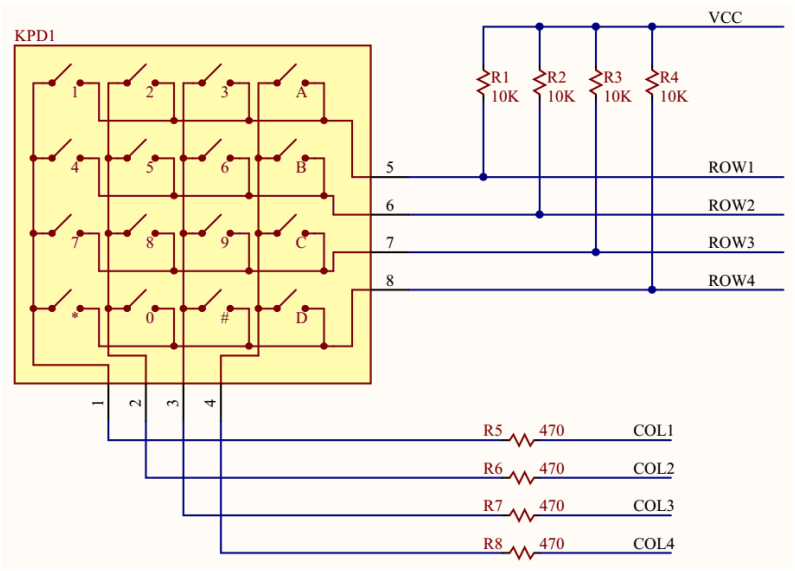
   Convert the output, $y[n]$ to the BCD format and display it on 7-segment display.

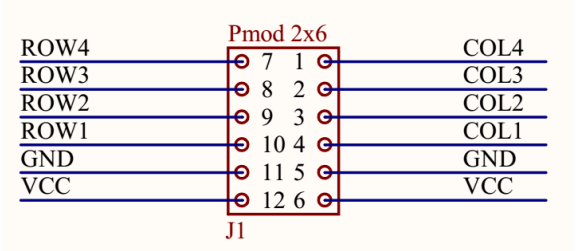




2. Write a Verilog code which connects Keypad to Basys3 board via PMOD and displays the key press on the 7 segment display.







3. Write a Verilog code which connects a keypad and external 7 segment display to the Basys 3 board via PMOD ports. Instead of using switches in Ques. 1, use the key press on the keypad to enter the value of $x[n]$ that ranges from 0 to 9. Display the output $y[n]$ to an external 7-segement display.

Hint: https://reference.digilentinc.com/reference/pmod/pmodssd/reference-manual