LAB 9 -10
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TOP

```
`timescale 1ns / 1ps

module top(
    input [5:0] x_in,
    input [5:0] y_in,
    input pushbutton,
    input clk,
    input clr,
    output reg [7:0] cathode1,
    output reg [3:0] anode1,
    output reg [6:0] cathode2,
    output reg anode2,
    output  reg done
);

    wire [5:0] x_in,y_in;
    wire [3:0] onesx,tensx,hundredsx;
    wire [3:0] onesy,tensy,hundredsy;
    wire [3:0] onesz,tensz,hundredsz,anodea,anodeb,anodec;
    wire [7:0] cathodea,cathodeb,cathodec,cathoded;



    assign anodea=4'b1110;
    assign anodeb=4'b1101;
    assign anodec=4'b1011;
    assign anoded=4'b0111;
    initial
    begin
    assign cathode1 = cathodea;
    end

    debounce d1 (clk,clr,clr_out);

    fd #19 f1(clk,clk19);
    clean_pulse cp1 (clk19,pushbutton,inpclk);
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```
wire [7:0] x,y;
assign x = {2'b00,x_in};
assign y = {2'b00,y_in};

b2b b1 (x,onesx,tensx,hundredsx);
b2b b2 (y,onesy,tensy,hundredsy);

seven_segment s1 (onesx,cathodea);
seven_segment s2 (tensx,cathodeb);
seven_segment s3 (onesy,cathodec);
seven_segment s4 (tensy,cathoded);

reg [5:0] gcd;
reg [5:0] xs, ys;

always @(posedge clk or posedge clr_out)
begin
   if (pushbutton == 1)
   begin
      xs = x_in;
      ys = y_in;
      done = 0;
   end
   else if (clr_out == 1)
   begin
      xs=6'b000000;
      ys=6'b000000;
      done = 0;
   end
   else
   begin
      if(xs==0||ys===0)
         begin
         gcd = xs + ys;
         done = 1;
         end
      else if (xs < ys)
      begin
         ys = ys - xs;
      end
      else if (xs > ys)
      begin
         xs = xs - ys;
```

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        end
        else
        begin
            gcd = xs;
            done = 1;
        end
    end
end

wire [7:0] gcd1;
assign gcd1 = {2'b00,gcd};
b2b b3 (gcd1,onesz,tensz,hundredsz);

wire temp_anode2;
wire [6:0] temp_cathode1,temp_cathode2;

pmod p1 (onesz,temp_cathode1);
pmod p2 (tenz,temp_cathode2);

always @(posedge clk19)
    begin
        if (anode2 == 1'b0)
            begin
                anode2 = 1'b1;
                cathode2 = temp_cathode2;
            end
        else
            begin
                anode2 = 1'b0;
                cathode2 = temp_cathode1;
            end
    end


always @(posedge clk19)
    begin
        if (anode1 == anodea)
        begin
            anode1 = 4'b1101;
            cathode1 = cathodeb;
        end
        else if (anode1 == anodeb)
        begin
```

```
            anode1 = 4'b1011;
            cathode1 = cathodec;
        end
        else if (anode1 == anodec)
        begin
            anode1 = 4'b0111;
            cathode1 = cathoded;
        end
        else
        begin
            anode1 = 4'b1110;
            cathode1 = cathodea;
        end
    end

endmodule

SEVEN SEGMENT
`timescale 1ns / 1ps

module seven_segment (
        input [3:0] ones,
        //output [3:0] anode,
        output [7:0] cathode
        );

        reg [6:0] sseg_temp;
        always@ (*)
        begin
                case(ones)
                        4'd0 : sseg_temp = 7'b0000001;
                        4'd1 : sseg_temp = 7'b1001111;
                        4'd2 : sseg_temp = 7'b0010010;
                        4'd3 : sseg_temp = 7'b0000110;
                        4'd4 : sseg_temp = 7'b1001100;
                        4'd5 : sseg_temp = 7'b0100100;
                        4'd6 : sseg_temp = 7'b0100000;
                        4'd7 : sseg_temp = 7'b0001111;
                        4'd8 : sseg_temp = 7'b0000000;
                        4'd9 : sseg_temp = 7'b0000100;
                        default : sseg_temp = 7'b1111110;
                endcase;
        end;
```

```
        assign cathode = {sseg_temp, 1'b1};

endmodule
```

PMOD

```
`timescale 1ns / 1ps


module pmod(
   input [3:0] n1,
   output [6:0] cathode
   );

   reg [6:0] sseg_temp;


   always @ (*)
      begin
      case (n1)
      4'd0 : sseg_temp = 7'b0000001;
      4'd1 : sseg_temp = 7'b1001111;
      4'd2 : sseg_temp = 7'b0010010;
      4'd3 : sseg_temp = 7'b0000110;
      4'd4 : sseg_temp = 7'b1001100;
      4'd5 : sseg_temp = 7'b0100100;
      4'd6 : sseg_temp = 7'b0100000;
      4'd7 : sseg_temp = 7'b0001111;
      4'd8 : sseg_temp = 7'b0000000;
      4'd9 : sseg_temp = 7'b0000100;
      default : sseg_temp = 7'b1111110;
      endcase
      end
      assign cathode = ~sseg_temp;
endmodule
```

XDC

```
set_property PACKAGE_PIN W5 [get_ports {clk}]
set_property IOSTANDARD LVCMOS33 [get_ports {clk}]

set_property PACKAGE_PIN W15 [get_ports {x_in[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[0]}]
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```
set_property PACKAGE_PIN V15 [get_ports {x_in[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[1]}]
set_property PACKAGE_PIN W14 [get_ports {x_in[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[2]}]
set_property PACKAGE_PIN W13 [get_ports {x_in[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[3]}]
set_property PACKAGE_PIN V2 [get_ports {x_in[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[4]}]
set_property PACKAGE_PIN T3 [get_ports {x_in[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {x_in[5]}]

set_property PACKAGE_PIN R2 [get_ports {y_in[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[5]}]
set_property PACKAGE_PIN T1 [get_ports {y_in[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[4]}]
set_property PACKAGE_PIN U1 [get_ports {y_in[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[3]}]
set_property PACKAGE_PIN W2 [get_ports {y_in[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[2]}]
set_property PACKAGE_PIN R3 [get_ports {y_in[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[1]}]
set_property PACKAGE_PIN T2 [get_ports {y_in[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {y_in[0]}]

set_property PACKAGE_PIN W19 [get_ports {clr}]
set_property IOSTANDARD LVCMOS33 [get_ports {clr}]

set_property PACKAGE_PIN T17 [get_ports {pushbutton}]
set_property IOSTANDARD LVCMOS33 [get_ports {pushbutton}]

set_property PACKAGE_PIN V13 [get_ports {done}]
set_property IOSTANDARD LVCMOS33 [get_ports {done}]

set_property PACKAGE_PIN P18 [get_ports {anode2}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode2}]

set_property PACKAGE_PIN A14 [get_ports {cathode2[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[6]}]
set_property PACKAGE_PIN A16 [get_ports {cathode2[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[5]}]
set_property PACKAGE_PIN B15 [get_ports {cathode2[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[4]}]
set_property PACKAGE_PIN B16 [get_ports {cathode2[3]}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[3]}]
set_property PACKAGE_PIN K17 [get_ports {cathode2[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[2]}]
set_property PACKAGE_PIN M18 [get_ports {cathode2[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[1]}]
set_property PACKAGE_PIN N17 [get_ports {cathode2[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode2[0]}]

set_property PACKAGE_PIN W7 [get_ports {cathode1[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[7]}]
set_property PACKAGE_PIN W6 [get_ports {cathode1[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[6]}]
set_property PACKAGE_PIN U8 [get_ports {cathode1[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[5]}]
set_property PACKAGE_PIN V8 [get_ports {cathode1[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[4]}]
set_property PACKAGE_PIN U5 [get_ports {cathode1[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[3]}]
set_property PACKAGE_PIN V5 [get_ports {cathode1[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[2]}]
set_property PACKAGE_PIN U7 [get_ports {cathode1[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[1]}]
set_property PACKAGE_PIN V7 [get_ports {cathode1[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {cathode1[0]}]


set_property PACKAGE_PIN U2 [get_ports {anode1[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode1[0]}]
set_property PACKAGE_PIN U4 [get_ports {anode1[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode1[1]}]
set_property PACKAGE_PIN V4 [get_ports {anode1[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode1[2]}]
set_property PACKAGE_PIN W4 [get_ports {anode1[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {anode1[3]}]
```