LAB 2 PROBLEM 2

CODE:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/23/2017 02:49:50 AM
// Design Name:
// Module Name: lab2_p2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module lab2_p2(
    input [1:0]cost,
    input [1:0]qual_teacher,
    input qual_notes,
    input other_sub,
    output reg y,
    output reg z
    );
    always @(*)
    begin
        if ((qual_teacher == 2'b00 && other_sub == 1) || (cost != 2'b11 && other_sub == 1 ))
        begin
        z = 1;
        y = 0;
        end
        else if ((cost == 2'b11 && qual_teacher == 2'b00 && other_sub == 0) || (qual_teacher !=
2'b00 && qual_notes == 1 && cost == 2'b00))
```

```
        begin
        y = 1;
        z = 0;
        end
    end
endmodule
```

CONSTRAINT FILE :

```
set_property PACKAGE_PIN M15 [get_ports {cost[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cost[0]}];
set_property PACKAGE_PIN H17 [get_ports {cost[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {cost[1]}];
set_property PACKAGE_PIN H18 [get_ports {qual_teacher[0]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {qual_teacher[0]}];
set_property PACKAGE_PIN H19 [get_ports {qual_teacher[1]}]
   set_property IOSTANDARD LVCMOS33 [get_ports {qual_teacher[1]}];
set_property PACKAGE_PIN F21 [get_ports {qual_notes}]
   set_property IOSTANDARD LVCMOS33 [get_ports {qual_notes}];
set_property PACKAGE_PIN H22 [get_ports {other_sub}]
    set_property IOSTANDARD LVCMOS33 [get_ports {other_sub}];
set_property PACKAGE_PIN T21 [get_ports {y}]
   set_property IOSTANDARD LVCMOS33 [get_ports {y}];
set_property PACKAGE_PIN T22 [get_ports {z}]
    set_property IOSTANDARD LVCMOS33 [get_ports {z}];
```