HALF ADDER

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/15/2017 10:28:02 PM
// Design Name:
// Module Name: half_adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module half_adder(
    input A,
    input B,
    output sum,
    output carry
    );
    assign sum = A ^ B;
    assign carry = A && B;
endmodule
```

CONSTRAINT FILE:

```
set_property PACKAGE_PIN F22 [get_ports {A}]
set_property IOSTANDARD LVCMOS33 [get_ports {A}];
set_property PACKAGE_PIN F22 [get_ports {B}]
set_property IOSTANDARD LVCMOS33 [get_ports {B}];
set_property PACKAGE_PIN T18 [get_ports {sum}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum}];
```

```
set_property PACKAGE_PIN V22 [get_ports {carry}]
set_property IOSTANDARD LVCMOS33 [get_ports {carry}];
```

FULL ADDER

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/15/2017 10:30:46 PM
// Design Name:
// Module Name: full_adder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module full_adder(
    input A,
    input B,
    input C,
    output sum,
    output carry,
    wire sum1,carry1,carry2
    );
    half_adder o1 (A,B,sum1,carry1);
    half_adder o2 (sum1,C,sum,carry2);
    or (carry,carry1,carry2);
```

```
endmodule
```

CONSTRAINT FILE:

```
set_property PACKAGE_PIN F22 [get_ports {A}]
set_property IOSTANDARD LVCMOS33 [get_ports {A}];
set_property PACKAGE_PIN F22 [get_ports {B}]
set_property IOSTANDARD LVCMOS33 [get_ports {B}];
set_property PACKAGE_PIN F22 [get_ports {C}]
set_property IOSTANDARD LVCMOS33 [get_ports {C}];
set_property PACKAGE_PIN T18 [get_ports {sum}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum}];
set_property PACKAGE_PIN V22 [get_ports {carry}]
set_property IOSTANDARD LVCMOS33 [get_ports {carry}];
```

4 - BIT FULL ADDER - SUBTRACTOR USING 1 - BIT ADDER

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/15/2017 10:47:25 PM
// Design Name:
// Module Name: four_bit_using_one
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
```

```
module four_bit_using_one(
    input [3:0] A,
    input [3:0] B,
    input M,
    output [3:0] sum,
    output carry,
    wire c1,c2,c3
    );
    full_adder o3 (A[0],(B[0]^M),M,sum[0],c1);
    full_adder o4 (A[1],(B[1]^M),c1,sum[1],c2);
    full_adder o5 (A[2],(B[2]^M),c2,sum[2],c3);
    full_adder o6 (A[3],(B[3]^M),c3,sum[3],carry);
endmodule
```

CONSTRAINT FILE:

```
set_property PACKAGE_PIN F22 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}];
set_property PACKAGE_PIN G22 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}];
set_property PACKAGE_PIN H22 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}];
set_property PACKAGE_PIN F21 [get_ports {A[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}];
set_property PACKAGE_PIN H19 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}];
set_property PACKAGE_PIN H18 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}];
set_property PACKAGE_PIN H17 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}];
set_property PACKAGE_PIN M15 [get_ports {B[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}];
set_property PACKAGE_PIN T22 [get_ports {sum[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum[3]}];
set_property PACKAGE_PIN T21 [get_ports {sum[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum[2]}];
set_property PACKAGE_PIN U22 [get_ports {sum[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum[1]}];
set_property PACKAGE_PIN U21 [get_ports {sum[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {sum[0]}];
set_property PACKAGE_PIN V22 [get_ports {carry}]
set_property IOSTANDARD LVCMOS33 [get_ports {carry}];
set_property PACKAGE_PIN T18 [get_ports {M}]
```

```
set_property IOSTANDARD LVCMOS33 [get_ports {M}];
```