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Facultad de Ingeniería
Escuela de Ingeniería Eléctrica
IE-0624: Laboratorio de Microcontroladores

Laboratorio #1: Introducción a microcontroladores y manejo de GPIOS

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Índice

1. Introducción	1
2. Nota teórica	2
2.1. Información general del MCU	2
2.1.1. Características	2
2.1.2. Diagrama de bloques	2
2.1.3. Diagrama de pines	3
2.2. Características eléctricas	3
2.3. Periféricos	3
2.4. Lista de componentes y precios	4
2.4.1. Componentes pasivos	4
2.4.2. Componentes activos	4
2.5. Diseño de circuito	5
2.6. Conceptos/temas del laboratorio	6
3. Desarrollo	7
4. Conclusiones y Recomendaciones	13
5. Bibliografía	14
6. Apéndice	14

Índice de figuras

1.	Diagrama de bloques para PIC12F683	2
2.	Diagrama de pines para PIC12F683	3
3.	Especificaciones eléctricas del PIC12F683	3
4.	Diseño realizado para el funcionamiento del circuito	5
5.	Diagrama de flujo del programa realizado	8
6.	Número aleatorio 41 obtenido al presionar el botón del circuito diseñado	8
7.	Número aleatorio 01 obtenido al presionar el botón del circuito diseñado	9
8.	Número aleatorio 20 obtenido al presionar el botón del circuito diseñado	9
9.	Número aleatorio 40 obtenido al presionar el botón del circuito diseñado	10
10.	Número aleatorio 22 obtenido al presionar el botón del circuito diseñado	10
11.	Número aleatorio 8 obtenido al presionar el botón del circuito diseñado	11
12.	Número aleatorio 42 obtenido al presionar el botón del circuito diseñado	11
13.	Número 00 (parpadeando) obtenido luego de 10 números	12

1. Introducción

Para el primer laboratorio se desarrolló un simulador de tómbola simplificado de bingo, utilizando componentes como un display de 7 Segmentos de 2 dígitos, un botón, el microcontrolador PIC12F683, resistencias, capacitor, decodificador BCD a 7 segmentos, transistor y un demultiplexador. Se diseña el circuito con los componentes necesarios mediante SimulIDE y luego se procede a programar mediante lenguaje c el funcionamiento del microcontrolador utilizado para lograr el objetivo de la práctica.

Con el desarrollo de esta práctica, se busca que el estudiante se familiarice con el diseño de circuitos que utilizan microcontroladores, como es el caso de la familia PIC, así como la programación de dicho componente. El estudio de las hojas de datos proporcionada por el fabricante de los elementos electrónicos es clave para tener un buen entendimiento del funcionamiento y la arquitectura de estos.

En el siguiente link se encuentra el repositorio de trabajo: https://github.com/NisseUR/IE-0624_C07893

2. Nota teórica

2.1. Información general del MCU

2.1.1. Características

Se trabaja con un microcontrolador PIC12F683, fabricado por Microchip Technology, de la familia CMOS con una memoria de datos de 8 bits. Utilizan memoria flash para guardar programas, y tiene 8 pines con tecnología nanoWatt, de los cuales 6 son de tipo I/O que pueden ser configurados como entradas o salidas digitales. Posee un CPU arquitectura RISC de alto rendimiento con 35 instrucciones, y para efectos del laboratorio se programa en C (SDCC). La corriente de salida máxima generada por cualquier I/O pin es de 25 mA. Posee una memoria de datos RAM de 128 bytes, e incluye 256 bytes de memoria EEPROM la cual puede ser utilizada en el almacenamiento de datos que deben mantenerse incluso cuando el dispositivo está apagado.

2.1.2. Diagrama de bloques

Se muestra el diagrama de bloques obtenido de la hoja de datos del PIC12F683:

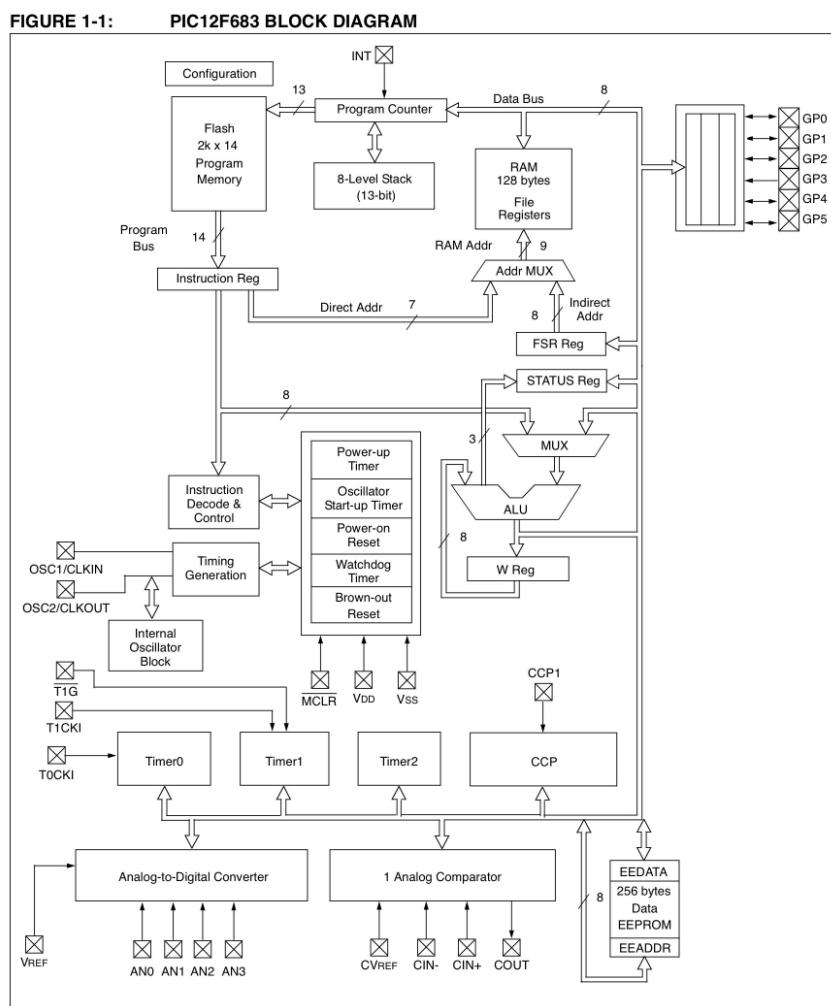


Figura 1: Diagrama de bloques para PIC12F683

2.1.3. Diagrama de pines

De la misma hoja de datos, se obtiene el diagrama de pines que se muestra a continuación:

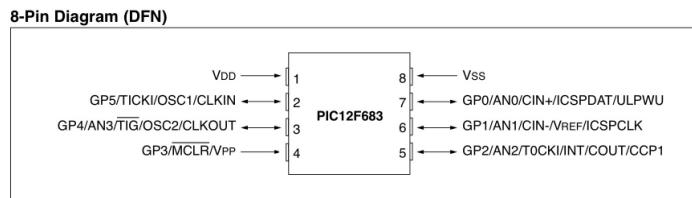


Figura 2: Diagrama de pines para PIC12F683

De la figura 2, los GP0 al GP5 corresponden a señal digital I/O, V_{DD} es la fuente de alimentación de 5 V y V_{SS} la conexión a tierra

2.2. Características eléctricas

Las especificaciones eléctricas del microcontrolador se encuentran en la hoja de datos, y se detallan en la siguiente figura:

Absolute Maximum Ratings ⁽¹⁾	
Ambient temperature under bias.....	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD} with respect to V_{SS}	-0.3V to +6.5V
Voltage on MCLR with respect to V_{SS}	-0.3V to +13.5V
Voltage on all other pins with respect to V_{SS}	-0.3V to (V_{DD} + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of V_{SS} pin	95 mA
Maximum current into V_{DD} pin	95 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$).....	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by GPIO	90 mA
Maximum current sourced GPIO.....	90 mA
Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$.	

Figura 3: Especificaciones eléctricas del PIC12F683

2.3. Periféricos

El PIC12F683 posee diversos registros los cuales son operables digitalmente, los cuales son de gran importancia ya que controlan cómo interactúa el microcontrolador con el resto del circuito a través de sus pines de I/O. Se detallan a continuación:

- **CONFIG:** utilizado para configurar ajustes importantes del MCU, como la selección del oscilador, configuración de Watchdog Timer, protección de código y otros ajustes de operación los cuales van a definir cómo el microcontrolador se comportará al encenderse o reiniciarse. Es parte del espacio de memoria de configuración del microcontrolador.
- **TRISIO:** se encarga de definir la dirección de flujo de datos de los pines I/O. Al configurar un bit del registro TRISIO a 1, el pin correspondiente se configura como entrada, lo cual implica que el pin puede leer señales. Si se coloca TRISIO a 0, el pin va a ser programado como salida, lo cual significa que va a enviar señales fuera del PIC12F683.

- **GPIO:** se encarga de leer el estado del pin y se escribe al latch de salida. Mantiene la información del estado actual de todos los pines del puerto GPIO, tanto para entradas como salidas.

2.4. Lista de componentes y precios

Los componentes que se utilizaron en el diseño del circuito, el cual se muestra en la figura 4, fueron los siguientes:

2.4.1. Componentes pasivos

- **Capacitor:** almacena energía en un campo eléctrico. Precio: ₡80
- **Resistencia:** se opone al flujo de corriente. Precio: Para 10k Ω son ₡65, 130 Ω son 45₡, 1k Ω son 50₡.

2.4.2. Componentes activos

- **Microcontrolador PIC12F683:** Es un componente activo que puede controlar otros componentes en un circuito, procesando información. Precio: ₡1444
- **Transistor BJT** (Transistor de Unión Bipolar): para amplificar corriente o, su función principal en el diseño realizado, para actuar como un interruptor. Precio: ₡150
- **Demultiplexor:** toma una señal de entrada y la selecciona entre varias salidas. Precio: ₡880
- **Decodificador BCD a 7 Segmentos:** decodifica una entrada binaria en una salida específica para displays de 7 segmentos. Precio: ₡595
- **2-digit Display de 7 Segmentos:** dispositivos de visualización de caracteres, en este caso, números decimales. Precio: ₡1150

2.5. Diseño de circuito

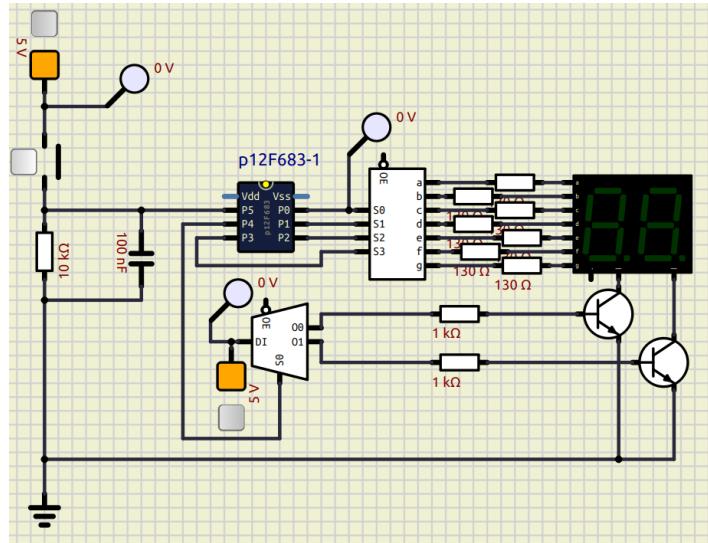


Figura 4: Diseño realizado para el funcionamiento del circuito

Para el programa que se busca realizar, se diseña el circuito mostrado en la figura 4, con los componentes explicados en la sección anterior. Se tiene el botón, que corresponde al dispositivo de entrada del usuario, y tiene una resistencia de 10k Ω y un capacitor de 100 nF conectados con el objetivo de filtrar el ruido y los posibles rebotes del botón (conocido como debouncing). La elección de los valores para la resistencia y el capacitor conectados la botón va a depender del tiempo que se desee que tarde la señal en estabilizarse después de presionar el botón. Según las recomendaciones de [1], se opta por una resistencia de 10k Ω y un capacitor de 100 nF, proporcionando así un intervalo adecuado entre pulsaciones de aproximadamente 0.5 ms, lo cual se ajusta a los requerimientos del laboratorio..

Al presionar el botón, la combinación de la resistencia y el capacitor actúa para atenuar variaciones bruscas o rebotes en la señal. Esto conduce a una transición de señal más suave y precisa, mejorando así la fiabilidad del circuito.

El botón se encuentra conectado a la entrada GP5 del microcontrolador PIC12F683, el cual está programado para recibir y leer la señal que envía dicho botón al ser presionado, para que se genere el número aleatorio en el display de 7 segmentos. El decodificador BCD a 7 segmentos, que está conectado a los pines GP0-GP3, toma la señal de salida binarias del PIC y las convierte en las señales apropiadas para activar los segmentos individuales del display. Entre el decodificador y el display de 7 segmentos se colocan resistencias de 130 Ω para limitar la corriente que fluye hacia el display y evitar daños en el componente; se escoge este valor porque según las especificaciones de la hoja de datos del display de 7S la corriente máxima que puede pasar por el display de 7S es de 20 mA mientras que su tensión es de 2.4 V, y del microcontrolador proporciona una tensión de 5 V. Se procede a realizar el siguiente cálculo:

$$R = \frac{V_{MCU} - V_{7S}}{I_{7S}} \quad (1)$$

$$R = \frac{5 - 2,4}{20m} = 130\Omega$$

El display de 7 segmentos de 2 dígitos corresponde al componente de salida que muestra los números generados por el PIC, donde segmento del display se ilumina en base a las señales proporcionadas por el decodificador BCD mencionado previamente. Cada dígito del display tiene su propio cátodo común, y para controlar dichos dígitos se les conecta un transistor BJT PNP. En una configuración PNP, cuando la base del transistor es llevada a un nivel bajo, el transistor se activa y permite que la corriente fluya desde el emisor al colector, lo cual encendería el dígito correspondiente en el display.

La base del transistor se encuentra conectada a la salida del demultiplexor 2 a 1 (con una resistencia en el medio de esos componentes para limitar la corriente que fluye), el cual es un dispositivo utilizado para seleccionar cuál dígito del display de 7 segmentos está activo en un momento dado. Esto corresponde a parte del proceso de multiplexación, donde los dígitos se activan uno a la vez a una velocidad suficientemente alta para que el ojo humano vea ambos números como si estuvieran encendidos constantemente. La entrada del demux se encuentra conectada al GP4 (pin programado como una señal de salida digital).

El valor de $1k\ \Omega$ es una elección común que proporciona una corriente de base adecuada para muchos transistores en aplicaciones generales de baja potencia, por lo cual se decide utilizar.

El funcionamiento del circuito consiste en que al presionar el botón, el PIC12F683 genera un número aleatorio. Este número es enviado al decodificador BCD que activa los segmentos correctos en el display de 7 segmentos. Los transistores PNP y el demultiplexor van a trabajar juntos para alternar entre los dos dígitos del display, mostrando el número generado. El capacitor y la resistencia de pull-down van a ayudar para que el botón proporcione una señal clara y sin rebotes al microcontrolador. Finalmente, la fuente de poder suministra la energía necesaria para que todos los componentes operen correctamente.

2.6. Conceptos/temas del laboratorio

Para este laboratorio se busca el estudio de las GPIOs así como la introducción a los microcontroladores y su historia, donde se le da un énfasis a los de la familia PIC ya que va a ser el tipo de MCU utilizado en el desarrollo de la práctica.

3. Desarrollo

Una vez diseñado el circuito, se procede a realizar la programación del microcontrolador PIC12F683 mediante el lenguaje c y un editor de texto. El propósito del código es generar y mostrar números aleatorios entre 0 y 99 en un display de 7 segmentos, utilizando un botón para activar la generación de números y un sistema para evitar repetir números ya mostrados. Al inicio del código fuente se configura el registro CONFIG, definiendo la variable de tipo word y desactivando el Watchdog Timer.

Se define al pin del GP5 como una entrada que recibe la señal del botón, GP4 como salida que le envía la señal al display para encender los dígitos y GP0-GP3 como salida que va a enviarle la señal al display para indicarle que números debe mostrar. Luego se define el arrays de caracteres con los números decimales que representan los dígitos del 0 al 9, tomando en cuenta que se tiene un display de cátodo común.

Se procede a definir las funciones a utilizar en el programa, como el delay que se encarga de crear un retardo; showNumber que muestra un número en el display utilizando multiplexación; savedNumber, la cual verifica si un número ya ha sido generado anteriormente; save, que guarda un número en el array saved; reset, provoca el reinicio del array saved; finalmente blink99 hace que parpadee el número 99 en el display, como indicador. En el main se configura los pines GPIO, y luego entra en un bucle infinito donde comprueba el estado del botón. Si está presionado (donde al ser una configuración de tipo pull down entonces se activa en 0), genera un número entre 0 y 99 que no haya sido generado antes y lo muestra en el display.

Para generar los números aleatorios se hace uso de una aproximación simple basada en un contador que se incrementa cada vez que el bucle main se ejecuta y cada vez que se presiona el botón. La variable llamada seed se inicializa en 0 y se incrementa en 1 en cada iteración del bucle principal, que ocurre cada vez que se detecta un botón presionado. Se tiene la variable num = seed % 100 que calcula el resto de la división de seed por 100, resultando en un número entre 0 y 99, y se asigna a num. Luego se incrementa seed en 1 para cambiar el valor para la próxima generación de número, esto al hacer seed++.

Después de generar un número, se verifica si ese valor ya ha sido generado anteriormente usando la función savedNumber. En caso de que ya haya sido generado, se repite el proceso con el siguiente valor de seed, hasta encontrar una cantidad la cual no se encuentre entre los repetidos.

A continuación se muestra el diagrama de flujo realizado con la lógica del código utilizada:

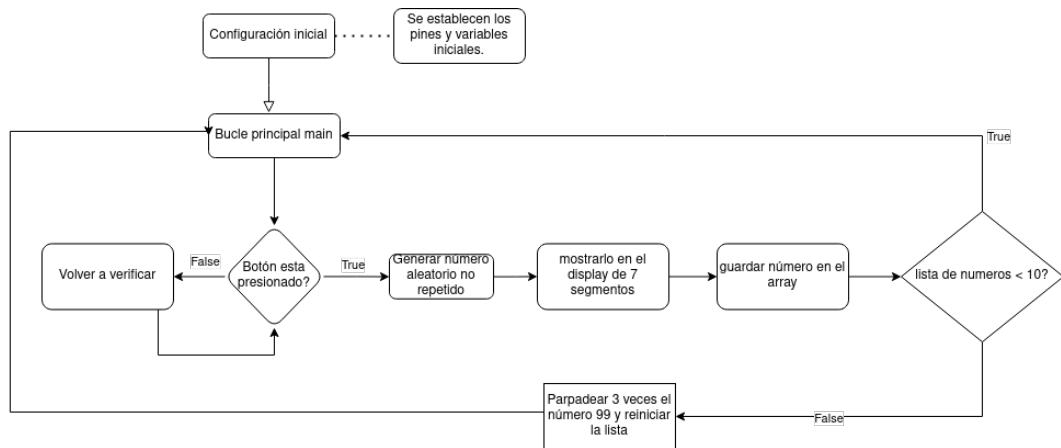


Figura 5: Diagrama de flujo del programa realizado

Al encender el simulación y presionar el botón del circuito, se procede a desplegar un número aleatorio entre 00 y 99 en la pantalla como el que se muestra en las siguientes figuras se pueden observar los números aleatorios obtenidos:

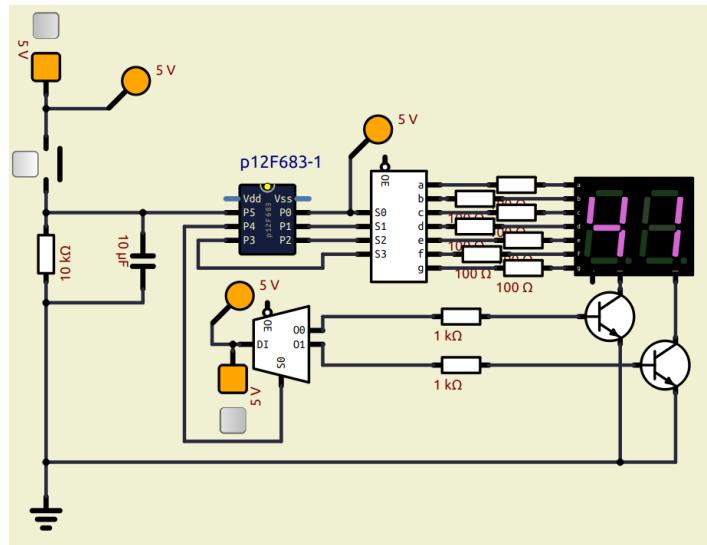


Figura 6: Número aleatorio 41 obtenido al presionar el botón del circuito diseñado

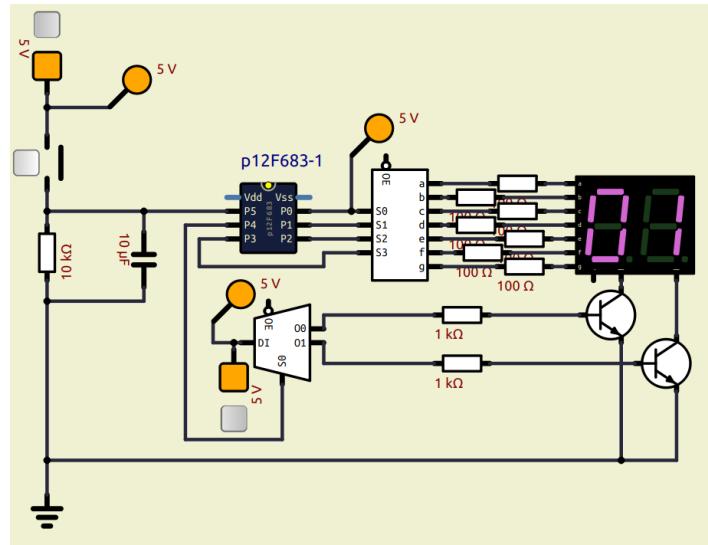


Figura 7: Número aleatorio 01 obtenido al presionar el botón del circuito diseñado

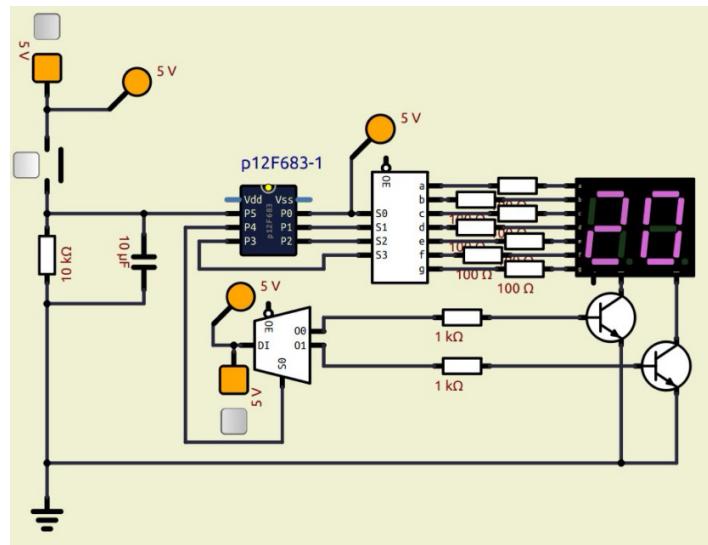


Figura 8: Número aleatorio 20 obtenido al presionar el botón del circuito diseñado

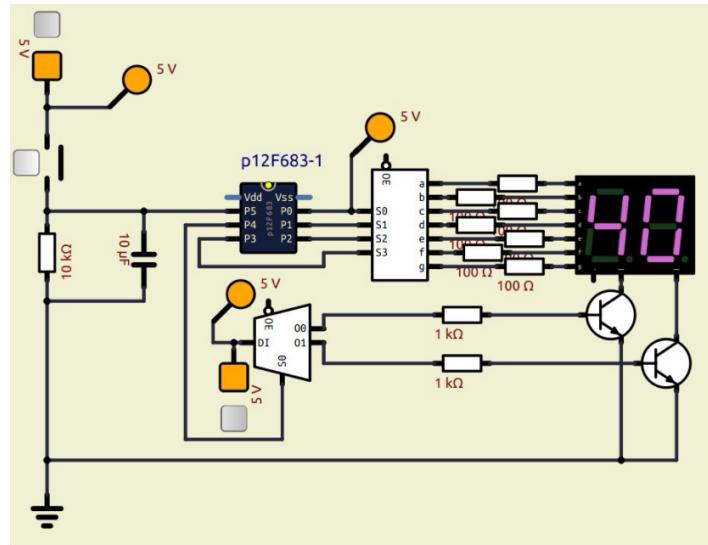


Figura 9: Número aleatorio 40 obtenido al presionar el botón del circuito diseñado

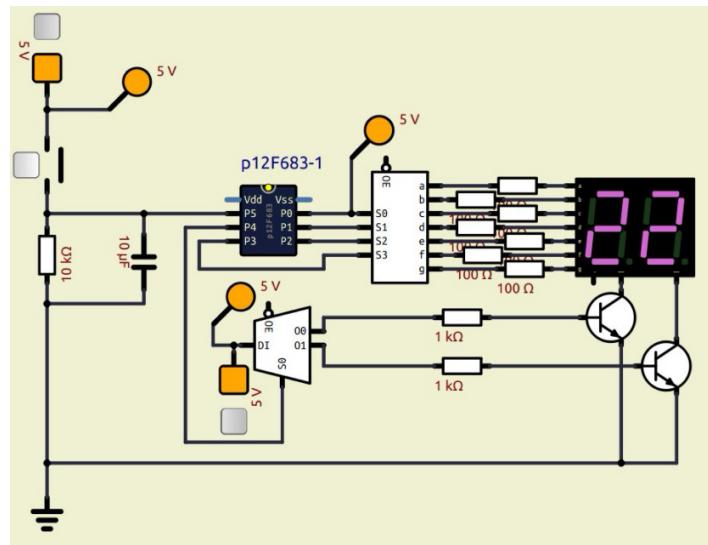


Figura 10: Número aleatorio 22 obtenido al presionar el botón del circuito diseñado

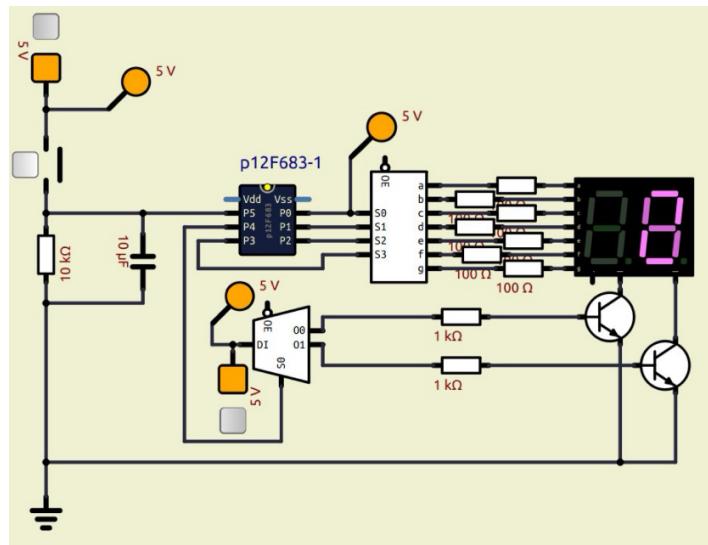


Figura 11: Número aleatorio 8 obtenido al presionar el botón del circuito diseñado

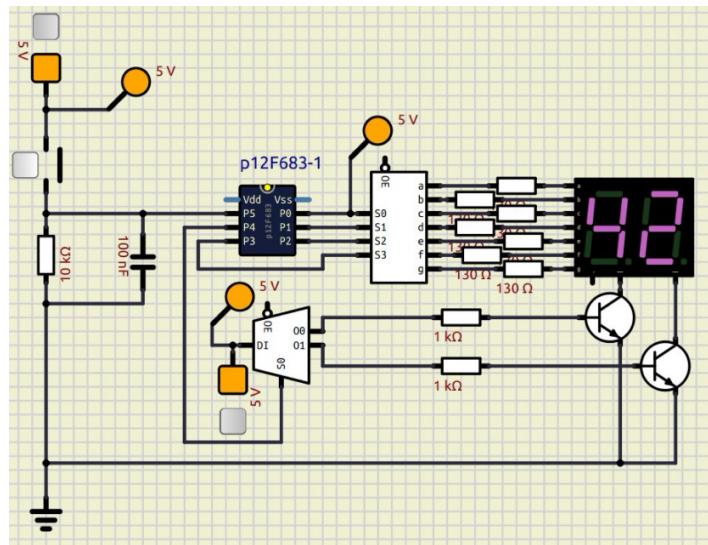


Figura 12: Número aleatorio 42 obtenido al presionar el botón del circuito diseñado

Al presionar el botón 10 veces, se reinicia el sistema y en el display se muestra el 00 parpadeando como indicación del reset.

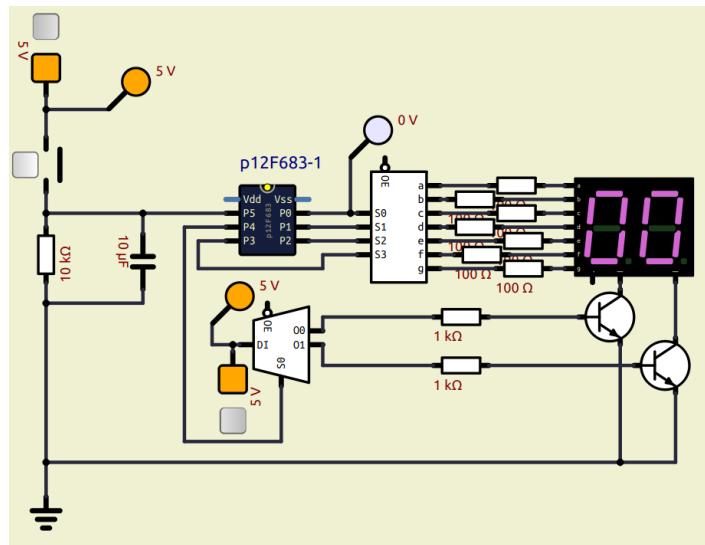


Figura 13: Número 00 (parpadeando) obtenido luego de 10 números

Se logra obtener números aleatorias en el display de 7 segmentos al presionar el botón en el circuito, sin embargo se presentan ciertas fallas como la observada en la figura 11 donde en vez de mostrarse el número 08 se tiene el dígito 8. También, en vez de parpadear el número 99 una vez presentados 10 números, se despliega el número 00. Pero en general, el programa realizado cumple el objetivo de la práctica.

4. Conclusiones y Recomendaciones

Para concluir el laboratorio, se realiza una introducción al concepto de microcontroladores y como manejar los GPIOs. Es importante leer y entender las hojas de datos de los componentes utilizados para así tener una mejor comprensión de sus especificaciones y arquitectura. De esta forma se puede hacer uso adecuado de los elementos electrónicos al diseñar el circuito, donde se busca que sea lo más adecuado posible y evitar fallos o dañar dichos dispositivos.

Al utilizar un botón, se debe tomar en cuenta el efecto rebote que puede provocar al ser presionado, por lo cual se debe tomar en consideración medidas para disminuir este efecto, como lo es el implementar una configuración pull down con una resistencia y capacitor, además de la lógica de programación necesaria para agregar un retardo que evita la lectura múltiple debido al efecto rebote del botón. La resistencia pull-down asegura que el pin de entrada al PIC tenga un estado lógico bajo claro y previene lecturas incorrectas causadas por el ruido eléctrico o al ya mencionado rebote del botón.

Para el uso óptimo del microcontrolador, se recomienda utilizar herramientas las cuales ofrezcan entorno integrado para escribir, depurar y programar el código. Con SimulIDE se logra aprender y experimentar con la simulación de circuitos electrónicos analógicos y digitales, así como microcontroladores, para practicar su uso sin la necesidad de utilizar componentes reales que pueden sufrir daños además de ser costosos.

Hay diversas formas de crear un generador de números, la utilizada en el código se basa en un contador simple que genera números secuenciales entre 0 y 99 y verifica si el número ya ha sido generado antes. Para efectos de implementación en un sistema simple como es la simulación de una tómbola de bingo es útil, pero para efectos de aplicaciones más complejas es recomendable hacer uso de metodologías más exactas.

El programa presenta ciertas fallas, como el caso donde se enciende un solo dígito en vez de los dos dígitos, pero se logra cumplir el propósito del laboratorio que consiste en la introducción al diseño de circuito que incluyen microcontroladores así el estudio de su arquitectura y su programación para funcionar.

5. Bibliografía

Referencias

- [1] D. Segura and V. T. mi Perfil. Electrónica fácil.
<http://arduinopractico.blogspot.com/2014/11/resistencias-pull-up-y-pull-down.html>,
2014. 2.5

6. Apéndice

Se incluyen las hojas de datos de todos los componentes pasivos y activos utilizados.



PIC12F683

Data Sheet

8-Pin Flash-Based, 8-Bit
CMOS Microcontrollers with
nanoWatt Technology

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**MICROCHIP****PIC12F683**

8-Pin Flash-Based, 8-Bit CMOS Microcontrollers with nanoWatt Technology

High-Performance RISC CPU:

- Only 35 instructions to learn:
 - All single-cycle instructions except branches
- Operating speed:
 - DC – 20 MHz oscillator/clock input
 - DC – 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect and Relative Addressing modes

Special Microcontroller Features:

- Precision Internal Oscillator:
 - Factory calibrated to $\pm 1\%$, typical
 - Software selectable frequency range of 8 MHz to 125 kHz
 - Software tunable
 - Two-Speed Start-up mode
 - Crystal fail detect for critical applications
 - Clock mode switching during operation for power savings
- Power-Saving Sleep mode
- Wide operating voltage range (2.0V-5.5V)
- Industrial and Extended temperature range
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with software control option
- Enhanced Low-Current Watchdog Timer (WDT) with on-chip oscillator (software selectable nominal 268 seconds with full prescaler) with software enable
- Multiplexed Master Clear with pull-up/input pin
- Programmable code protection
- High Endurance Flash/EEPROM cell:
 - 100,000 write Flash endurance
 - 1,000,000 write EEPROM endurance
 - Flash/Data EEPROM Retention: > 40 years

Low-Power Features:

- Standby Current:
 - 50 nA @ 2.0V, typical
- Operating Current:
 - 11 μ A @ 32 kHz, 2.0V, typical
 - 220 μ A @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
 - 1 μ A @ 2.0V, typical

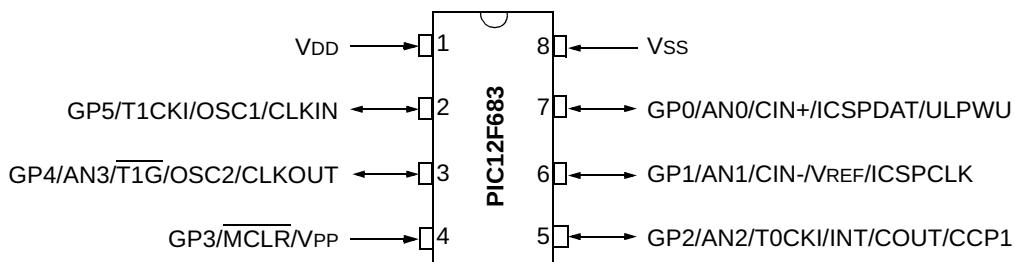
Peripheral Features:

- 6 I/O pins with individual direction control:
 - High current source/sink for direct LED drive
 - Interrupt-on-pin change
 - Individually programmable weak pull-ups
 - Ultra Low-Power Wake-up on GP0
- Analog Comparator module with:
 - One analog comparator
 - Programmable on-chip voltage reference (CVREF) module (% of VDD)
 - Comparator inputs and output externally accessible
- A/D Converter:
 - 10-bit resolution and 4 channels
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Timer1 Gate (count enable)
 - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator if INTOSC mode selected
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Capture, Compare, PWM module:
 - 16-bit Capture, max resolution 12.5 ns
 - Compare, max resolution 200 ns
 - 10-bit PWM, max frequency 20 kHz
- In-Circuit Serial Programming™ (ICSP™) via two pins

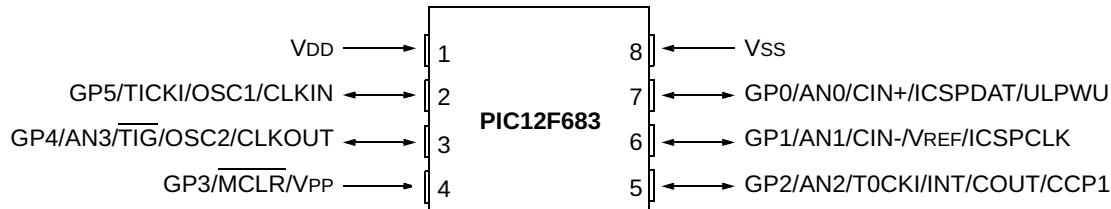
Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	Flash (words)	SRAM (bytes)	EEPROM (bytes)				
PIC12F683	2048	128	256	6	4	1	2/1

PIC12F683

8-Pin Diagram (PDIP, SOIC)



8-Pin Diagram (DFN)



8-Pin Diagram (DFN-S)

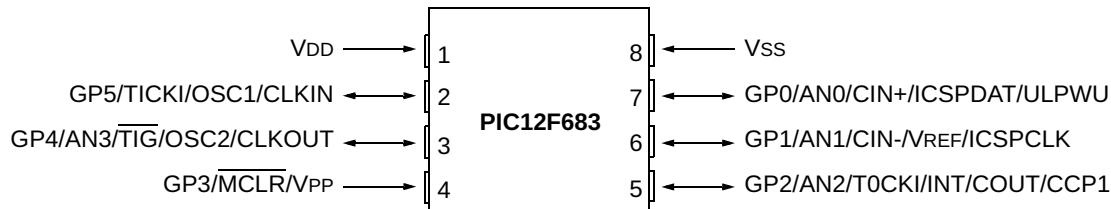


TABLE 1: 8-PIN SUMMARY

I/O	Pin	Analog	Comparators	Timer	CCP	Interrupts	Pull-ups	Basic
GP0	7	AN0	CIN+	—	—	IOC	Y	ICSPDAT/ULPWU
GP1	6	AN1/VREF	CIN-	—	—	IOC	Y	ICSPCLK
GP2	5	AN2	COUT	T0CKI	CCP1	INT/IOC	Y	—
GP3 ⁽¹⁾	4	—	—	—	—	IOC	Y ⁽²⁾	MCLR/VPP
GP4	3	AN3	—	T1G	—	IOC	Y	OSC2/CLKOUT
GP5	2	—	—	T1CKI	—	IOC	Y	OSC1/CLKIN
—	1	—	—	—	—	—	—	VDD
—	8	—	—	—	—	—	—	VSS

Note 1: Input only.

2: Only when pin is configured for external MCLR.

Table of Contents

1.0	Device Overview	5
2.0	Memory Organization	7
3.0	Oscillator Module (With Fail-Safe Clock Monitor).....	19
4.0	GPIO Port.....	31
5.0	Timer0 Module	41
6.0	Timer1 Module with Gate Control.....	44
7.0	Timer2 Module	49
8.0	Comparator Module.....	51
9.0	Analog-to-Digital Converter (ADC) Module	61
10.0	Data EEPROM Memory	71
11.0	Capture/Compare/PWM (CCP) Module	75
12.0	Special Features of the CPU.....	83
13.0	Instruction Set Summary	101
14.0	Development Support.....	111
15.0	Electrical Specifications.....	115
16.0	DC and AC Characteristics Graphs and Tables.....	137
17.0	Packaging Information.....	159
	Appendix A: Data Sheet Revision History.....	165
	Appendix B: Migrating From Other PIC® Devices.....	165
	The Microchip Web Site.....	171
	Customer Change Notification Service	171
	Customer Support.....	171
	Reader Response	172
	Product Identification System	173

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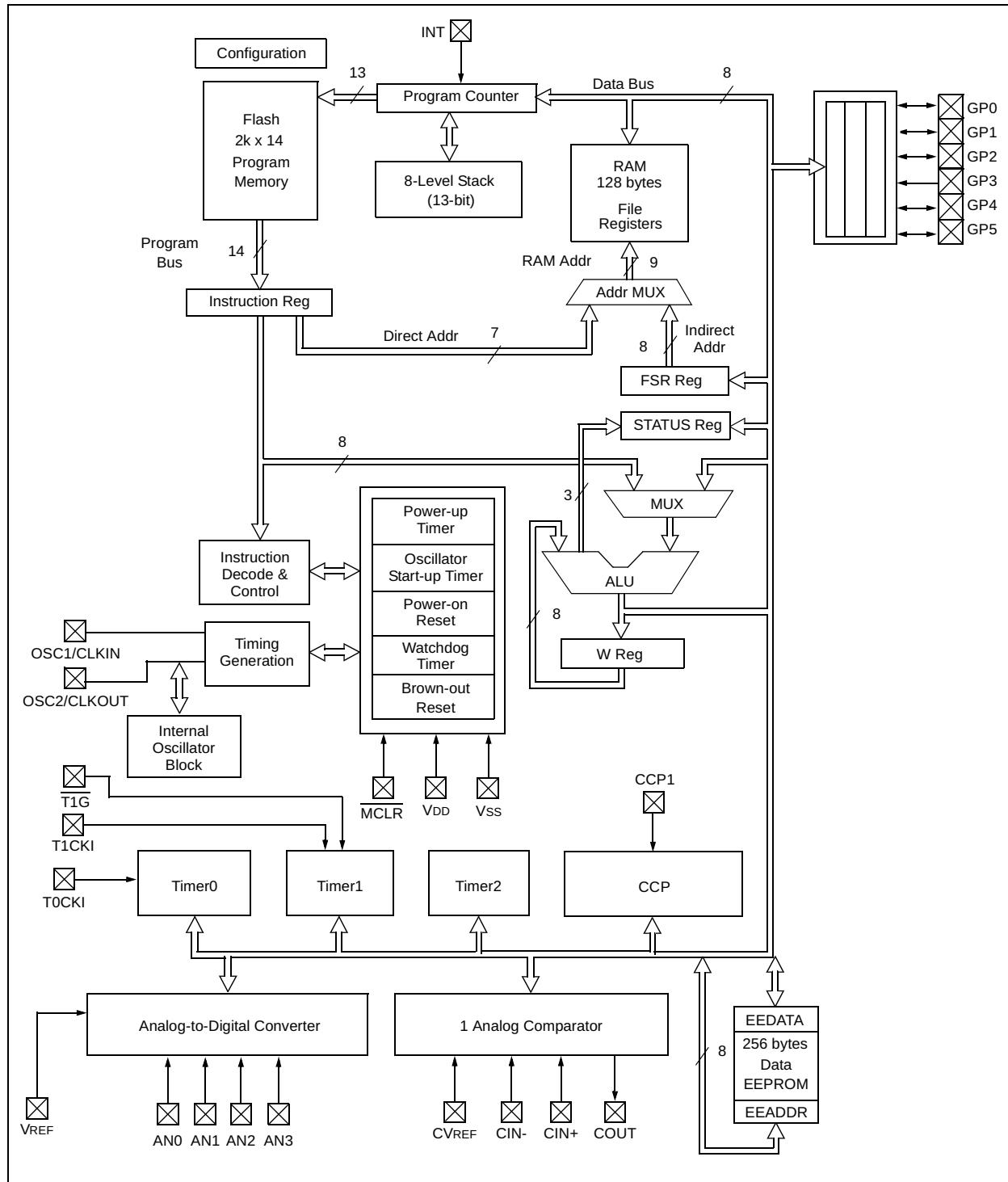
PIC12F683

NOTES:

1.0 DEVICE OVERVIEW

The PIC12F683 is covered by this data sheet. It is available in 8-pin PDIP, SOIC and DFN-S packages. Figure 1-1 shows a block diagram of the PIC12F683 device. Table 1-1 shows the pinout description.

FIGURE 1-1: PIC12F683 BLOCK DIAGRAM



PIC12F683

TABLE 1-1: PIC12F683 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
VDD	VDD	Power	—	Positive supply
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	T1CKI	ST	—	Timer1 clock
	OSC1	XTAL	—	Crystal/Resonator
	CLKIN	ST	—	External clock input/RC oscillator connection
	GP4	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
GP4/AN3/T1G/OSC2/CLKOUT	AN3	AN	—	A/D Channel 3 input
	<u>T1G</u>	ST	—	Timer1 gate
	OSC2	—	XTAL	Crystal/Resonator
	CLKOUT	—	CMOS	Fosc/4 output
	GP3/MCLR/VPP	—	—	GPIO input with interrupt-on-change
GP2/AN2/T0CKI/INT/COUT/CCP1	MCLR	ST	—	Master Clear with internal pull-up
	VPP	HV	—	Programming voltage
	GP2	ST	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External Interrupt
GP1/AN1/CIN-/VREF/ICSPCLK	COUT	—	CMOS	Comparator 1 output
	CCP1	ST	CMOS	Capture input/Compare output/PWM output
	GP1	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN1	AN	—	A/D Channel 1 input
	CIN-	AN	—	Comparator 1 input
GP0/AN0/CIN+/ICSPDAT/ULPWU	VREF	AN	—	External Voltage Reference for A/D
	ICSPCLK	ST	—	Serial Programming Clock
	GP0	TTL	CMOS	GPIO I/O with prog. pull-up and interrupt-on-change
	AN0	AN	—	A/D Channel 0 input
	CIN+	AN	—	Comparator 1 input
Vss	ICSPDAT	ST	CMOS	Serial Programming Data I/O
	ULPWU	AN	—	Ultra Low-Power Wake-up input
Vss	Vss	Power	—	Ground reference

Legend:
 AN = Analog input or output
 TTL = TTL compatible input
 HV = High Voltage

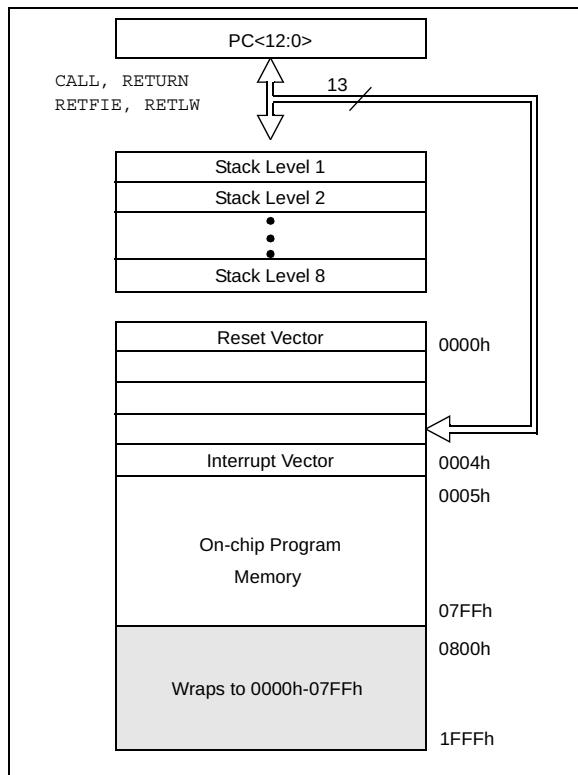
CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels
 XTAL = Crystal

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F683 has a 13-bit program counter capable of addressing an 8k x 14 program memory space. Only the first 2k x 14 (0000h-07FFh) for the PIC12F683 is physically implemented. Accessing a location above these boundaries will cause a wraparound within the first 2K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F683



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers (GPR) and the Special Function Registers (SFR). The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-7Fh in Bank 0 and A0h-BFh in Bank 1 are General Purpose Registers, implemented as static RAM. Register locations F0h-FFh in Bank 1 point to addresses 70h-7Fh in Bank 0. All other RAM is unimplemented and returns '0' when read. RP0 of the STATUS register is the bank select bit.

RP0

- 0 → Bank 0 is selected
- 1 → Bank 1 is selected

Note: The IRP and RP1 bits of the STATUS register are reserved and should always be maintained as '0's.

PIC12F683

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 128 x 8 in the PIC12F683. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4 “Indirect Addressing, INDF and FSR Registers”).

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function Registers associated with the “core” are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC12F683

File Address	File Address
Indirect addr. ⁽¹⁾	00h
TMR0	01h
PCL	02h
STATUS	03h
FSR	04h
GPIO	05h
	06h
	07h
	08h
	09h
PCLATH	0Ah
INTCON	0Bh
PIR1	0Ch
	0Dh
TMR1L	0Eh
TMR1H	0Fh
T1CON	10h
TMR2	11h
T2CON	12h
CCPR1L	13h
CCPR1H	14h
CCP1CON	15h
	16h
	17h
WDTCON	18h
CMCON0	19h
CMCON1	1Ah
	1Bh
	1Ch
	1Dh
ADRESH	1Eh
ADCON0	1Fh
General Purpose Registers 96 Bytes	20h
	7Fh
	BANK 0
	BANK 1
	Accesses 70h-7Fh
	EFh
	F0h
	FFh

 Unimplemented data memory locations, read as '0'.

Note 1: Not a physical register.

TABLE 2-1: PIC12F683 SPECIAL REGISTERS SUMMARY BANK 0

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 0											
00h	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	17, 90
01h	TMRO	Timer0 Module Register								xxxx xxxx	41, 90
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17, 90
03h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	TO	PD	Z	DC	C	0001 1xxx	11, 90
04h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	17, 90
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	31, 90
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for upper 5 bits of Program Counter					--0 0000	17, 90
0Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	13, 90
0Ch	PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	15, 90
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1								xxxx xxxx	44, 90
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1								xxxx xxxx	44, 90
10h	T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	\bar{T} 1SYNC	TMR1CS	TMR1ON	0000 0000	47, 90
11h	TMR2	Timer2 Module Register								0000 0000	49, 90
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	50, 90
13h	CCPR1L	Capture/Compare/PWM Register 1 Low Byte								xxxx xxxx	76, 90
14h	CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	76, 90
15h	CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	75, 90
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	--0 1000	97, 90
19h	CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	56, 90
1Ah	CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	57, 90
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH	Most Significant 8 bits of the left shifted A/D result or 2 bits of right shifted result								xxxx xxxx	61, 90
1Fh	ADCON0	ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON	00-- 0000	65, 90

Legend: — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition,
shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

PIC12F683

TABLE 2-2: PIC12F683 SPECIAL FUNCTION REGISTERS SUMMARY BANK 1

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Page
Bank 1											
80h	INDF									xxxx xxxx	17, 90
81h	OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	12, 90
82h	PCL									0000 0000	17, 90
83h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	TO	PD	Z	DC	C	0001 1xxx	11, 90
84h	FSR									xxxx xxxx	17, 90
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	32, 90
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—						---0 0000	17, 90
8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	13, 90
8Ch	PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	14, 90
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	ULPWUE	SBOREN	—	—	<u>POR</u>	<u>BOR</u>	--01 --qq	16, 90
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS ⁽²⁾	HTS	LTS	SCS	-110 x000	20, 90
90h	OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	24, 90
91h	—	Unimplemented								—	—
92h	PR2									1111 1111	49, 90
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPU ⁽³⁾	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	34, 90
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	34, 90
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	58, 90
9Ah	EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	71, 90
9Bh	EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	0000 0000	71, 90
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	72, 91
9Dh	EECON2									---- ----	72, 91
9Eh	ADRESL									xxxx xxxx	66, 91
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	33, 91

Legend: — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition,
shaded = unimplemented

Note 1: IRP and RP1 bits are reserved, always maintain these bits clear.

2: OSTs bit of the OSCCON register reset to '0' with Dual Speed Start-up and LP, HS or XT selected as the oscillator.

3: GP3 pull-up is enabled when MCLRE is '1' in the Configuration Word register.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- Arithmetic status of the ALU
- Reset status
- Bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uuu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the "Instruction Set Summary".

Note 1: Bits IRP and RP1 of the STATUS register are not used by the PIC12F683 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction.

REGISTER 2-1: STATUS: STATUS REGISTER

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	<u>TO</u>	<u>PD</u>	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	IRP: This bit is reserved and should be maintained as '0'
bit 6	RP1: This bit is reserved and should be maintained as '0'
bit 5	RP0: Register Bank Select bit (used for direct addressing) 1 = Bank 1 (80h – FFh) 0 = Bank 0 (00h – 7Fh)
bit 4	TO: Time-out bit 1 = After power-up, CLRWDAT instruction or SLEEP instruction 0 = A WDT time-out occurred
bit 3	PD: Power-down bit 1 = After power-up or by the CLRWDAT instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions), For Borrow, the polarity is reversed. 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	C: Carry/Borrow bit ⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

PIC12F683

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External GP2/INT interrupt
- TMR0
- Weak pull-ups on GPIO

Note: To achieve a 1:1 prescaler assignment for Timer0, assign the prescaler to the WDT by setting PSA bit of the OPTION register to '1' See **Section 5.1.3 "Software Programmable Prescaler"**.

REGISTER 2-2: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

GPPU: GPIO Pull-up Enable bit

1 = GPIO pull-ups are disabled

0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register

bit 6

INTEDG: Interrupt Edge Select bit

1 = Interrupt on rising edge of INT pin

0 = Interrupt on falling edge of INT pin

bit 5

T0CS: Timer0 Clock Source Select bit

1 = Transition on T0CKI pin

0 = Internal instruction cycle clock (Fosc/4)

bit 4

T0SE: Timer0 Source Edge Select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3

PSA: Prescaler Assignment bit

1 = Prescaler is assigned to the WDT

0 = Prescaler is assigned to the Timer0 module

bit 2-0

PS<2:0>: Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available. See **Section 12.6 "Watchdog Timer (WDT)"** for more information.

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO change and external GP2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GIE | PEIE | TOIE | INTE | GPIE | TOIF | INTF | GPIF |
| bit 7 | bit 0 | | | | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TOIE: Timer0 Overflow Interrupt Enable bit 1 = Enables the Timer0 interrupt 0 = Disables the Timer0 interrupt
bit 4	INTE: GP2/INT External Interrupt Enable bit 1 = Enables the GP2/INT external interrupt 0 = Disables the GP2/INT external interrupt
bit 3	GPIE: GPIO Change Interrupt Enable bit ⁽¹⁾ 1 = Enables the GPIO change interrupt 0 = Disables the GPIO change interrupt
bit 2	TOIF: Timer0 Overflow Interrupt Flag bit ⁽²⁾ 1 = Timer0 register has overflowed (must be cleared in software) 0 = Timer0 register did not overflow
bit 1	INTF: GP2/INT External Interrupt Flag bit 1 = The GP2/INT external interrupt occurred (must be cleared in software) 0 = The GP2/INT external interrupt did not occur
bit 0	GPIF: GPIO Change Interrupt Flag bit 1 = When at least one of the GPIO <5:0> pins changed state (must be cleared in software) 0 = None of the GPIO <5:0> pins have changed state

Note 1: IOC register must also be enabled.

2: TOIF bit is set when TMR0 rolls over. TMR0 is unchanged on Reset and should be initialized before clearing TOIF bit.

PIC12F683

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit

1 = Enables the EE write complete interrupt

0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter (ADC) Interrupt Enable bit

1 = Enables the ADC interrupt

0 = Disables the ADC interrupt

bit 5 **CCP1IE:** CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt

0 = Disables the CCP1 interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **CMIE:** Comparator Interrupt Enable bit

1 = Enables the Comparator 1 interrupt

0 = Disables the Comparator 1 interrupt

bit 2 **OSFIE:** Oscillator Fail Interrupt Enable bit

1 = Enables the oscillator fail interrupt

0 = Disables the oscillator fail interrupt

bit 1 **TMR2IE:** Timer2 to PR2 Match Interrupt Enable bit

1 = Enables the Timer2 to PR2 match interrupt

0 = Disables the Timer2 to PR2 match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit

1 = Enables the Timer1 overflow interrupt

0 = Disables the Timer1 overflow interrupt

2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- | | |
|-------|---|
| bit 7 | EEIF: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started |
| bit 6 | ADIF: A/D Interrupt Flag bit
1 = A/D conversion complete
0 = A/D conversion has not completed or has not been started |
| bit 5 | CCP1IF: CCP1 Interrupt Flag bit
<u>Capture mode:</u>
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
<u>Compare mode:</u>
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
<u>PWM mode:</u>
Unused in this mode |
| bit 4 | Unimplemented: Read as '0' |
| bit 3 | CMIF: Comparator Interrupt Flag bit
1 = Comparator 1 output has changed (must be cleared in software)
0 = Comparator 1 output has not changed |
| bit 2 | OSFIF: Oscillator Fail Interrupt Flag bit
1 = System oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = System clock operating |
| bit 1 | TMR2IF: Timer2 to PR2 Match Interrupt Flag bit
1 = Timer2 to PR2 match occurred (must be cleared in software)
0 = Timer2 to PR2 match has not occurred |
| bit 0 | TMR1IF: Timer1 Overflow Interrupt Flag bit
1 = Timer1 register overflowed (must be cleared in software)
0 = Timer1 has not overflowed |

PIC12F683

2.2.2.6 PCON Register

The Power Control (PCON) register contains flag bits (see Table 12-2) to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the Ultra Low-Power Wake-up and software enable of the BOR.

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	R/W-0	R/W-1	U-0	U-0	R/W-0	R/W-x
—	—	ULPWUE	SBOREN	—	—	<u><u>POR</u></u>	<u><u>BOR</u></u>
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

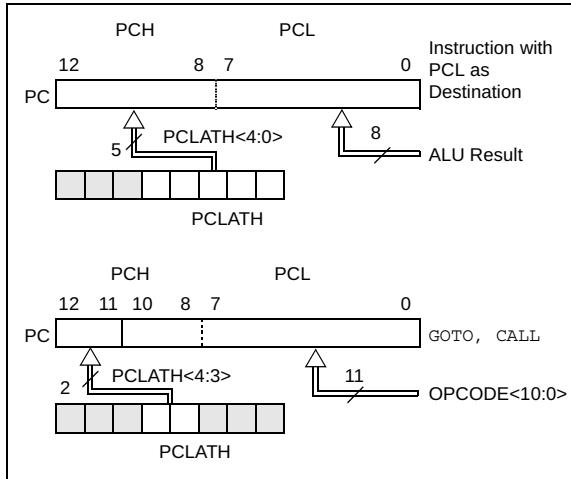
bit 7-6	Unimplemented: Read as '0'
bit 5	ULPWUE: Ultra Low-Power Wake-Up Enable bit 1 = Ultra Low-Power Wake-up enabled 0 = Ultra Low-Power Wake-up disabled
bit 4	SBOREN: Software BOR Enable bit ⁽¹⁾ 1 = BOR enabled 0 = BOR disabled
bit 3-2	Unimplemented: Read as '0'
bit 1	POR: Power-on Reset Status bit 1 = No Power-on Reset occurred 0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)
bit 0	BOR: Brown-out Reset Status bit 1 = No Brown-out Reset occurred 0 = A Brown-out Reset occurred (must be set in software after a Power-on Reset or Brown-out Reset occurs)

Note 1: Set BOREN<1:0> = 01 in the Configuration Word register for this bit to control the BOR.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte ($PC<12:8>$) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL ($PCLATH<4:0> \rightarrow PCH$). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction ($PCLATH<4:3> \rightarrow PCH$).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note AN556, "Implementing a Table Read" (DS00556).

2.3.2 STACK

The PIC12F683 family has an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit of the STATUS register, as shown in Figure 2-4.

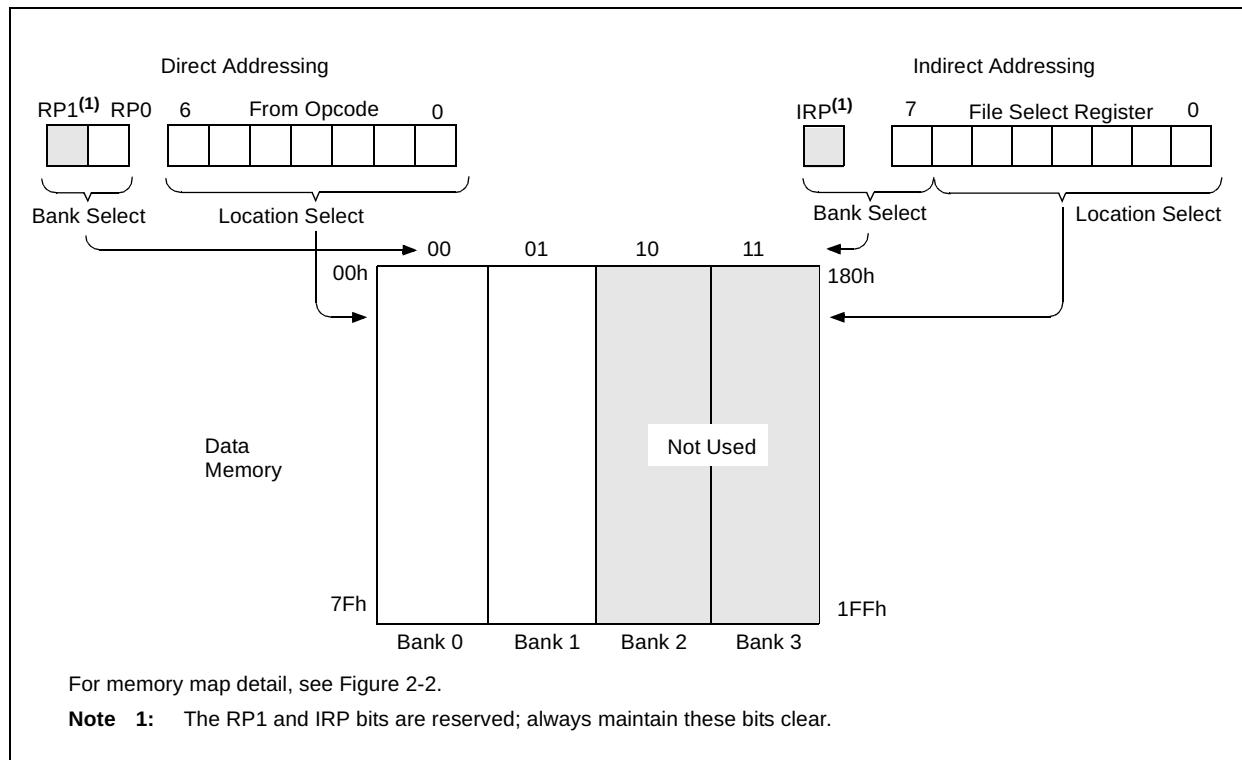
A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

MOVLW	0x20	; initialize pointer
MOVWF	FSR	; to RAM
NEXT	CLRF	INDF ;clear INDF register
	INCF	FSR ;inc pointer
	BTFSS	FSR, 4 ;all done?
	GOTO	NEXT ;no clear next
		CONTINUE ;yes continue

PIC12F683

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC12F683



3.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

3.1 Overview

The Oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 3-1 illustrates a block diagram of the Oscillator module.

Clock sources can be configured from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be configured from one of two internal oscillators, with a choice of speeds selectable via software. Additional clock features include:

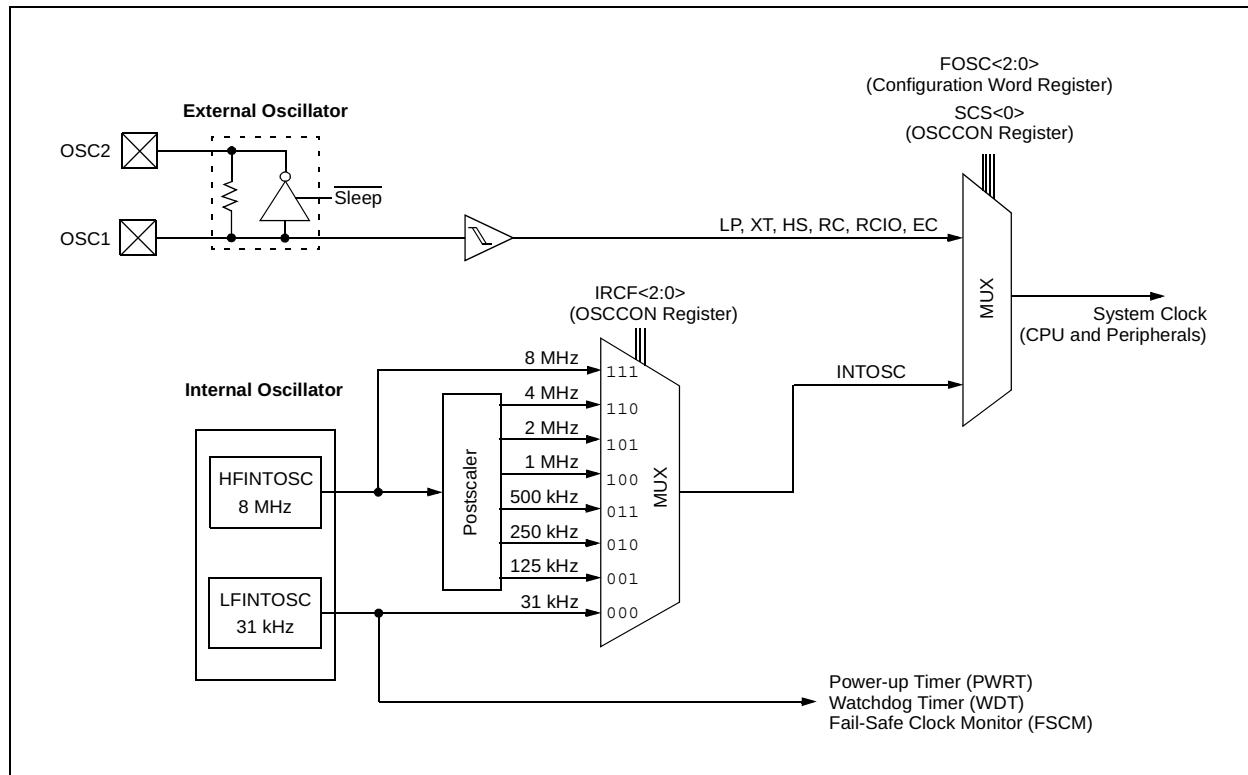
- Selectable system clock source between external or internal via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.

The Oscillator module can be configured in one of eight clock modes.

1. EC – External clock with I/O on OSC2/CLKOUT.
2. LP – 32 kHz Low-Power Crystal mode.
3. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode.
4. HS – High Gain Crystal or Ceramic Resonator mode.
5. RC – External Resistor-Capacitor (RC) with Fosc/4 output on OSC2/CLKOUT.
6. RCIO – External Resistor-Capacitor (RC) with I/O on OSC2/CLKOUT.
7. INTOSC – Internal oscillator with Fosc/4 output on OSC2 and I/O on OSC1/CLKIN.
8. INTSCIO – Internal oscillator with I/O on OSC1/CLKIN and OSC2/CLKOUT.

Clock Source modes are configured by the FOSC<2:0> bits in the Configuration Word register (CONFIG). The internal clock can be generated from two internal oscillators. The HFINTOSC is a calibrated high-frequency oscillator. The LFINTOSC is an uncalibrated low-frequency oscillator.

FIGURE 3-1: PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



PIC12F683

3.2 Oscillator Control

The Oscillator Control (OSCCON) register (Figure 3-1) controls the system clock and frequency selection options. The OSCCON register contains the following bits:

- Frequency selection bits (IRCF)
- Frequency Status bits (HTS, LTS)
- System clock control bits (OSTS, SCS)

REGISTER 3-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R/W-1	R/W-1	R/W-0	R-1	R-0	R-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS ⁽¹⁾	HTS	LTS	SCS
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	Unimplemented: Read as '0'
bit 6-4	IRCF<2:0>: Internal Oscillator Frequency Select bits 111 = 8 MHz 110 = 4 MHz (default) 101 = 2 MHz 100 = 1 MHz 011 = 500 kHz 010 = 250 kHz 001 = 125 kHz 000 = 31 kHz (LFINTOSC)
bit 3	OSTS: Oscillator Start-up Time-out Status bit ⁽¹⁾ 1 = Device is running from the external clock defined by FOSC<2:0> of the Configuration Word register 0 = Device is running from the internal oscillator (HFINTOSC or LFINTOSC)
bit 2	HTS: HFINTOSC Status bit (High Frequency – 8 MHz to 125 kHz) 1 = HFINTOSC is stable 0 = HFINTOSC is not stable
bit 1	LTS: LFINTOSC Stable bit (Low Frequency – 31 kHz) 1 = LFINTOSC is stable 0 = LFINTOSC is not stable
bit 0	SCS: System Clock Select bit 1 = Internal oscillator is used for system clock 0 = Clock source defined by FOSC<2:0> of the Configuration Word register

Note 1: Bit resets to '0' with Two-Speed Start-up and LP, XT or HS selected as the Oscillator mode or Fail-Safe mode is enabled.

3.3 Clock Source Modes

Clock Source modes can be classified as external or internal.

- External Clock modes rely on external circuitry for the clock source. Examples are: Oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.
- Internal clock sources are contained internally within the Oscillator module. The Oscillator module has two internal oscillators: the 8 MHz High-Frequency Internal Oscillator (HFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bit of the OSCCON register. See **Section 3.6 “Clock Switching”** for additional information.

3.4 External Clock Modes

3.4.1 OSCILLATOR START-UP TIMER (OST)

If the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the Oscillator module. When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 3-1.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 3.7 “Two-Speed Clock Start-up Mode”**).

TABLE 3-1: OSCILLATOR DELAY EXAMPLES

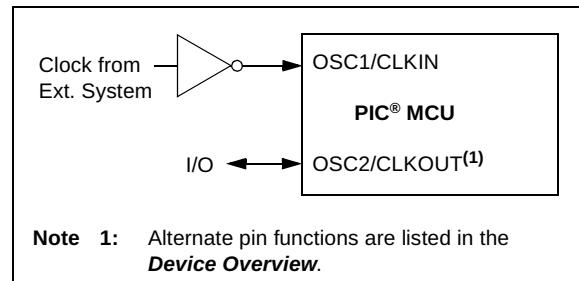
Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC HFINTOSC	31 kHz 125 kHz to 8 MHz	Oscillator Warm-Up Delay (TWARM)
Sleep/POR	EC, RC	DC – 20 MHz	2 instruction cycles
LFINTOSC (31 kHz)	EC, RC	DC – 20 MHz	1 cycle of each
Sleep/POR	LP, XT, HS	32 kHz to 20 MHz	1024 Clock Cycles (OST)
LFINTOSC (31 kHz)	HFINTOSC	125 kHz to 8 MHz	1 μ s (approx.)

3.4.2 EC MODE

The External Clock (EC) mode allows an externally generated logic level as the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input and the OSC2 is available for general purpose I/O. Figure 3-2 shows the pin connections for EC mode.

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 3-2: EXTERNAL CLOCK (EC) MODE OPERATION



PIC12F683

3.4.3 LP, XT, HS MODES

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 3-3). The mode selects a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

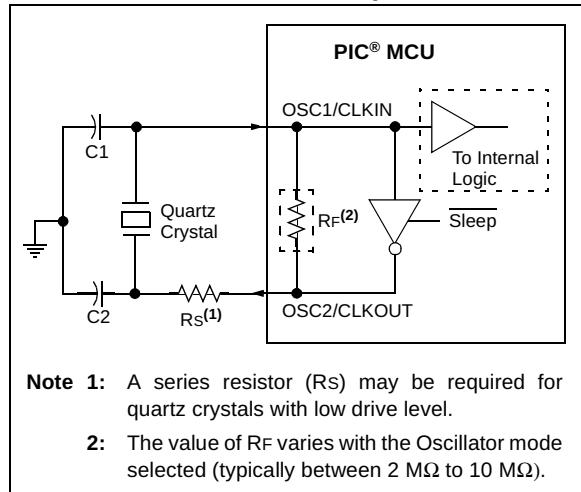
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 3-3 and Figure 3-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

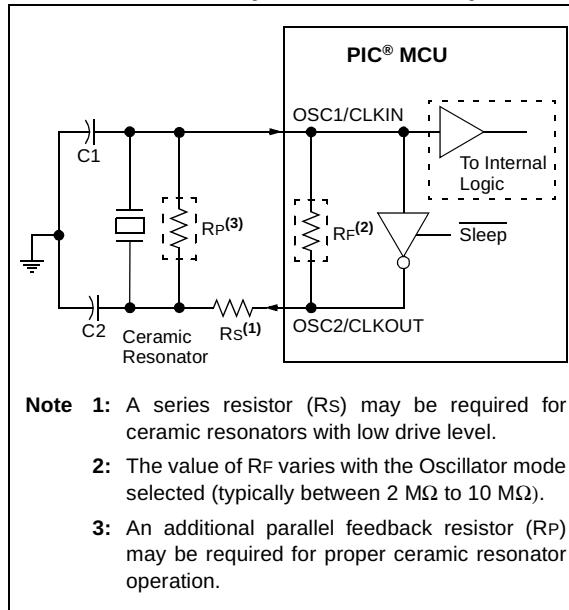
FIGURE 3-3: QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

- 2:** Always verify oscillator performance over the VDD and temperature range that is expected for the application.
- 3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices" (DS00826)
 - AN849, "Basic PIC® Oscillator Design" (DS00849)
 - AN943, "Practical PIC® Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 3-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)

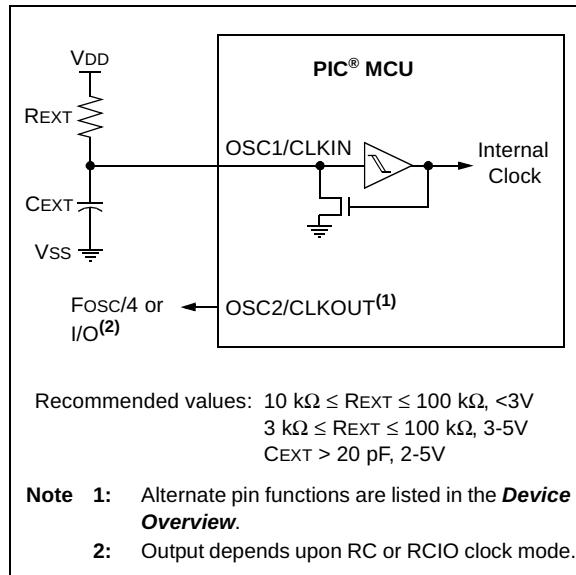


3.4.4 EXTERNAL RC MODES

The external Resistor-Capacitor (RC) modes support the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required. There are two modes: RC and RCIO.

In RC mode, the RC circuit connects to OSC1. OSC2/CLKOUT outputs the RC oscillator frequency divided by 4. This signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements. Figure 3-5 shows the external RC mode connections.

FIGURE 3-5: EXTERNAL RC MODES



In RCIO mode, the RC circuit is connected to OSC1. OSC2 becomes an additional general purpose I/O pin.

The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. Other factors affecting the oscillator frequency are:

- threshold voltage variation
- component tolerances
- packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

3.5 Internal Clock Modes

The Oscillator module has two independent, internal oscillators that can be configured or selected as the system clock source.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 8 MHz. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 3-2).
2. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register.

The system clock can be selected between external or internal clock sources via the System Clock Selection (SCS) bit of the OSCCON register. See **Section 3.6 “Clock Switching”** for more information.

3.5.1 INTOSC AND INTOSCI MODES

The INTOSC and INTOSCI modes configure the internal oscillators as the system clock source when the device is programmed using the oscillator selection or the FOSC<2:0> bits in the Configuration Word register (CONFIG). See **Section 12.0 “Special Features of the CPU”** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT outputs the selected internal oscillator frequency divided by 4. The CLKOUT signal may be used to provide a clock for external circuitry, synchronization, calibration, test or other application requirements.

In **INTOSCI** mode, OSC1/CLKIN and OSC2/CLKOUT are available for general purpose I/O.

3.5.2 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 8 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 3-2).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). One of seven frequencies can be selected via software using the IRCF<2:0> bits of the OSCCON register. See **Section 3.5.4 “Frequency Select Bits (IRCF)”** for more information.

The HFINTOSC is enabled by selecting any frequency between 8 MHz and 125 kHz by setting the IRCF<2:0> bits of the OSCCON register ≠ 000. Then, set the System Clock Source (SCS) bit of the OSCCON register to ‘1’ or enable Two-Speed Start-up by setting the IESO bit in the Configuration Word register (CONFIG) to ‘1’.

The HF Internal Oscillator (HTS) bit of the OSCCON register indicates whether the HFINTOSC is stable or not.

PIC12F683

3.5.2.1 OSCTUNE Register

The HFINTOSC is factory calibrated but can be adjusted in software by writing to the OSCTUNE register (Register 3-2).

The default value of the OSCTUNE register is '0'. The value is a 5-bit two's complement number.

When the OSCTUNE register is modified, the HFINTOSC frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

REGISTER 3-2: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **TUN<4:0>:** Frequency Tuning bits

01111 = Maximum frequency

01110 =

•

•

•

00001 =

00000 = Oscillator module is running at the calibrated frequency.

11111 =

•

•

•

10000 = Minimum frequency

3.5.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). Select 31 kHz, via software, using the IRCF<2:0> bits of the OSCCON register. See **Section 3.5.4 “Frequency Select Bits (IRCF)**” for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<2:0> bits of the OSCCON register = 000) as the system clock source (SCS bit of the OSCCON register = 1), or when any of the following are enabled:

- Two-Speed Start-up IESO bit of the Configuration Word register = 1 and IRCF<2:0> bits of the OSCCON register = 000
- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The LF Internal Oscillator (LTS) bit of the OSCCON register indicates whether the LFINTOSC is stable or not.

3.5.4 FREQUENCY SELECT BITS (IRCF)

The output of the 8 MHz HFINTOSC and 31 kHz LFINTOSC connects to a postscaler and multiplexer (see Figure 3-1). The Internal Oscillator Frequency Select bits IRCF<2:0> of the OSCCON register select the frequency output of the internal oscillators. One of eight frequencies can be selected via software:

- 8 MHz
- 4 MHz (Default after Reset)
- 2 MHz
- 1 MHz
- 500 kHz
- 250 kHz
- 125 kHz
- 31 kHz (LFINTOSC)

Note: Following any Reset, the IRCF<2:0> bits of the OSCCON register are set to ‘110’ and the frequency selection is set to 4 MHz. The user can modify the IRCF bits to select a different frequency.

3.5.5 HF AND LF INTOSC CLOCK SWITCH TIMING

When switching between the LFINTOSC and the HFINTOSC, the new oscillator may already be shut down to save power (see Figure 3-6). If this is the case, there is a delay after the IRCF<2:0> bits of the OSCCON register are modified before the frequency selection takes place. The LTS and HTS bits of the OSCCON register will reflect the current active status of the LFINTOSC and HFINTOSC oscillators. The timing of a frequency selection is as follows:

1. IRCF<2:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. CLKOUT is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. CLKOUT is now connected with the new clock. LTS and HTS bits of the OSCCON register are updated as required.
6. Clock switch is complete.

See Figure 3-1 for more details.

If the internal oscillator speed selected is between 8 MHz and 125 kHz, there is no start-up delay before the new frequency is selected. This is because the old and new frequencies are derived from the HFINTOSC via the postscaler and multiplexer.

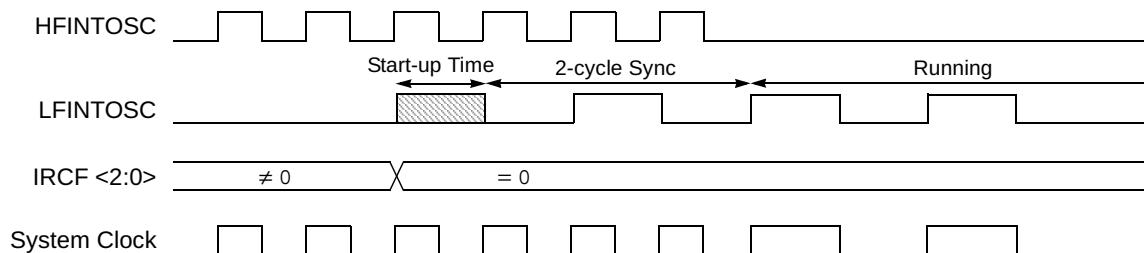
Start-up delay specifications are located in the **Electrical Specifications Chapter of this data sheet, under AC Specifications (Oscillator Module)**.

PIC12F683

FIGURE 3-6: INTERNAL OSCILLATOR SWITCH TIMING

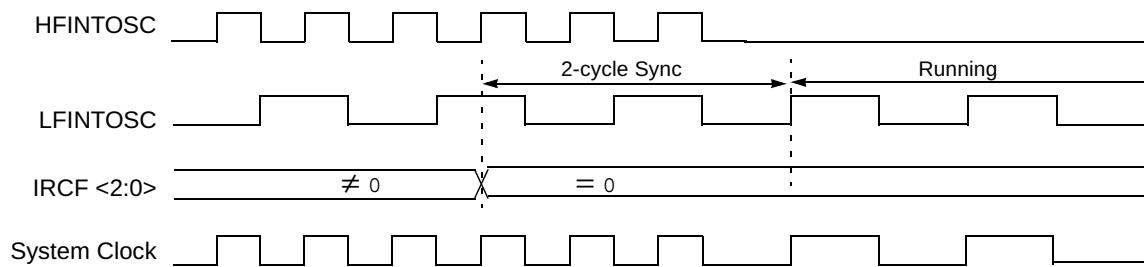
HF → LF⁽¹⁾

HFINTOSC → LFINTOSC (FSCM and WDT disabled)



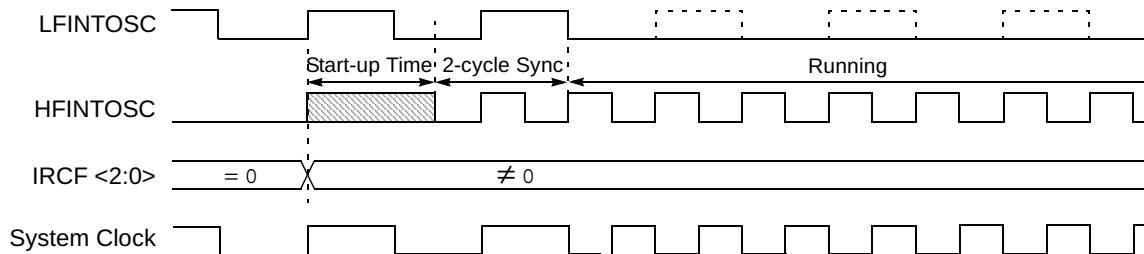
Note 1: When going from LF to HF.

HFINTOSC → LFINTOSC (Either FSCM or WDT enabled)



LFINTOSC → HFINTOSC

LFINTOSC turns off unless WDT or FSCM is enabled



3.6 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bit of the OSCCON register.

3.6.1 SYSTEM CLOCK SELECT (SCS) BIT

The System Clock Select (SCS) bit of the OSCCON register selects the system clock source that is used for the CPU and peripherals.

- When the SCS bit of the OSCCON register = 0, the system clock source is determined by configuration of the FOSC<2:0> bits in the Configuration Word register (CONFIG).
- When the SCS bit of the OSCCON register = 1, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<2:0> bits of the OSCCON register. After a Reset, the SCS bit of the OSCCON register is always cleared.

Note: Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bit of the OSCCON register. The user can monitor the OSTS bit of the OSCCON register to determine the current system clock source.

3.6.2 OSCILLATOR START-UP TIME-OUT STATUS (OSTS) BIT

The Oscillator Start-up Time-out Status (OSTS) bit of the OSCCON register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes.

3.7 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device.

This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCCON register to remain clear.

When the Oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) is enabled (see **Section 3.4.1 “Oscillator Start-up Timer (OST)”**). The OST will suspend program execution until 1024 oscillations are counted. Two-Speed Start-up mode minimizes the delay in code execution by operating from the internal oscillator as the OST is counting. When the OST count reaches 1024 and the OSTS bit of the OSCCON register is set, program execution switches to the external oscillator.

3.7.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word register) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 0.
- FOSC<2:0> bits in the Configuration Word register (CONFIG) configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

If the external clock oscillator is configured to be anything other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

3.7.2 TWO-SPEED START-UP SEQUENCE

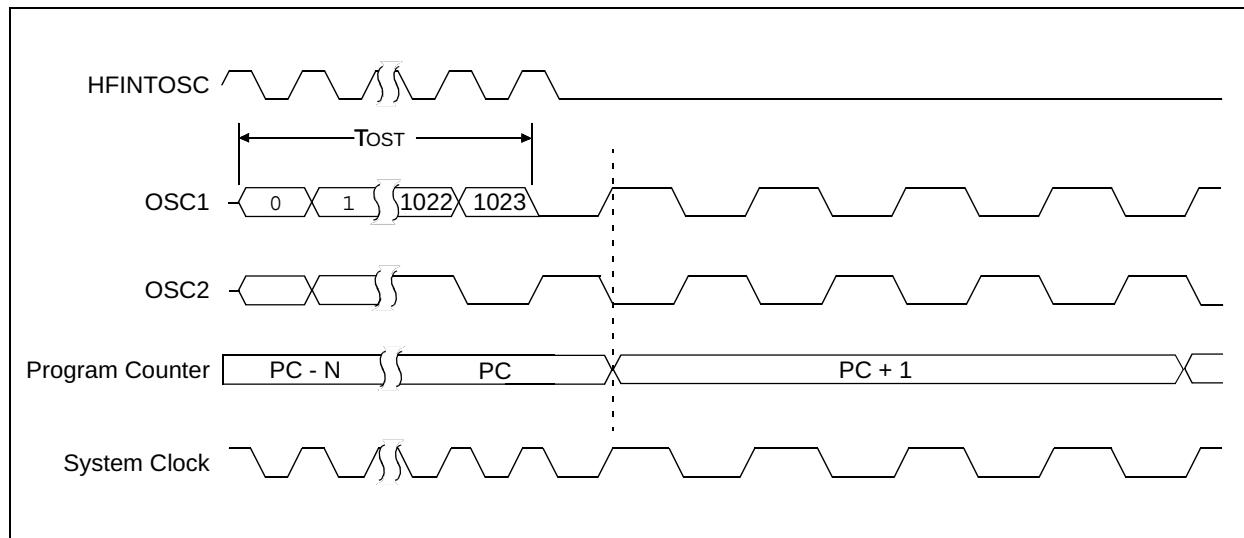
- Wake-up from Power-on Reset or Sleep.
- Instructions begin execution by the internal oscillator at the frequency set in the IRCF<2:0> bits of the OSCCON register.
- OST enabled to count 1024 clock cycles.
- OST timed out, wait for falling edge of the internal oscillator.
- OSTS is set.
- System clock held low until the next falling edge of new clock (LP, XT or HS mode).
- System clock is switched to external clock source.

PIC12F683

3.7.3 CHECKING TWO-SPEED CLOCK STATUS

Checking the state of the OSTS bit of the OSCCON register will confirm if the microcontroller is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Word register (CONFIG), or the internal oscillator.

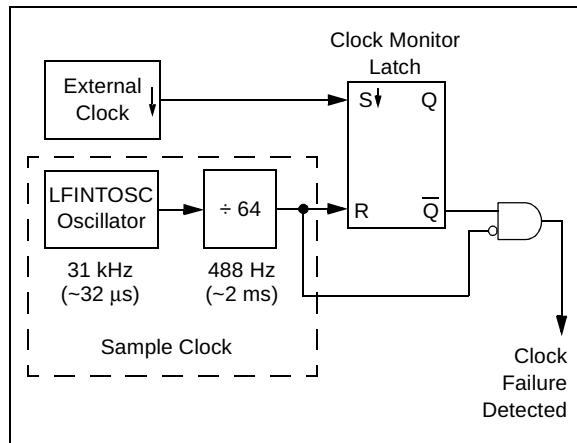
FIGURE 3-7: TWO-SPEED START-UP



3.8 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word register (CONFIG). The FSCM is applicable to all external oscillator modes (LP, XT, HS, EC, RC and RCIO).

FIGURE 3-8: FSCM BLOCK DIAGRAM



3.8.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 3-8. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the primary clock goes low.

3.8.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<2:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

3.8.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or toggling the SCS bit of the OSCCON register. When the SCS bit is toggled, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared and the device will be operating from the external clock source. The Fail-Safe condition must be cleared before the OSFIF flag can be cleared.

3.8.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the OSTS bit of the OSCCON register to verify the oscillator start-up and that the system clock switchover has successfully completed.

PIC12F683

FIGURE 3-9: FSCM TIMING DIAGRAM

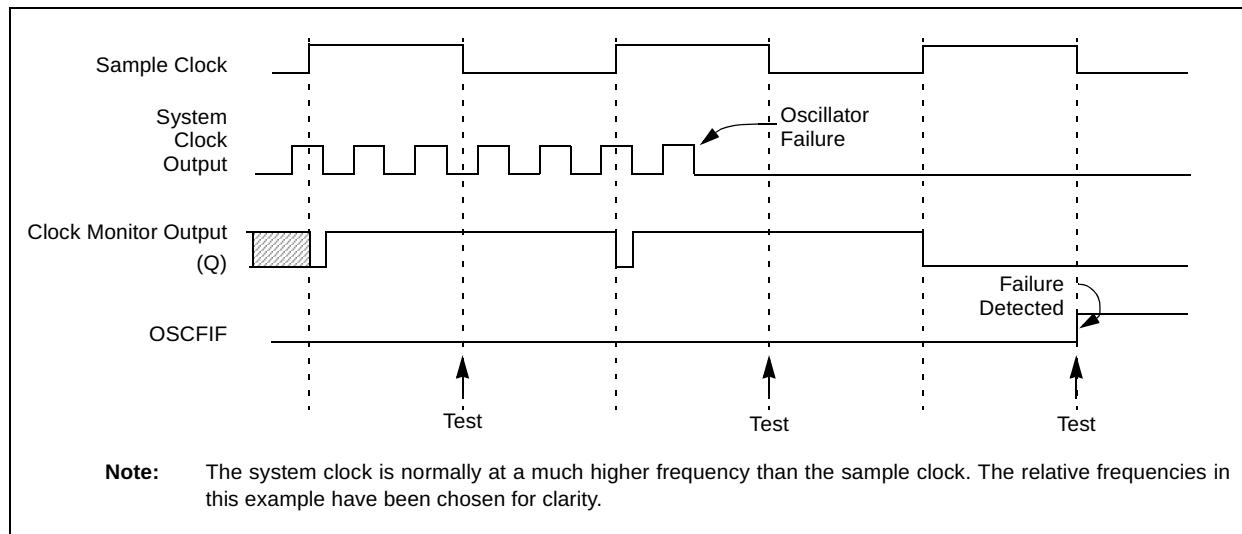


TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR ⁽¹⁾	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	0000 000x
OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	HTS	LTS	SCS	-110 x000	-110 x000
OSCTUNE	—	—	—	TUN4	TUN3	TUN2	TUN1	TUN0	---0 0000	---u uuuu
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by oscillators.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

4.0 GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

4.1 GPIO and the TRISIO Registers

GPIO is a 6-bit wide, bidirectional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). An exception is GP3, which is input only and its TRISIO bit will always read as '1'. Example 4-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations.

Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch. GP3 reads '0' when MCLRE = 1.

The TRISIO register controls the direction of the GPIO pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

Note: The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'.

EXAMPLE 4-1: INITIALIZING GPIO

```
BANKSEL    GPIO          ;  
CLRF      GPIO          ;Init GPIO  
MOVLW    07h           ;Set GP<2:0> to  
MOVWF    CMCON0        ;digital I/O  
BANKSEL    ANSEL         ;  
CLRF      ANSEL        ;digital I/O  
MOVLW    0Ch            ;Set GP<3:2> as inputs  
MOVWF    TRISIO        ;and set GP<5:4,1:0>  
                      ;as outputs
```

REGISTER 4-1: GPIO: GENERAL PURPOSE I/O REGISTER

U-0	U-0	R/W-x	R/W-0	R-x	R/W-0	R/W-0	R/W-0
—	—	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **GP<5:0>:** GPIO I/O Pin bit

1 = Port pin is > VIH

0 = Port pin is < VIL

REGISTER 4-2: TRISIO GPIO TRI-STATE REGISTER

U-0	U-0	R/W-1	R/W-1	R-1	R/W-1	R/W-1	R/W-1
—	—	TRISIO5 ^(2,3)	TRISIO4 ⁽²⁾	TRISIO3 ⁽¹⁾	TRISIO2	TRISIO1	TRISIO0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7:6	Unimplemented: Read as '0'
bit 5:4	TRISIO<5:4>: GPIO Tri-State Control bit 1 = GPIO pin configured as an input (tri-stated) 0 = GPIO pin configured as an output
bit 3	TRISIO<3>: GPIO Tri-State Control bit Input only
bit 2:0	TRISIO<2:0>: GPIO Tri-State Control bit 1 = GPIO pin configured as an input (tri-stated) 0 = GPIO pin configured as an output

- Note 1:** TRISIO<3> always reads '1'.
2: TRISIO<5:4> always reads '1' in XT, HS and LP OSC modes.
3: TRISIO<5> always reads '1' in RC and RCIO and EC modes.

4.2 Additional Pin Functions

Every GPIO pin on the PIC12F683 has an interrupt-on-change option and a weak pull-up option. GP0 has an Ultra Low-Power Wake-up option. The next three sections describe these functions.

4.2.1 ANSEL REGISTER

The ANSEL register is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSEL bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSEL bits has no affect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

4.2.2 WEAK PULL-UPS

Each of the GPIO pins, except GP3, has an individually configurable internal weak pull-up. Control bits WPUx enable or disable each pull-up. Refer to Register 4-4. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the GPPU bit of the OPTION register). A weak pull-up is automatically enabled for GP3 when configured as MCLR and disabled when GP3 is an I/O. There is no software control of the MCLR pull-up.

4.2.3 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOCx enable or disable the interrupt function for each pin. Refer to Register 4-5. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The 'mismatch' outputs of the last read are OR'd together to set the GPIO Change Interrupt Flag bit (GPIF) in the INTCON register (Register 2-3).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, clears the interrupt by:

- Any read or write of GPIO. This will end the mismatch condition, then,
- Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared. The latch holding the last read value is not affected by a MCLR nor Brown-out Reset. After these resets, the GPIF flag will continue to be set if a mismatch is present.

Note: If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.

REGISTER 4-3: ANSEL: ANALOG SELECT REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'bit 6-4 **ADCS<2:0>:** A/D Conversion Clock Select bits

000 = Fosc/2

001 = Fosc/8

010 = Fosc/32

x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

100 = Fosc/4

101 = Fosc/16

110 = Fosc/64

bit 3-0 **ANS<3:0>:** Analog Select bits

Analog select between analog or digital function on pins AN<3:0>, respectively.

1 = Analog input. Pin is assigned as analog input⁽¹⁾.

0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups and interrupt-on-change, if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

PIC12F683

REGISTER 4-4: WPU: WEAK PULL-UP REGISTER

U-0	U-0	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **WPU<5:4>:** Weak Pull-up Control bits

1 = Pull-up enabled

0 = Pull-up disabled

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **WPU<2:0>:** Weak Pull-up Control bits

1 = Pull-up enabled

0 = Pull-up disabled

Note 1: Global GPPU must be enabled for individual pull-ups to be enabled.

2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).

3: The GP3 pull-up is enabled when configured as MCLR and disabled as an I/O in the Configuration Word.

4: WPU<5:4> always reads '1' in XT, HS and LP OSC modes.

REGISTER 4-5: IOC: INTERRUPT-ON-CHANGE GPIO REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOC<5:0>:** Interrupt-on-change GPIO Control bits

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

Note 1: Global Interrupt Enable (GIE) must be enabled for individual interrupts to be recognized.

2: IOC<5:4> always reads '0' in XT, HS and LP OSC modes.

4.2.4 ULTRA LOW-POWER WAKE-UP

The Ultra Low-Power Wake-up (ULPWU) on GP0 allows a slow falling voltage to generate an interrupt-on-change on GP0 without excess current consumption. The mode is selected by setting the ULPWUE bit of the PCON register. This enables a small current sink which can be used to discharge a capacitor on GP0.

To use this feature, the GP0 pin is configured to output '1' to charge the capacitor, interrupt-on-change for GP0 is enabled and GP0 is configured as an input. The ULPWUE bit is set to begin the discharge and a SLEEP instruction is performed. When the voltage on GP0 drops below VIL, an interrupt will be generated which will cause the device to wake-up. Depending on the state of the GIE bit of the INTCON register, the device will either jump to the interrupt vector (0004h) or execute the next instruction when the interrupt event occurs. See **Section 4.2.3 “Interrupt-on-Change”** and **Section 12.4.3 “GPIO Interrupt”** for more information.

This feature provides a low-power technique for periodically waking up the device from Sleep. The time-out is dependent on the discharge time of the RC circuit on GP0. See Example 4-2 for initializing the Ultra Low-Power Wake-up module.

The series resistor provides overcurrent protection for the GP0 pin and can allow for software calibration of the time-out (see Figure 4-1). A timer can be used to measure the charge time and discharge time of the capacitor. The charge time can then be adjusted to provide the desired interrupt delay. This technique will compensate for the affects of temperature, voltage and component accuracy. The Ultra Low-Power Wake-up peripheral can also be configured as a simple Programmable Low-Voltage Detect or temperature sensor.

Note: For more information, refer to the Application Note AN879, "Using the Microchip Ultra Low-Power Wake-up Module" (DS00879).

EXAMPLE 4-2: ULTRA LOW-POWER WAKE-UP INITIALIZATION

```
BANKSEL CMCON0      ;  
MOVLW H'7'          ;Turn off  
MOVWF CMCON0        ;comparators  
BANKSEL ANSEL       ;  
BCF   ANSEL,0        ;RA0 to digital I/O  
BCF   TRISA,0        ;Output high to  
BANKSEL PORTA       ;  
BSF   PORTA,0        ;charge capacitor  
CALL  CapDelay      ;  
BANKSEL PCON         ;  
BSF   PCON,ULPWUE   ;Enable ULP Wake-up  
BSF   IOCA,0          ;Select RA0 IOC  
BSF   TRISA,0        ;RA0 to input  
MOVLW B'10001000'    ;Enable interrupt  
MOVWF INTCON         ; and clear flag  
SLEEP                 ;Wait for IOC  
NOP                  ;
```

PIC12F683

4.2.5 PIN DESCRIPTIONS AND DIAGRAMS

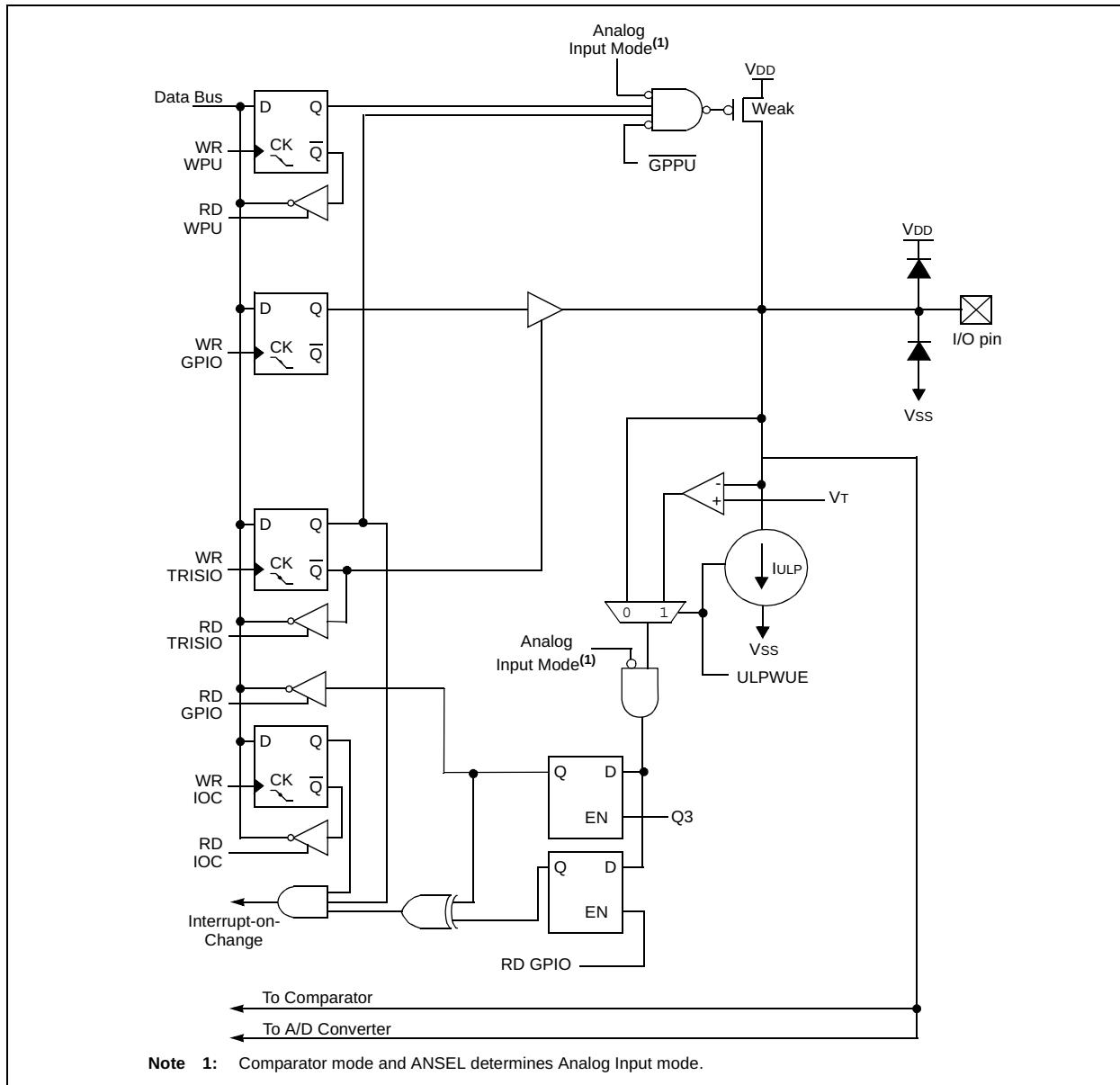
Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the ADC, refer to the appropriate section in this data sheet.

4.2.5.1 GP0/AN0/CIN+/ICSPDAT/ULPWU

Figure 4-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input to the comparator
- In-Circuit Serial Programming™ data
- an analog input to the Ultra Low-Power Wake-up

FIGURE 4-1: BLOCK DIAGRAM OF GP0

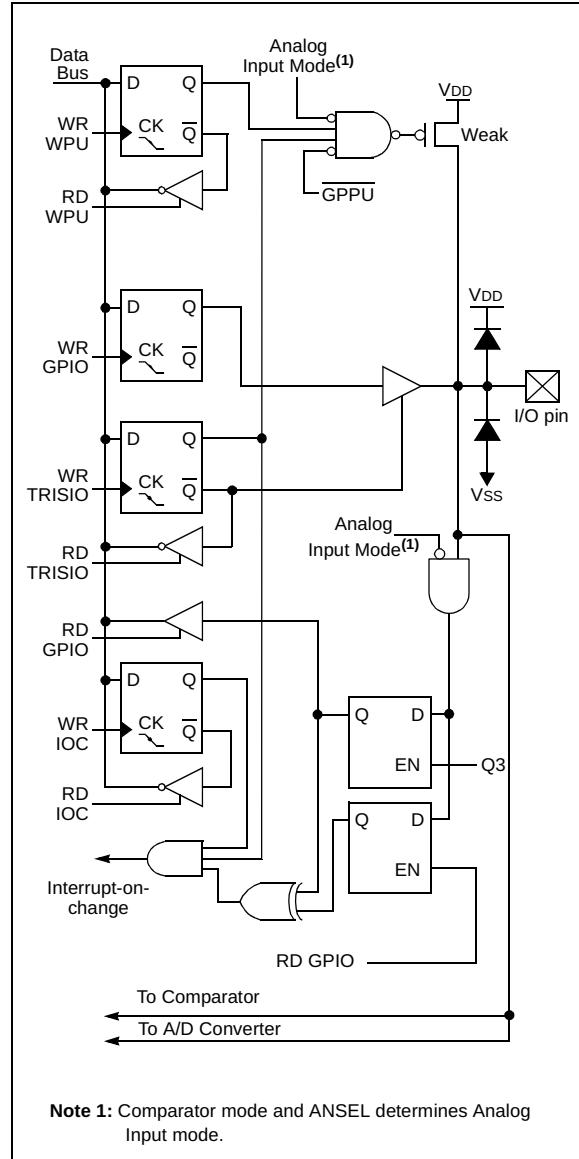


4.2.5.2 GP1/AN1/CIN-/VREF/ICSPCLK

Figure 4-2 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- an analog input to the comparator
- a voltage reference input for the ADC
- In-Circuit Serial Programming clock

FIGURE 4-2: BLOCK DIAGRAM OF GP1

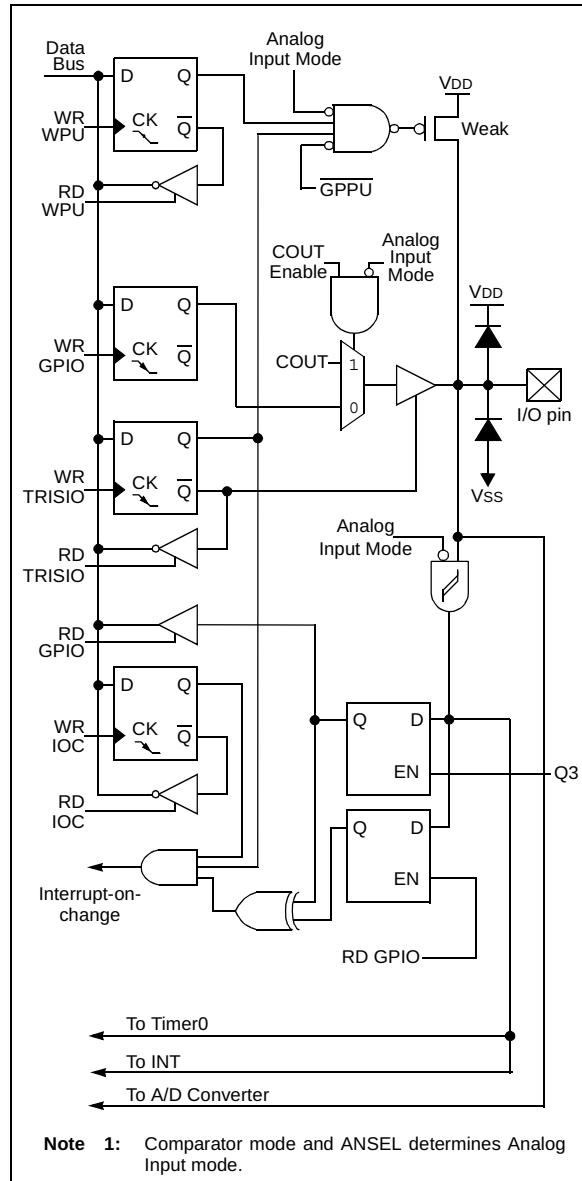


4.2.5.3 GP2/AN2/T0CKI/INT/COUT/CCP1

Figure 4-3 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- the clock input for Timer0
- an external edge triggered interrupt
- a digital output from the Comparator
- a digital input/output for the CCP (refer to Section 11.0 “Capture/Compare/PWM (CCP) Module”).

FIGURE 4-3: BLOCK DIAGRAM OF GP2



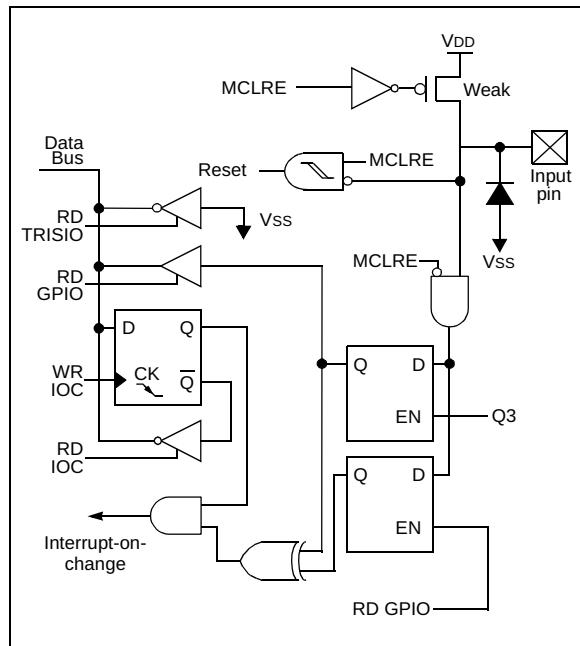
PIC12F683

4.2.5.4 GP3/MCLR/VPP

Figure 4-4 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset with weak pull-up

FIGURE 4-4: BLOCK DIAGRAM OF GP3

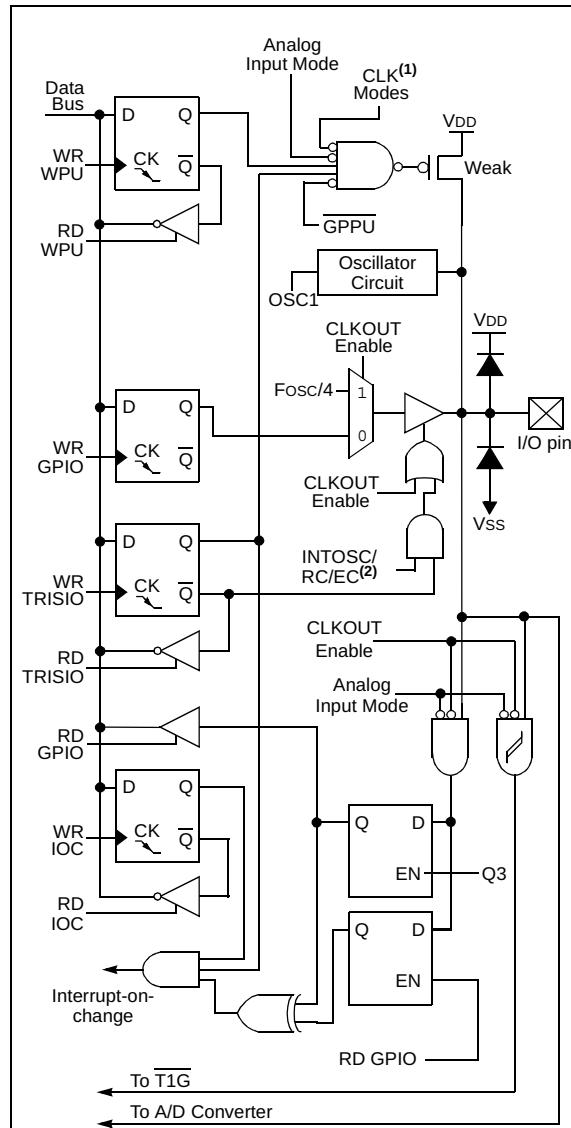


4.2.5.5 GP4/AN3/T1G/OSC2/CLKOUT

Figure 4-5 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the ADC
- a Timer1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 4-5: BLOCK DIAGRAM OF GP4



Note 1: CLK modes are XT, HS, LP, optional LP oscillator and CLKOUT Enable.

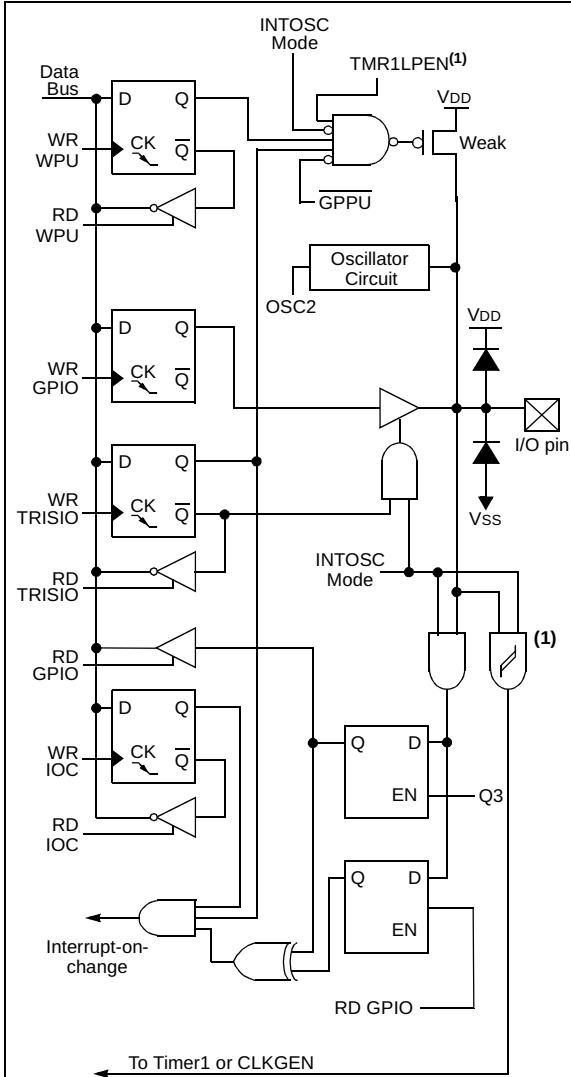
2: With CLKOUT option.

4.2.5.6 GP5/T1CKI/OSC1/CLKIN

Figure 4-6 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a Timer1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 4-6: BLOCK DIAGRAM OF GP5



Note 1: Timer1 LP oscillator enabled.

2: When using Timer1 with LP oscillator, the Schmitt Trigger is bypassed.

TABLE 4-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
PCON	—	—	ULPWUE	SBOREN	—	—	POR	BOR	--01 --qq	--0u --uu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--x0 x000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	0000 0000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	--11 -111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by GPIO.

PIC12F683

NOTES:

5.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (shared with Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt on overflow

Figure 5-1 is a block diagram of the Timer0 module.

5.1 Timer0 Operation

When used as a timer, the Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

5.1.1 8-BIT TIMER MODE

When used as a timer, the Timer0 module will increment every instruction cycle (without prescaler). Timer mode is selected by clearing the T0CS bit of the OPTION register to '0'.

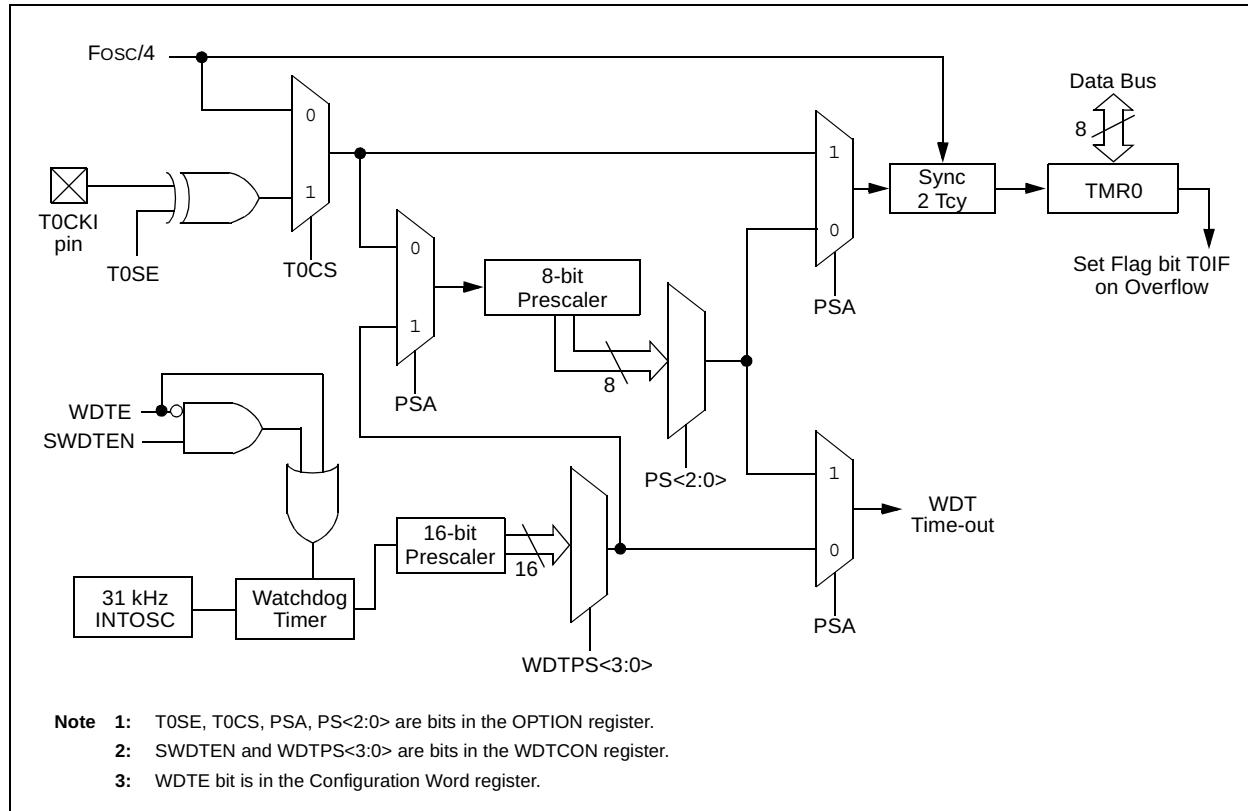
When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note: The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

5.1.2 8-BIT COUNTER MODE

When used as a counter, the Timer0 module will increment on every rising or falling edge of the TOCKI pin. The incrementing edge is determined by the TOSE bit of the OPTION register. Counter mode is selected by setting the T0CS bit of the OPTION register to '1'.

FIGURE 5-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



5.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A single software programmable prescaler is available for use with either Timer0 or the Watchdog Timer (WDT), but not both simultaneously. The prescaler assignment is controlled by the PSA bit of the OPTION register. To assign the prescaler to Timer0, the PSA bit must be cleared to a '0'.

There are 8 prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be assigned to the WDT module.

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMRO register will clear the prescaler.

When the prescaler is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.

5.1.3.1 Switching Prescaler Between Timer0 and WDT Modules

As a result of having the prescaler assigned to either Timer0 or the WDT, it is possible to generate an unintended device Reset when switching prescaler values. When changing the prescaler assignment from Timer0 to the WDT module, the instruction sequence shown in Example 5-1, must be executed.

EXAMPLE 5-1: CHANGING PRESCALER (TIMER0 → WDT)

```
BANKSEL TMRO      ;  
CLRWDT           ;Clear WDT  
CLRF  TMRO       ;Clear TMRO and  
                 ;prescaler  
BANKSEL OPTION_REG ;  
BSF   OPTION_REG, PSA ;Select WDT  
CLRWDT           ;  
                 ;  
MOVLW  b'11111000' ;Mask prescaler  
ANDWF  OPTION_REG,W ;bits  
IORLW  b'00000101' ;Set WDT prescaler  
MOVWF  OPTION_REG ;to 1:32
```

When changing the prescaler assignment from the WDT to the Timer0 module, the following instruction sequence must be executed (see Example 5-2).

EXAMPLE 5-2: CHANGING PRESCALER (WDT → TIMER0)

```
CLRWDT           ;Clear WDT and  
                 ;prescaler  
BANKSEL OPTION_REG ;  
MOVLW  b'11110000' ;Mask TMRO select and  
ANDWF  OPTION_REG,W ;prescaler bits  
IORLW  b'00000011' ;Set prescale to 1:16  
MOVWF  OPTION_REG ;
```

5.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMRO register overflows from FFh to 00h. The TOIF interrupt flag bit of the INTCON register is set every time the TMRO register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TOIF bit must be cleared in software. The Timer0 interrupt enable is the TOIE bit of the INTCON register.

Note: The Timer0 interrupt cannot wake the processor from Sleep since the timer is frozen during Sleep.

5.1.5 USING TIMER0 WITH AN EXTERNAL CLOCK

When Timer0 is in Counter mode, the synchronization of the T0CKI input and the Timer0 register is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, the high and low periods of the external clock source must meet the timing requirements as shown in the **Section 15.0 “Electrical Specifications”**.

REGISTER 5-1: OPTION_REG: OPTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7	GPPU: GPIO Pull-up Enable bit 1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual PORT latch values in WPU register
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of INT pin 0 = Interrupt on falling edge of INT pin
bit 5	T0CS: Timer0 Clock Source Select bit 1 = Transition on T0CKI pin 0 = Internal instruction cycle clock (Fosc/4)
bit 4	T0SE: Timer0 Source Edge Select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module
bit 2-0	PS<2:0>: Prescaler Rate Select bits

BIT VALUE	TIMER0 RATE	WDT RATE
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Note 1: A dedicated 16-bit WDT postscaler is available. See **Section 12.6 “Watchdog Timer (WDT)”** for more information.

TABLE 5-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Timer0 module.

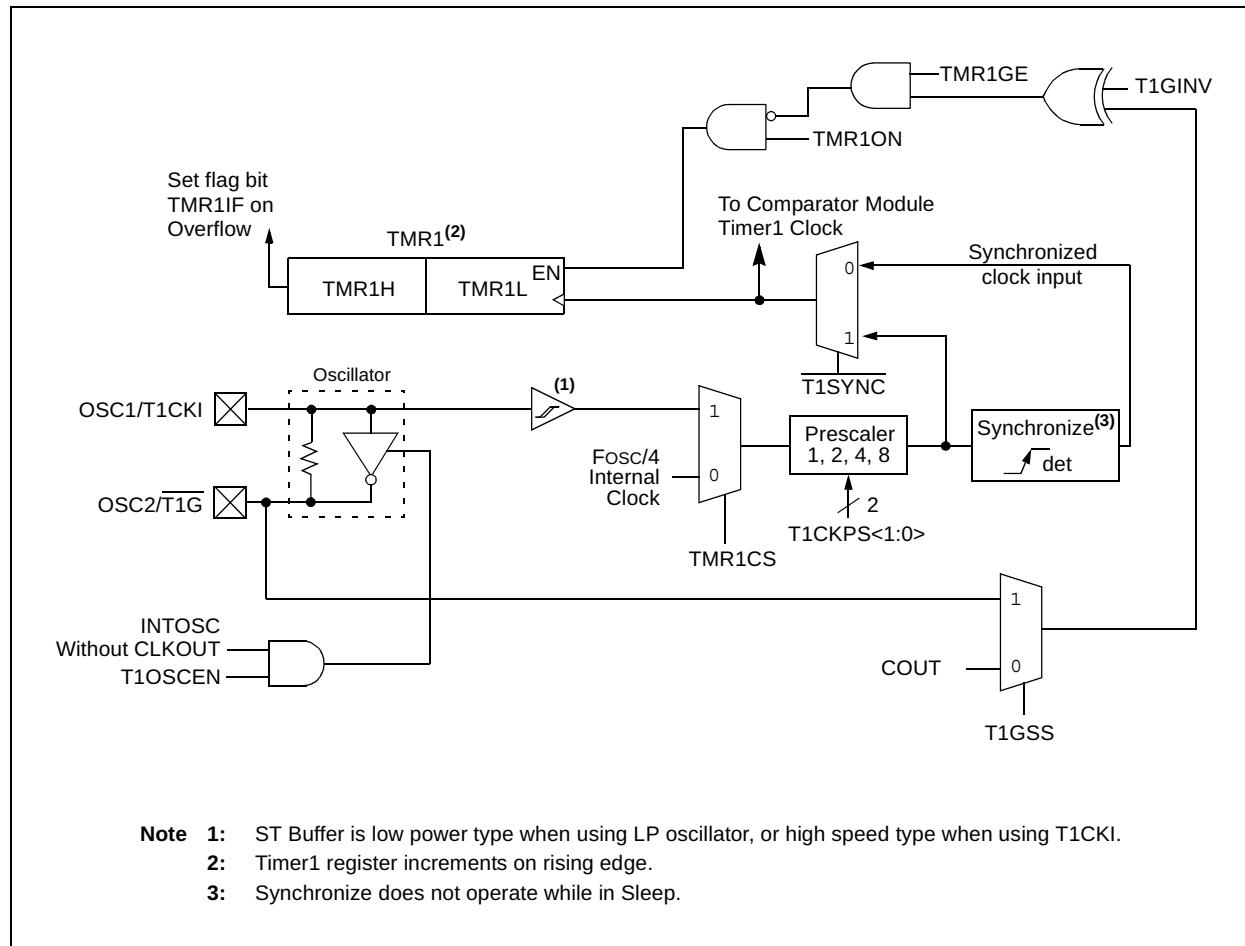
6.0 TIMER1 MODULE WITH GATE CONTROL

The Timer1 module is a 16-bit timer/counter with the following features:

- 16-bit timer/counter register pair (TMR1H:TMR1L)
- Programmable internal or external clock source
- 3-bit prescaler
- Optional LP oscillator
- Synchronous or asynchronous operation
- Timer1 gate (count enable) via comparator or T1G pin
- Interrupt on overflow
- Wake-up on overflow (external clock, Asynchronous mode only)
- Special Event Trigger (with CCP)
- Comparator output synchronization to Timer1 clock

Figure 6-1 is a block diagram of the Timer1 module.

FIGURE 6-1: TIMER1 BLOCK DIAGRAM



6.1 Timer1 Operation

The Timer1 module is a 16-bit incrementing counter which is accessed through the TMR1H:TMR1L register pair. Writes to TMR1H or TMR1L directly update the counter.

When used with an internal clock source, the module is a timer. When used with an external clock source, the module can be used as either a timer or counter.

6.2 Clock Source Selection

The TMR1CS bit of the T1CON register is used to select the clock source. When TMR1CS = 0, the clock source is Fosc/4. When TMR1CS = 1, the clock source is supplied externally.

Clock Source	TMR1CS
Fosc/4	0
T1CKI pin	1

6.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

6.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

6.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (amplifier output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when in LP oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISIO<5:4> bits are set when the Timer1 oscillator is enabled. GP5 and GP4 bits read as '0' and TRISIO5 and TRISIO4 bits read as '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce a single spurious increment.

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TTMR1L register pair.

6.6 Timer1 Gate

Timer1 gate source is software configurable to be the T1G pin or the output of the Comparator. This allows the device to directly time external events using T1G or analog events using Comparator 2. See the CMCON1 register (**Register 8-2**) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note: TMR1GE bit of the T1CON register must be set to use either T1G or COUT as the Timer1 gate source. See **Register 8-2** for more information on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the T1G pin or Comparator 2 output. This configures Timer1 to measure either the active-high or active-low time between events.

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt enable bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

6.9 CCP Special Event Trigger

If a CCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the Fosc to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the CCP, the write will take precedence.

For more information, see **Section on CCP**.

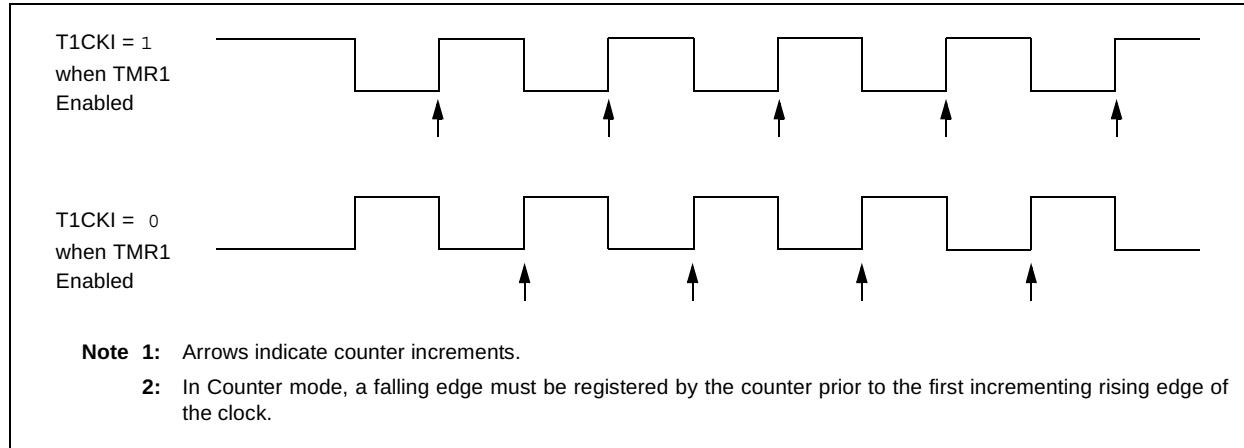
6.10 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see **Section 8.0 “Comparator Module”**.

FIGURE 6-2: TIMER1 INCREMENTING EDGE



6.11 Timer1 Control Register

The Timer1 Control register (T1CON), shown in Register 6-1, is used to control Timer1 and select the various features of the Timer1 module.

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1GINV ⁽¹⁾	TMR1GE ⁽²⁾	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **T1GINV:** Timer1 Gate Invert bit⁽¹⁾
 1 = Timer1 gate is active-high (Timer1 counts when gate is high)
 0 = Timer1 gate is active-low (Timer1 counts when gate is low)
- bit 6 **TMR1GE:** Timer1 Gate Enable bit⁽²⁾
If TMR1ON = 0:
 This bit is ignored
If TMR1ON = 1:
 1 = Timer1 is on if Timer1 gate is not active
 0 = Timer1 is on
- bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
 11 = 1:8 Prescale Value
 10 = 1:4 Prescale Value
 01 = 1:2 Prescale Value
 00 = 1:1 Prescale Value
- bit 3 **T1OSCEN:** LP Oscillator Enable Control bit
If INTOSC without CLKOUT oscillator is active:
 1 = LP oscillator is enabled for Timer1 clock
 0 = LP oscillator is off
Else:
 This bit is ignored. LP oscillator is disabled.
- bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
 1 = Do not synchronize external clock input
 0 = Synchronize external clock input
TMR1CS = 0:
 This bit is ignored. Timer1 uses the internal clock
- bit 1 **TMR1CS:** Timer1 Clock Source Select bit
 1 = External clock from T1CKI pin (on the rising edge)
 0 = Internal clock (Fosc/4)
- bit 0 **TMR1ON:** Timer1 On bit
 1 = Enables Timer1
 0 = Stops Timer1

Note 1: T1GINV bit inverts the Timer1 gate logic, regardless of source.

2: TMR1GE bit must be set to use either T1G pin or COUT, as selected by the T1GSS bit of the CMCON1 register, as a Timer1 gate source.

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TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CONFIG ⁽¹⁾	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
CMCON1	—	—	—	—	—	T1GSS	CMSYNC	-----10	-----10	-----10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register							xxxxx xxxx	uuuuu uuuuu	uuuuu uuuuu
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register							xxxxx xxxx	uuuuu uuuuu	uuuuu uuuuu
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	uuuuu uuuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: See Configuration Word register (Register 12-1) for operation of all register bits.

7.0 TIMER2 MODULE

The Timer2 module is an 8-bit timer with the following features:

- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Interrupt on TMR2 match with PR2
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscale (1:1 to 1:16)

See Figure 7-1 for a block diagram of Timer2.

7.1 Timer2 Operation

The clock input to the Timer2 module is the system instruction clock ($F_{osc}/4$). The clock is fed into the Timer2 prescaler, which has prescale options of 1:1, 1:4 or 1:16. The output of the prescaler is then used to increment the TMR2 register.

The values of TMR2 and PR2 are constantly compared to determine when they match. TMR2 will increment from 00h until it matches the value in PR2. When a match occurs, two things happen:

- TMR2 is reset to 00h on the next increment cycle.
- The Timer2 postscaler is incremented

The match output of the Timer2/PR2 comparator is then fed into the Timer2 postscaler. The postscaler has postscale options of 1:1 to 1:16 inclusive. The output of the Timer2 postscaler is used to set the TMR2IF interrupt flag bit in the PIR1 register.

The TMR2 and PR2 registers are both fully readable and writable. On any Reset, the TMR2 register is set to 00h and the PR2 register is set to FFh.

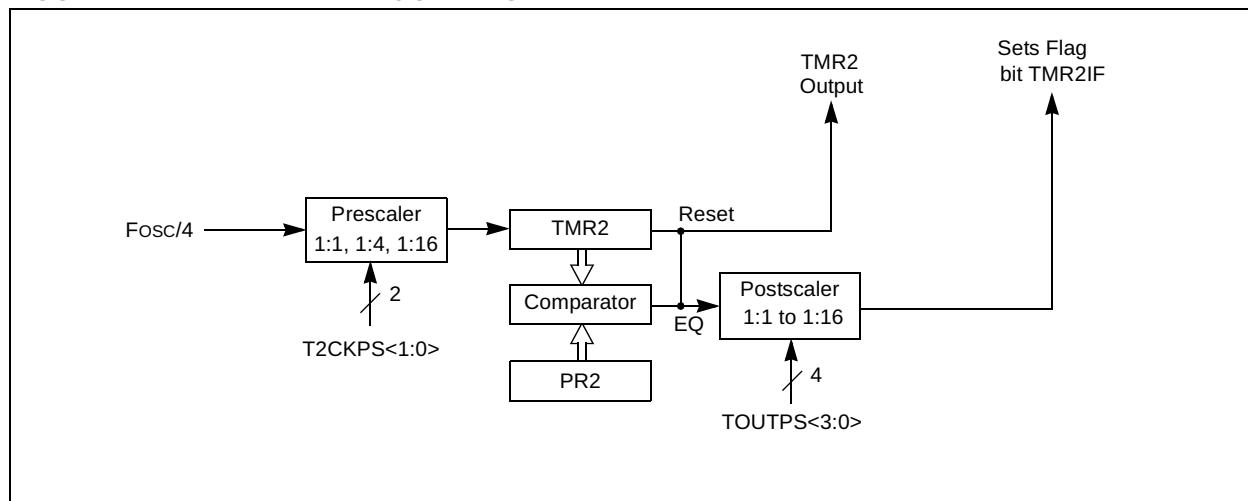
Timer2 is turned on by setting the TMR2ON bit in the T2CON register to a '1'. Timer2 is turned off by clearing the TMR2ON bit to a '0'.

The Timer2 prescaler is controlled by the T2CKPS bits in the T2CON register. The Timer2 postscaler is controlled by the TOUTPS bits in the T2CON register. The prescaler and postscaler counters are cleared when:

- A write to TMR2 occurs.
- A write to T2CON occurs.
- Any device Reset occurs (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset).

Note: TMR2 is not cleared when T2CON is written.

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



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REGISTER 7-1: T2CON: TIMER 2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscaler Select bits

0000 = 1:1 Postscaler

0001 = 1:2 Postscaler

0010 = 1:3 Postscaler

0011 = 1:4 Postscaler

0100 = 1:5 Postscaler

0101 = 1:6 Postscaler

0110 = 1:7 Postscaler

0111 = 1:8 Postscaler

1000 = 1:9 Postscaler

1001 = 1:10 Postscaler

1010 = 1:11 Postscaler

1011 = 1:12 Postscaler

1100 = 1:13 Postscaler

1101 = 1:14 Postscaler

1110 = 1:15 Postscaler

1111 = 1:16 Postscaler

bit 2 **TMR2ON:** Timer2 On bit

1 = Timer2 is on

0 = Timer2 is off

bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits

00 = Prescaler is 1

01 = Prescaler is 4

1x = Prescaler is 16

TABLE 7-1: SUMMARY OF ASSOCIATED TIMER2 REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PR2	Timer2 Module Period Register							1111 1111	1111 1111	
TMR2	Holding Register for the 8-bit TMR2 Register							0000 0000	0000 0000	
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for Timer2 module.

8.0 COMPARATOR MODULE

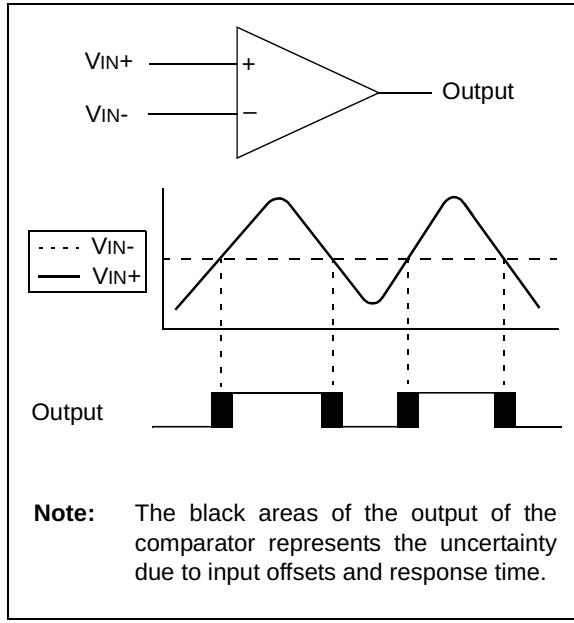
Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. The comparators are very useful mixed signal building blocks because they provide analog functionality independent of the program execution. The analog comparator module includes the following features:

- Multiple comparator configurations
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Timer1 gate (count enable)
- Output synchronization to Timer1 clock input
- Programmable voltage reference

8.1 Comparator Overview

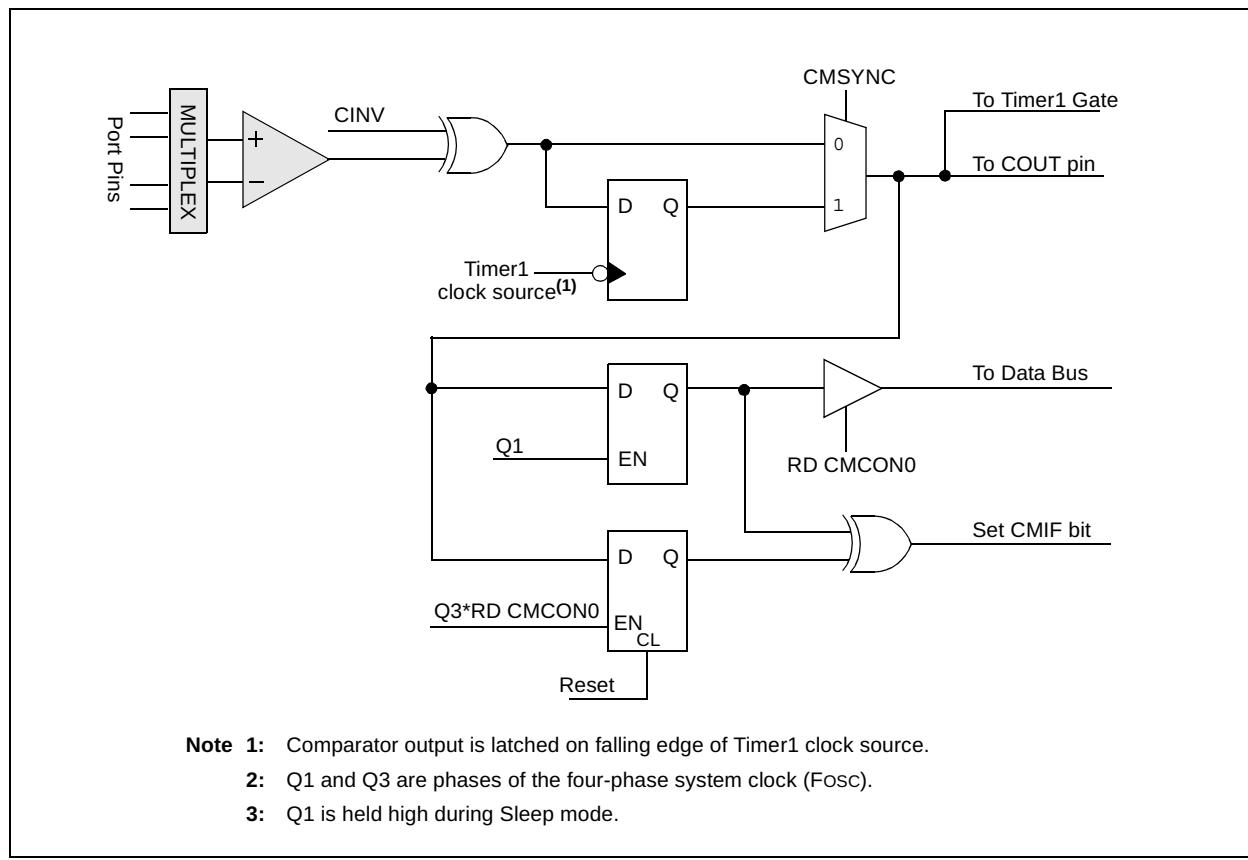
The comparator is shown in Figure 8-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at V_{IN+} is less than the analog voltage at V_{IN-} , the output of the comparator is a digital low level. When the analog voltage at V_{IN+} is greater than the analog voltage at V_{IN-} , the output of the comparator is a digital high level.

FIGURE 8-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

FIGURE 8-2: COMPARATOR OUTPUT BLOCK DIAGRAM



Note 1: Comparator output is latched on falling edge of Timer1 clock source.

2: Q1 and Q3 are phases of the four-phase system clock (Fosc).

3: Q1 is held high during Sleep mode.

8.2 Analog Input Connection Considerations

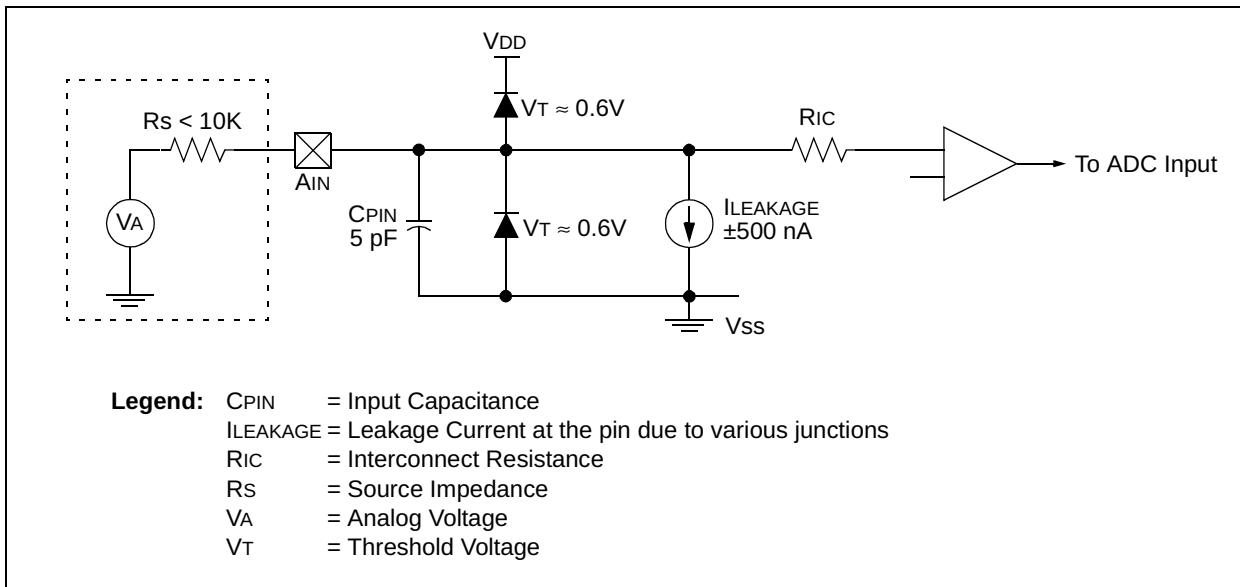
A simplified circuit for an analog input is shown in Figure 8-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10\text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 8-3: ANALOG INPUT MODEL



8.3 Comparator Configuration

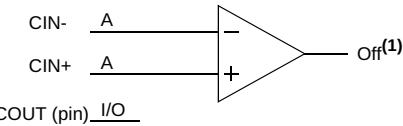
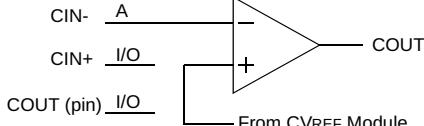
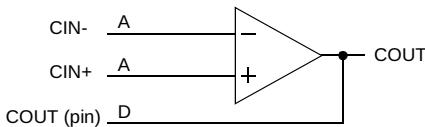
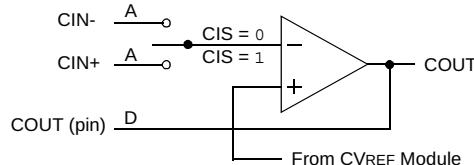
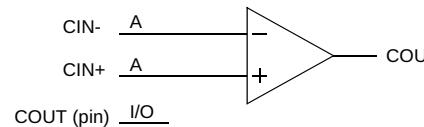
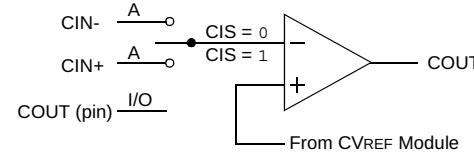
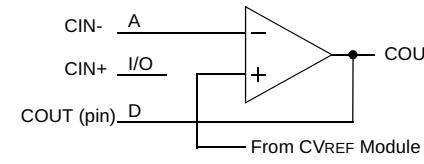
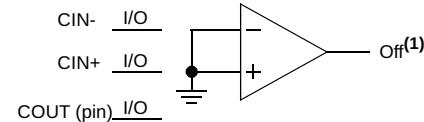
There are eight modes of operation for the comparator. The CM<2:0> bits of the CMCON0 register are used to select these modes as shown in Figure 8-4.

- Analog function (A): digital input buffer is disabled
- Digital function (D): comparator digital output, overrides port function
- Normal port function (I/O): independent of comparator

The port pins denoted as "A" will read as a '0' regardless of the state of the I/O pin or the I/O control TRIS bit. Pins used as analog inputs should also have the corresponding TRIS bit set to '1' to disable the digital output driver. Pins denoted as "D" should have the corresponding TRIS bit set to '0' to enable the digital output driver.

Note: Comparator interrupts should be disabled during a Comparator mode change to prevent unintended interrupts.

FIGURE 8-4: COMPARATOR I/O OPERATING MODES

<p>Comparator Reset (POR Default Value – low power) CM<2:0> = 000</p> 	<p>Comparator w/o Output and with Internal Reference CM<2:0> = 100</p> 
<p>Comparator with Output CM<2:0> = 001</p> 	<p>Multiplexed Input with Internal Reference and Output CM<2:0> = 101</p> 
<p>Comparator without Output CM<2:0> = 010</p> 	<p>Multiplexed Input with Internal Reference CM<2:0> = 110</p> 
<p>Comparator with Output and Internal Reference CM<2:0> = 011</p> 	<p>Comparator Off (Lowest power) CM<2:0> = 111</p> 
<p>Legend: A = Analog Input, ports always reads '0' I/O = Normal port I/O</p> <p>Note 1: Reads as '0', unless CINV = 1.</p>	<p>CIS = Comparator Input Switch (CMCON0<3>) D = Comparator Digital Output</p>

8.4 Comparator Control

The CMCON0 register (Register 8-1) provides access to the following comparator features:

- Mode selection
- Output state
- Output polarity
- Input switch

8.4.1 COMPARATOR OUTPUT STATE

The Comparator state can always be read internally via the COUT bit of the CMCON0 register. The comparator state may also be directed to the COUT pin in the following modes:

- CM<2:0> = 001
- CM<2:0> = 011
- CM<2:0> = 101

When one of the above modes is selected, the associated TRIS bit of the COUT pin must be cleared.

8.4.2 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CINV bit of the CMCON0 register. Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 8-1.

TABLE 8-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	COUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

Note: COUT refers to both the register bit and output pin.

8.4.3 COMPARATOR INPUT SWITCH

The inverting input of the comparator may be switched between two analog pins in the following modes:

- CM<2:0> = 101
- CM<2:0> = 110

In the above modes, both pins remain in analog mode regardless of which pin is selected as the input. The CIS bit of the CMCON0 register controls the comparator input switch.

8.5 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 15.0 “Electrical Specifications”** for more details.

8.6 Comparator Interrupt Operation

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Changes are recognized by means of a mismatch circuit which consists of two latches and an exclusive-or gate (see Figure 8.2). One latch is updated with the comparator output level when the CMCON0 register is read. This latch retains the value until the next read of the CMCON0 register or the occurrence of a Reset. The other latch of the mismatch circuit is updated on every Q1 system clock. A mismatch condition will occur when a comparator output change is clocked through the second latch on the Q1 clock cycle. The mismatch condition will persist, holding the CMIF bit of the PIR1 register true, until either the CMCON0 register is read or the comparator output returns to the previous state.

Note: A write operation to the CMCON0 register will also clear the mismatch condition because all writes include a read operation at the beginning of the write cycle.

Software will need to maintain information about the status of the comparator output to determine the actual change that has occurred.

The CMIF bit of the PIR1 register, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit of the PIE1 register and the PEIE and GIE bits of the INTCON register must all be set to enable comparator interrupts. If any of these bits are cleared, the interrupt is not enabled, although the CMIF bit of the PIR1 register will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of CMCON0. This will end the mismatch condition.
- Clear the CMIF interrupt flag.

A persistent mismatch condition will preclude clearing the CMIF interrupt flag. Reading CMCON0 will end the mismatch condition and allow the CMIF bit to be cleared.

Note: If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF interrupt flag may not get set.

FIGURE 8-5: COMPARATOR INTERRUPT TIMING W/O CMCON0 READ

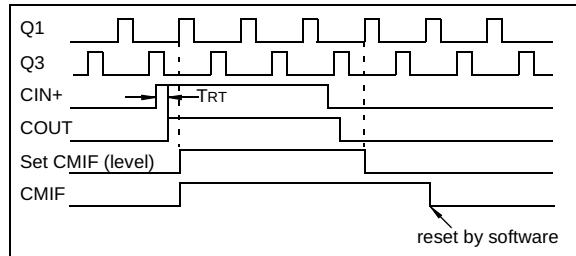
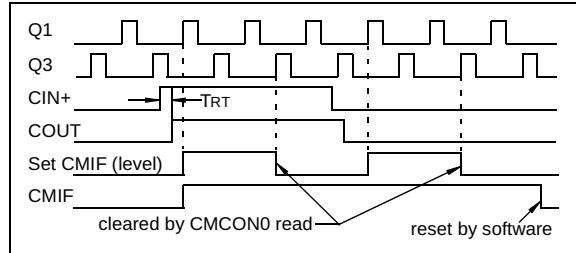


FIGURE 8-6: COMPARATOR INTERRUPT TIMING WITH CMCON0 READ



Note 1: If a change in the CMCON0 register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF of the PIR1 register interrupt flag may not get set.

- When either comparator is first enabled, bias circuitry in the Comparator module may cause an invalid output from the comparator until the bias circuitry is stable. Allow about 1 μ s for bias settling then clear the mismatch condition and interrupt flags before enabling comparator interrupts.

8.7 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in **Section 15.0 “Electrical Specifications”**. If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. The comparator is turned off by selecting mode CM<2:0> = 000 or CM<2:0> = 111 of the CMCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CMIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the Interrupt Service Routine.

REGISTER 8-1: CMCON0: COMPARATOR CONFIGURATION REGISTER

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0
bit 7							
bit 0							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

-n = Value at POR

‘1’ = Bit is set

‘0’ = Bit is cleared

x = Bit is unknown

bit 7	Unimplemented: Read as ‘0’
bit 6	COUT: Comparator Output bit <u>When CINV = 0:</u> 1 = VIN+ > VIN- 0 = VIN+ < VIN- <u>When CINV = 1:</u> 1 = VIN+ < VIN- 0 = VIN+ > VIN-
bit 5	Unimplemented: Read as ‘0’
bit 4	CINV: Comparator Output Inversion bit 1 = Output inverted 0 = Output not inverted
bit 3	CIS: Comparator Input Switch bit <u>When CM<2:0> = 110 or 101:</u> 1 = CIN+ connects to VIN- 0 = CIN- connects to VIN- <u>When CM<2:0> = 0xx or 100 or 111:</u> CIS has no effect.
bit 2-0	CM<2:0>: Comparator Mode bits (See Figure 8-5) 000 = CIN pins are configured as analog, COUT pin configured as I/O, Comparator output turned off 001 = CIN pins are configured as analog, COUT pin configured as Comparator output 010 = CIN pins are configured as analog, COUT pin configured as I/O, Comparator output available internally 011 = CIN- pin is configured as analog, CIN+ pin is configured as I/O, COUT pin configured as Comparator output, CVREF is non-inverting input 100 = CIN- pin is configured as analog, CIN+ pin is configured as I/O, COUT pin is configured as I/O, Comparator output available internally, CVREF is non-inverting input 101 = CIN pins are configured as analog and multiplexed, COUT pin is configured as Comparator output, CVREF is non-inverting input 110 = CIN pins are configured as analog and multiplexed, COUT pin is configured as I/O, Comparator output available internally, CVREF is non-inverting input 111 = CIN pins are configured as I/O, COUT pin is configured as I/O, Comparator output disabled, Comparator off.

8.9 Comparator Gating Timer1

This feature can be used to time the duration or interval of analog events. Clearing the T1GSS bit of the CMCON1 register will enable Timer1 to increment based on the output of the comparator. This requires that Timer1 is on and gating is enabled. See **Section 6.0 “Timer1 Module with Gate Control”** for details.

It is recommended to synchronize the comparator with Timer1 by setting the CMSYNC bit when the comparator is used as the Timer1 gate source. This ensures Timer1 does not miss an increment if the comparator changes during an increment.

8.10 Synchronizing Comparator Output to Timer1

The comparator output can be synchronized with Timer1 by setting the CMSYNC bit of the CMCON1 register. When enabled, the comparator output is latched on the falling edge of the Timer1 clock source. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 8-2) and the Timer1 Block Diagram (Figure 6-1) for more information.

REGISTER 8-2: CMCON1: COMPARATOR CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-1	R/W-0
—	—	—	—	—	—	T1GSS	CMSYNC
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **T1GSS:** Timer1 Gate Source Select bit⁽¹⁾

1 = Timer 1 Gate Source is $\overline{T1G}$ pin (pin should be configured as digital input)
0 = Timer 1 Gate Source is comparator output

bit 0 **CMSYNC:** Comparator Output Synchronization bit⁽²⁾

1 = Output is synchronized with falling edge of Timer1 clock
0 = Output is asynchronous

Note 1: Refer to **Section 6.6 “Timer1 Gate”**.

2: Refer to Figure 8-2.

8.11 Comparator Voltage Reference

The Comparator Voltage Reference module provides an internally generated voltage reference for the comparators. The following features are available:

- Independent from Comparator operation
- Two 16-level voltage ranges
- Output clamped to V_{SS}
- Ratiometric with V_{DD}

The VRCON register (Register 8-3) controls the Voltage Reference module shown in Figure 8-7.

8.11.1 INDEPENDENT OPERATION

The comparator voltage reference is independent of the comparator configuration. Setting the VREN bit of the VRCON register will enable the voltage reference.

8.11.2 OUTPUT VOLTAGE SELECTION

The CVREF voltage reference has 2 ranges with 16 voltage levels in each range. Range selection is controlled by the VRR bit of the VRCON register. The 16 levels are set with the VR<3:0> bits of the VRCON register.

The CVREF output voltage is determined by the following equations:

EQUATION 8-1: CVREF OUTPUT VOLTAGE

$$V_{RR} = 1 \text{ (low range)}$$

$$CVREF = (VR<3:0>/24) \times V_{DD}$$

$$V_{RR} = 0 \text{ (high range)}$$

$$CVREF = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

The full range of V_{SS} to V_{DD} cannot be realized due to the construction of the module. See Figure 8-1.

8.11.3 OUTPUT CLAMPED TO V_{SS}

The CVREF output voltage can be set to V_{SS} with no power consumption by configuring VRCON as follows:

- VREN = 0
- VRR = 1
- VR<3:0> = 0000

This allows the comparator to detect a zero-crossing while not consuming additional CVREF module current.

8.11.4 OUTPUT RATIO METRIC TO V_{DD}

The comparator voltage reference is V_{DD} derived and therefore, the CVREF output changes with fluctuations in V_{DD}. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 15.0 "Electrical Specifications"**.

REGISTER 8-3: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	—	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

VREN: CVREF Enable bit

1 = CVREF circuit powered on

0 = CVREF circuit powered down, no IDD drain and CVREF = V_{SS}.

bit 6

Unimplemented: Read as '0'

bit 5

VRR: CVREF Range Selection bit

1 = Low range

0 = High range

bit 4

Unimplemented: Read as '0'

bit 3-0

VR<3:0>: CVREF Value Selection $0 \leq VR<3:0> \leq 15$

When VRR = 1: $CVREF = (VR<3:0>/24) * V_{DD}$

When VRR = 0: $CVREF = V_{DD}/4 + (VR<3:0>/32) * V_{DD}$

FIGURE 8-7: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

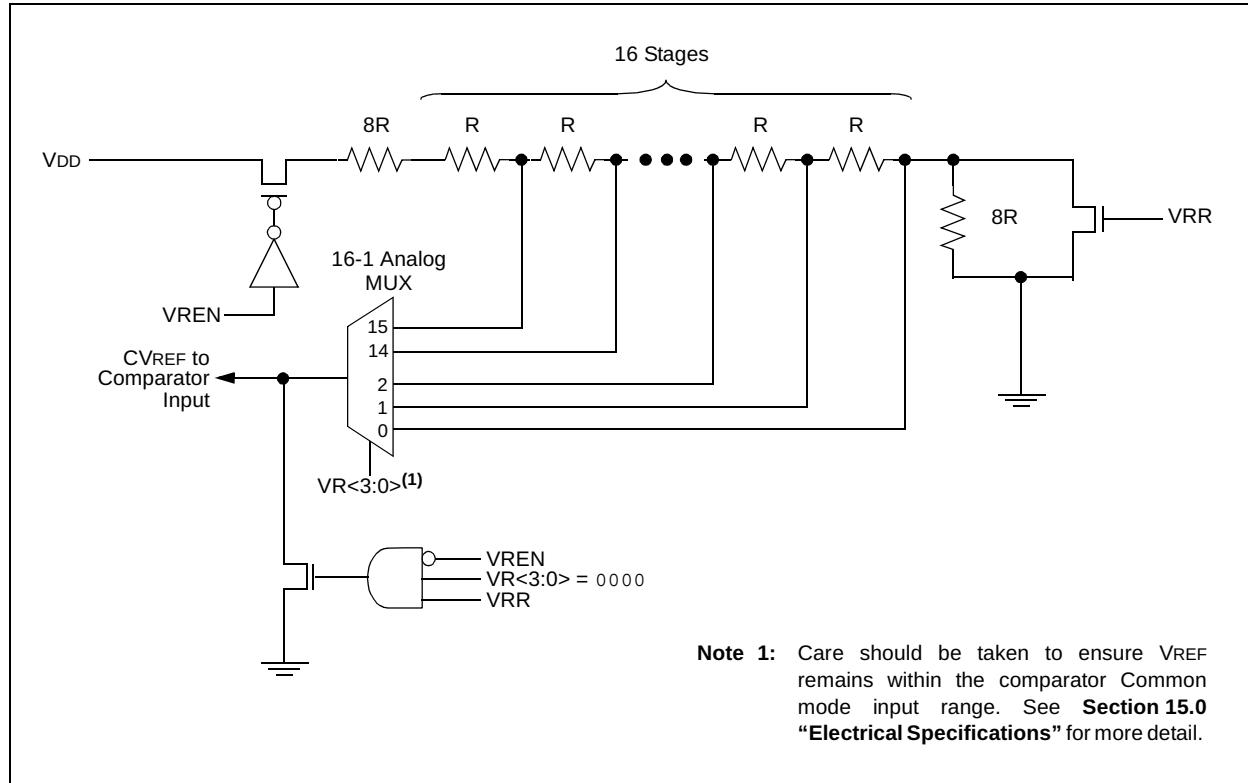


TABLE 8-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE COMPARATOR AND VOLTAGE REFERENCE MODULES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
CMCON0	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	TOIE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
VRCN	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	-0-0 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for comparator.

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NOTES:

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

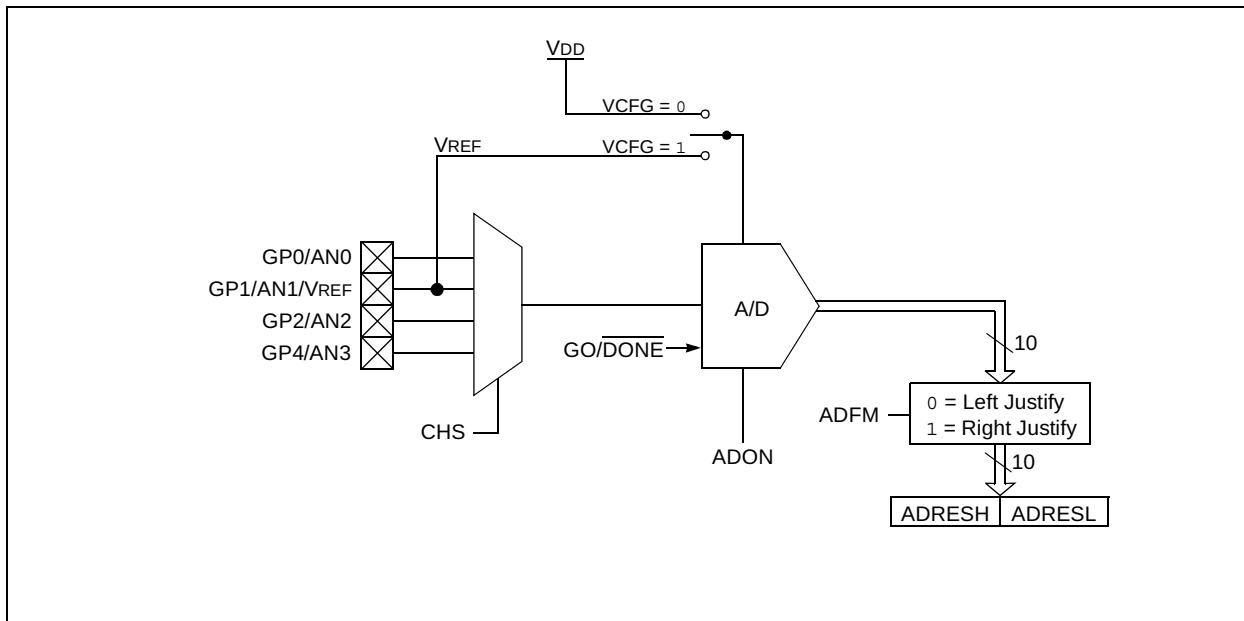
The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

FIGURE 9-1: ADC BLOCK DIAGRAM



9.1 ADC Configuration

When configuring and using the ADC the following functions must be considered:

- GPIO configuration
- Channel selection
- ADC voltage reference selection
- ADC conversion clock source
- Interrupt control
- Results formatting

9.1.1 GPIO CONFIGURATION

The ADC can be used to convert both analog and digital signals. When converting analog signals, the I/O pin should be configured for analog by setting the associated TRIS and ANSEL bits. See the corresponding GPIO section for more information.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

9.1.2 CHANNEL SELECTION

The CHS bits of the ADCON0 register determine which channel is connected to the sample and hold circuit.

When changing channels, a delay is required before starting the next conversion. Refer to **Section 9.2 “ADC Operation”** for more information.

9.1.3 ADC VOLTAGE REFERENCE

The VCFG bit of the ADCON0 register provides control of the positive voltage reference. The positive voltage reference can be either Vdd or an external voltage source. The negative voltage reference is always connected to the ground reference.

9.1.4 CONVERSION CLOCK

The source of the conversion clock is software selectable via the ADCS bits of the ANSEL register. There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal oscillator)

The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods as shown in Figure 9-2.

For correct conversion, the appropriate TAD specification must be met. See A/D conversion requirements in **Section 15.0 “Electrical Specifications”** for more information. Table 9-1 gives examples of appropriate ADC clock selections.

Note: Unless using the FRC, any changes in the system clock frequency will change the ADC clock frequency, which may adversely affect the ADC result.

TABLE 9-1: ADC CLOCK PERIOD (TAD) Vs. DEVICE OPERATING FREQUENCIES (VDD \geq 3.0V)

ADC Clock Period (TAD)		Device Frequency (Fosc)			
ADC Clock Source	ADCS<2:0>	20 MHz	8 MHz	4 MHz	1 MHz
Fosc/2	000	100 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μ s
Fosc/4	100	200 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μ s ⁽²⁾	4.0 μ s
Fosc/8	001	400 ns ⁽²⁾	1.0 μ s ⁽²⁾	2.0 μ s	8.0 μ s ⁽³⁾
Fosc/16	101	800 ns ⁽²⁾	2.0 μ s	4.0 μ s	16.0 μ s ⁽³⁾
Fosc/32	010	1.6 μ s	4.0 μ s	8.0 μ s ⁽³⁾	32.0 μ s ⁽³⁾
Fosc/64	110	3.2 μ s	8.0 μ s ⁽³⁾	16.0 μ s ⁽³⁾	64.0 μ s ⁽³⁾
FRC	x11	2-6 μ s ^(1,4)			

Legend: Shaded cells are outside of recommended range.

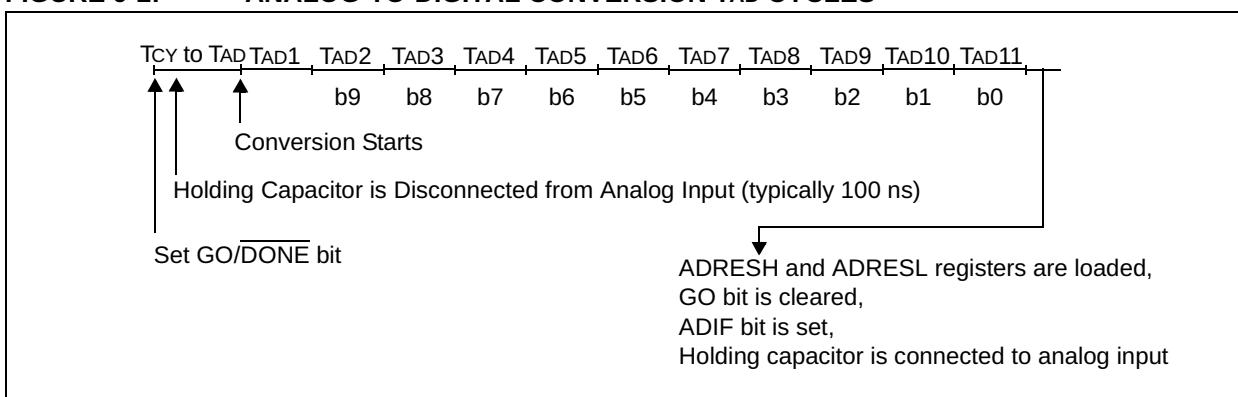
Note 1: The FRC source has a typical TAD time of 4 μ s for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the FRC clock source is only recommended if the conversion will be performed during Sleep.

FIGURE 9-2: ANALOG-TO-DIGITAL CONVERSION TAD CYCLES



9.1.5 INTERRUPTS

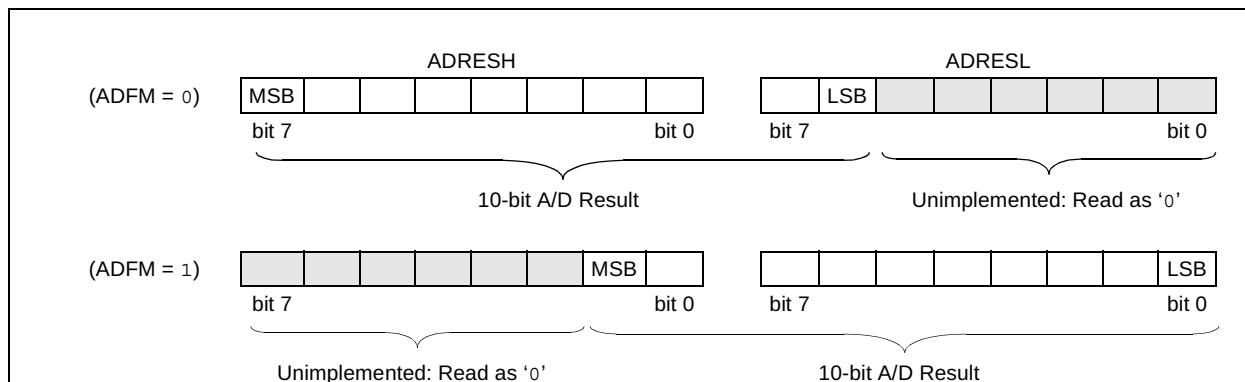
The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC interrupt flag is the ADIF bit in the PIR1 register. The ADC interrupt enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note: The ADIF bit is set at the completion of every conversion, regardless of whether or not the ADC interrupt is enabled.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the global interrupt must be disabled. If the global interrupt is enabled, execution will switch to the interrupt service routine.

Please see **Section 12.4 “Interrupts”** for more information.

FIGURE 9-3: 10-BIT A/D CONVERSION RESULT FORMAT



9.2 ADC Operation

9.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note: The GO/DONE bit should not be set in the same instruction that turns on the ADC. Refer to **Section 9.2.6 “A/D Conversion Procedure”**.

9.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF flag bit
- Update the ADRESH:ADRESL registers with new conversion result

9.1.6 RESULT FORMATTING

The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON0 register controls the output format.

Figure 9-3 shows the two output formats.

9.2.3 TERMINATING A CONVERSION

If a conversion must be terminated before completion, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete Analog-to-Digital conversion sample. Instead, the ADRESH:ADRESL register pair will retain the value of the previous conversion. Additionally, a 2 TAD delay is required before another acquisition can be initiated. Following this delay, an input acquisition is automatically started on the selected channel.

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

PIC12F683

9.2.4 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the FRC option. When the FRC clock source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than FRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

9.2.5 SPECIAL EVENT TRIGGER

The CCP Special Event Trigger allows periodic ADC measurements without software intervention. When this trigger occurs, the GO/DONE bit is set by hardware and the Timer1 counter resets to zero.

Using the Special Event Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See **Section 11.0 "Capture/Compare/PWM (CCP) Module"** for more information.

9.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure GPIO Port:
 - Disable pin output driver (See TRIS register)
 - Configure pin as analog
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Select result format
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result

8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: See **Section 9.3 "A/D Acquisition Requirements"**.

EXAMPLE 9-1: A/D CONVERSION

```
;This code block configures the ADC  
;for polling, Vdd reference, Frc clock  
;and GPO input.  
;  
;Conversion start & polling for completion  
; are included.  
;  
BANKSEL TRISIO      ;  
BSF    TRISIO,0      ;Set GPO to input  
BANKSEL ANSEL       ;  
MOVLW  B'01110001'  ;ADC Frc clock,  
IORWF  ANSEL       ; and GPO as analog  
BANKSEL ADCON0      ;  
MOVLW  B'10000001'  ;Right justify,  
MOVWF  ADCON0      ;Vdd Vref, AN0, On  
CALL   SampleTime   ;Acquisition delay  
BSF    ADCON0,GO    ;Start conversion  
BTFSC  ADCON0,GO    ;Is conversion done?  
GOTO   $-1          ;No, test again  
BANKSEL ADRESH      ;  
MOVF   ADRESH,W     ;Read upper 2 bits  
MOVWF  RESULTHI    ;Store in GPR space  
BANKSEL ADRESL      ;  
MOVF   ADRESL,W     ;Read lower 8 bits  
MOVWF  RESULTLO    ;Store in GPR space
```

9.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 9-1: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON
bit 7	bit 0						

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 7 **ADFM:** A/D Conversion Result Format Select bit
1 = Right justified
0 = Left justified
- bit 6 **VCFG:** Voltage Reference bit
1 = VREF pin
0 = VDD
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3-2 **CHS<1:0>: Analog Channel Select bits**
00 = AN0
01 = AN1
10 = AN2
11 = AN3
- bit 1 **GO/DONE:** A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress
- bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

PIC12F683

REGISTER 9-2: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

| R/W-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES9 | ADRES8 | ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper 8 bits of 10-bit conversion result

REGISTER 9-3: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
ADRES1	ADRES0	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower 2 bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

REGISTER 9-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

| R/W-x |
|-------|-------|-------|-------|-------|-------|-------|--------|
| — | — | — | — | — | — | — | ADRES9 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-2 **Reserved**: Do not use.

bit 1-0 **ADRES<9:8>**: ADC Result Register bits
Upper 2 bits of 10-bit conversion result

REGISTER 9-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

| R/W-x |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits
Lower 8 bits of 10-bit conversion result

9.3 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-4. The source impedance (R_s) and the internal sampling switch (R_{ss}) impedance directly affect the time required to charge the capacitor C_{HOLD} . The sampling switch (R_{ss}) impedance varies over the device voltage (V_{DD}), see Figure 9-4. **The maximum recommended impedance for analog sources is 10 k Ω .** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed),

an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the ADC). The 1/2 LSB error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 9-1: ACQUISITION TIME EXAMPLE

Assumptions: Temperature = 50°C and external impedance of 10k Ω 5.0V VDD

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25^\circ C)(0.05\mu s/\text{ }^\circ C)] \end{aligned}$$

The value for T_C can be approximated with the following equations:

$$V_{APPLIED} \left(1 - \frac{1}{2047}\right) = V_{CHOLD} \quad ;[1] \text{ } V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}}\right) = V_{CHOLD} \quad ;[2] \text{ } V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED} \left(1 - e^{-\frac{T_C}{RC}}\right) = V_{APPLIED} \left(1 - \frac{1}{2047}\right) \quad ;\text{combining [1] and [2]}$$

Solving for T_C :

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_s) \ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega) \ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.37\mu s + [(50^\circ C - 25^\circ C)(0.05\mu s/\text{ }^\circ C)] \\ &= 4.67\mu s \end{aligned}$$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

- 2:** The charge holding capacitor (C_{HOLD}) is not discharged after each conversion.
- 3:** The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

PIC12F683

FIGURE 9-4: ANALOG INPUT MODEL

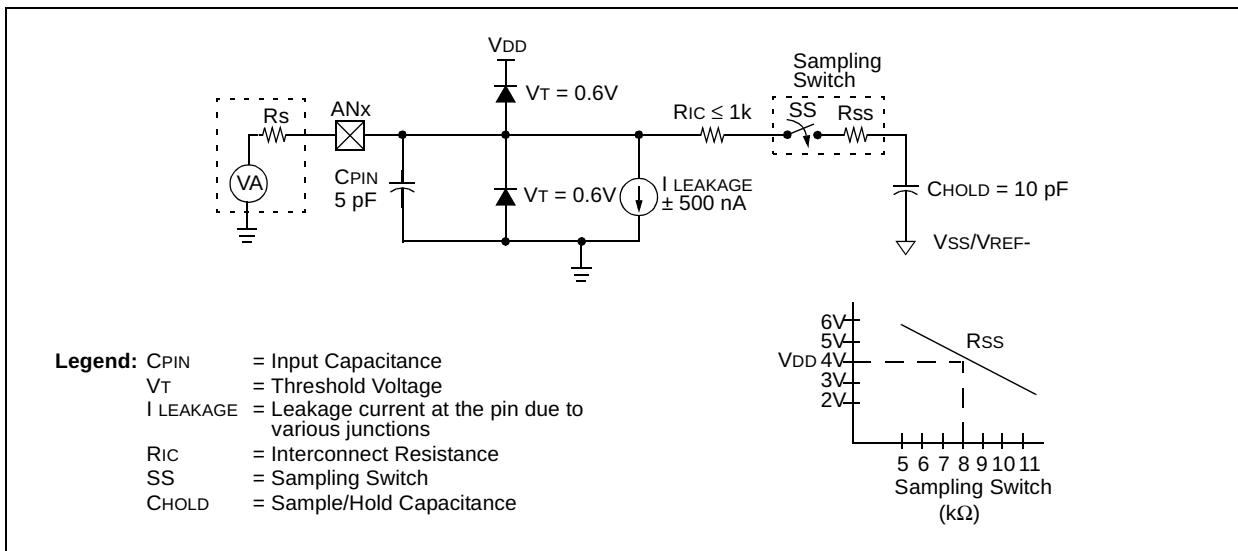


FIGURE 9-5: ADC TRANSFER FUNCTION

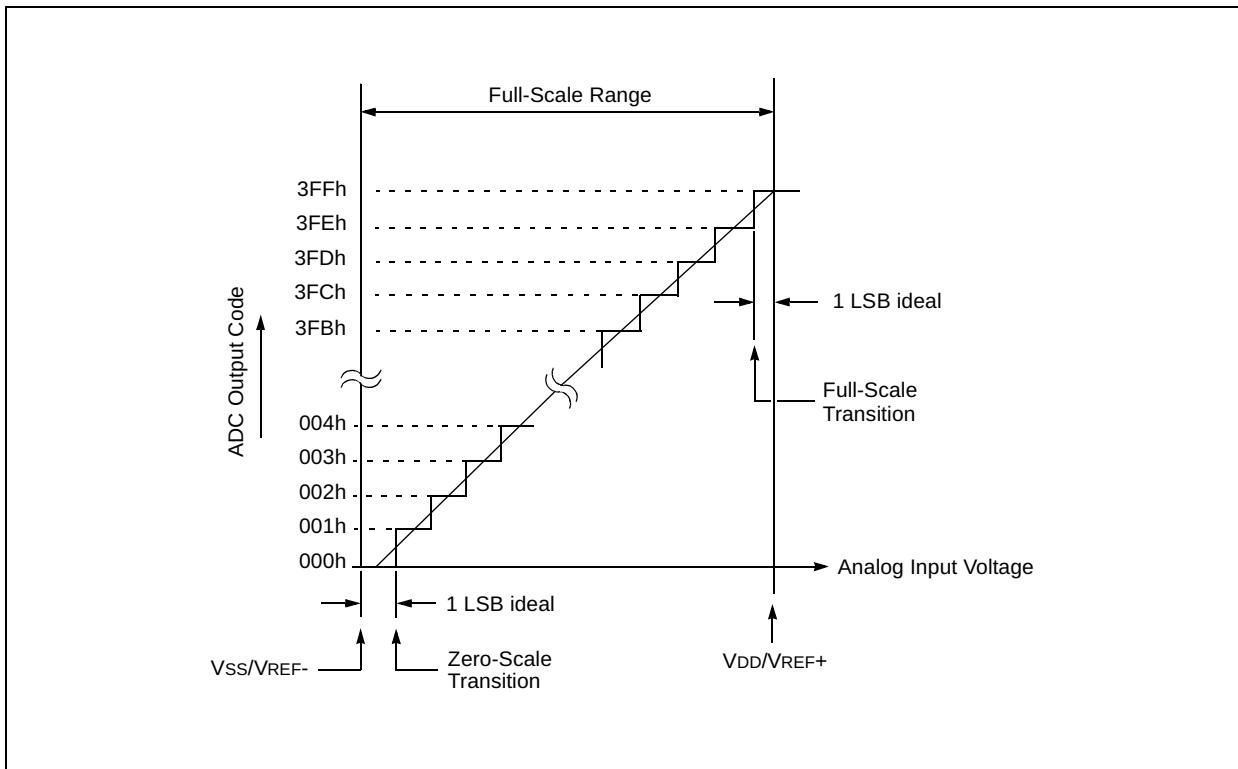


TABLE 9-2: SUMMARY OF ASSOCIATED ADC REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
ADCON0	ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON	00-- 0000	0000 0000
ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, – = unimplemented read as '0'. Shaded cells are not used for ADC module.

PIC12F683

NOTES:

10.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDAT
- EEADR

EEDAT holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F683 has 256 bytes of data EEPROM with an address range from 0h to FFh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip-to-chip. Please refer to AC Specifications in **Section 15.0 “Electrical Specifications”** for exact limits.

When the data memory is code-protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access the data EEPROM data and will read zeroes.

REGISTER 10-1: EEDAT: EEPROM DATA REGISTER

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| EEDAT7 | EEDAT6 | EEDAT5 | EEDAT4 | EEDAT3 | EEDAT2 | EEDAT1 | EEDAT0 |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 7-0

EEDATn: Byte Value to Write To or Read From Data EEPROM bits

REGISTER 10-2: EEADR: EEPROM ADDRESS REGISTER

| R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| EEADR7 | EEADR6 | EEADR5 | EEADR4 | EEADR3 | EEADR2 | EEADR1 | EEADR0 |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 7-0

EEADR: Specifies One of 256 Locations for EEPROM Read/Write Operation bits

10.1 EECON1 and EECON2 Registers

EECON1 is the control register with four low-order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal

operation. In these situations, following Reset, the user can check the WRERR bit, clear it and rewrite the location. The data and address will be cleared. Therefore, the EEDAT and EEADR registers will need to be re-initialized.

Interrupt flag, EEIF bit of the PIR1 register, is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence.

Note: The EECON1, EEDAT and EEADR registers should not be modified during a data EEPROM write (WR bit = 1).

REGISTER 10-3: EECON1: EEPROM CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7	bit 0						

Legend:

S = Bit can only be set

R = Readable bit

-n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

x = Bit is unknown

- bit 7-4 **Unimplemented:** Read as '0'
- bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any MCLR Reset, any WDT Reset during normal operation or BOR Reset)
0 = The write operation completed
- bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM
- bit 1 **WR:** Write Control bit
1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.)
0 = Write cycle to the data EEPROM is complete
- bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.)
0 = Does not initiate an EEPROM read

10.2 Reading the EEPROM Data Memory

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD of the EECON1 register, as shown in Example 10-1. The data is available, at the very next cycle, in the EEDAT register. Therefore, it can be read in the next instruction. EEDAT holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 10-1: DATA EEPROM READ

```
BANKSEL    EEADR      ;  
MOVlw     CONFIG_ADDR;  
MOVWF    EEADR      ;Address to read  
BSF      EECON1, RD  ;EE Read  
MOVF     EEDAT, W   ;Move data to W
```

10.3 Writing to the EEPROM Data Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDAT register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 10-2.

EXAMPLE 10-2: DATA EEPROM WRITE

```
BANKSEL    EECON1      ;  
BSF      EECON1, WREN ;Enable write  
BCF      INTCON, GIE  ;Disable INTS  
BTFSCL    INTCON, GIE ;See AN576  
GOTO    $-2          ;  
MOVLW    55h          ;Unlock write  
MOVWF    EECON2      ;  
MOVLW    AAh          ;  
MOVWF    EECON2      ;  
BSF      EECON1, WR   ;Start the write  
BSF      INTCON, GIE  ;Enable INTS
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit of the PIR1 register must be cleared by software.

10.4 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 10-3) to the desired value to be written.

EXAMPLE 10-3: WRITE VERIFY

```
BANKSELEEDAT      ;  
MOVF    EEDAT, W   ;EEDAT not changed  
           ;from previous write  
BSF     EECON1, RD ;YES, Read the  
           ;value written  
XORWF    EEDAT, W  
BTFSCL    STATUS, Z ;Is data the same  
GOTO    WRITE_ERR  ;No, handle error  
           ;Yes, continue
```

10.4.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). When variables in one section change frequently, while variables in another section do not change, it is possible to exceed the total number of write cycles to the EEPROM (specification D124) without exceeding the total number of write cycles to a single byte (specifications D120 and D120A). If this is the case, then a refresh of the array must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

10.5 Protection Against Spurious Write

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (64 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- Brown-out
- Power Glitch
- Software Malfunction

10.6 Data EEPROM Operation During Code-Protect

Data memory can be code-protected by programming the CPD bit in the Configuration Word register (Register 12-1) to '0'.

When the data memory is code-protected, the CPU is able to read and write data to the data EEPROM. It is recommended to code-protect the program memory when code-protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations in program memory to '0' will also help prevent data memory code protection from becoming breached.

TABLE 10-1: SUMMARY OF ASSOCIATED DATA EEPROM REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	0000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
EEDAT	EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	0000 0000	0000 0000
EEADR	EEADR7	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADRO	0000 0000	0000 0000
EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
EECON2 ⁽¹⁾	EEPROM Control Register 2							----	----	----

Legend: x = unknown, u = unchanged, — = unimplemented read as '0', q = value depends upon condition. Shaded cells are not used by the Data EEPROM module.

Note 1: EECON2 is not a physical register.

11.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM module is a peripheral which allows the user to time and control different events. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate a Pulse-Width Modulated signal of varying frequency and duty cycle.

The timer resources used by the module are shown in Table 11-1

Additional information on CCP modules is available in the Application Note AN594, "Using the CCP Modules" (DS00594).

TABLE 11-1: CCP MODE – TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 11-1: CCP1CON: CCP1 CONTROL REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6	Unimplemented: Read as '0'
bit 5-4	DC1B<1:0>: PWM Duty Cycle Least Significant bits
	<u>Capture mode:</u> Unused.
	<u>Compare mode:</u> Unused.
	<u>PWM mode:</u> These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.
bit 3-0	CCP1M<3:0>: CCP Mode Select bits
	0000 = Capture/Compare/PWM off (resets CCP module)
	0001 = Unused (reserved)
	0010 = Unused (reserved)
	0011 = Unused (reserved)
	0100 = Capture mode, every falling edge
	0101 = Capture mode, every rising edge
	0110 = Capture mode, every 4th rising edge
	0111 = Capture mode, every 16th rising edge
	1000 = Compare mode, set output on match (CCP1IF bit is set)
	1001 = Compare mode, clear output on match (CCP1IF bit is set)
	1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)
	1011 = Compare mode, trigger special event (CCP1IF bit is set, TMR1 is reset and A/D conversion is started if the ADC module is enabled. CCP1 pin is unaffected.)
	110x = PWM mode active-high
	111x = PWM mode active-low

11.1 Capture Mode

In Capture mode, CCP1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin CCP1. An event is defined as one of the following and is configured by the CCP1M<3:0> bits of the CCP1CON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

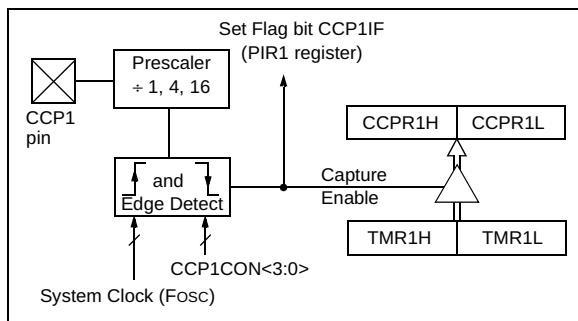
When a capture is made, the Interrupt Request Flag bit CCP1IF of the PIR1 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPR1H, CCPR1L register pair is read, the old captured value is overwritten by the new captured value (see Figure 11-1).

11.1.1 CCP1 PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the associated TRIS control bit.

Note: If the CCP1 pin is configured as an output, a write to the GPIO port can cause a capture condition.

FIGURE 11-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



11.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

11.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCP1IE interrupt enable bit of the PIE1 register clear to avoid false interrupts. Additionally, the user should clear the CCP1IF interrupt flag bit of the PIR1 register following any change in operating mode.

11.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCP1M<3:0> bits of the CCP1CON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCP1CON register before changing the prescaler (see Example 11-1).

EXAMPLE 11-1: CHANGING BETWEEN CAPTURE PRESCALERS

```

BANKSEL CCP1CON      ; Set Bank bits to point
                      ; to CCP1CON
CLRF   CCP1CON       ; Turn CCP module off
MOVLW  NEW_CAPT_PS  ; Load the W reg with
                      ; the new prescaler
                      ; move value and CCP ON
MOVWF CCP1CON        ; Load CCP1CON with this
                      ; value

```

11.2 Compare Mode

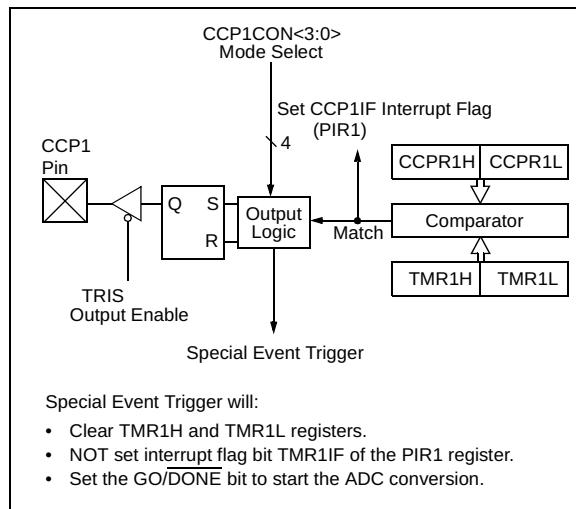
In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 module may:

- Toggle the CCP1 output.
- Set the CCP1 output.
- Clear the CCP1 output.
- Generate a Special Event Trigger.
- Generate a Software Interrupt.

The action on the pin is based on the value of the CCP1M<3:0> control bits of the CCP1CON register.

All Compare modes can generate an interrupt.

FIGURE 11-2: COMPARE MODE OPERATION BLOCK DIAGRAM



11.2.1 CCP1 PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the associated TRIS bit.

Note: Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the GPIO I/O data latch.

11.2.2 TIMER1 MODE SELECTION

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

11.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (CCP1M<3:0> = 1010), the CCP1 module does not assert control of the CCP1 pin (see the CCP1CON register).

11.2.4 SPECIAL EVENT TRIGGER

When Special Event Trigger mode is chosen (CCP1M<3:0> = 1011), the CCP1 module does the following:

- Resets Timer1
- Starts an ADC conversion if ADC is enabled

The CCP1 module does not assert control of the CCP1 pin in this mode (see the CCP1CON register).

The Special Event Trigger output of the CCP occurs immediately upon a match between the TMR1H, TMR1L register pair and the CCPR1H, CCPR1L register pair. The TMR1H, TMR1L register pair is not reset until the next rising edge of the Timer1 clock. This allows the CCPR1H, CCPR1L register pair to effectively provide a 16-bit programmable period register for Timer1.

Note 1: The Special Event Trigger from the CCP module does not set interrupt flag bit TMRxIF of the PIR1 register.

2: Removing the match condition by changing the contents of the CCPR1H and CCPR1L register pair, between the clock edge that generates the Special Event Trigger and the clock edge that generates the Timer1 Reset, will preclude the Reset from occurring.

11.3 PWM Mode

The PWM mode generates a Pulse-Width Modulated signal on the CCP1 pin. The duty cycle, period and resolution are determined by the following registers:

- PR2
- T2CON
- CCPR1L
- CCP1CON

In Pulse-Width Modulation (PWM) mode, the CCP module produces up to a 10-bit resolution PWM output on the CCP1 pin. Since the CCP1 pin is multiplexed with the PORT data latch, the TRIS for that pin must be cleared to enable the CCP1 pin output driver.

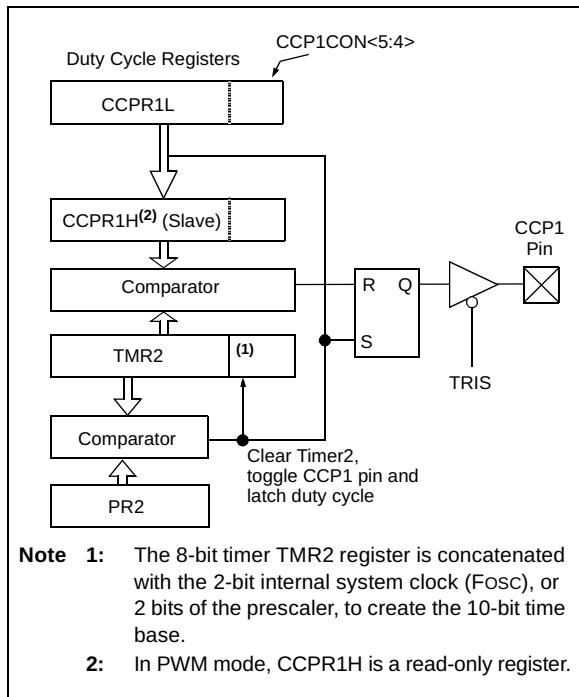
Note: Clearing the CCP1CON register will relinquish CCP1 control of the CCP1 pin.

Figure 11-1 shows a simplified block diagram of PWM operation.

Figure 11-4 shows a typical waveform of the PWM signal.

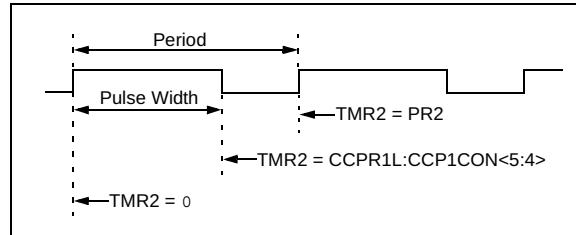
For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 11.3.7 “Setup for PWM Operation”**.

FIGURE 11-3: SIMPLIFIED PWM BLOCK DIAGRAM



The PWM output (Figure 11-4) has a time base (period) and a time that the output stays high (duty cycle).

FIGURE 11-4: CCP PWM OUTPUT



11.3.1 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 11-1.

EQUATION 11-1: PWM PERIOD

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{osc} \cdot (TMR2 \text{ Prescale Value})$$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPR1L into CCPR1H.

Note: The Timer2 postscaler (see [Section 7.0 “Timer2 Module”](#)) is not used in the determination of the PWM frequency.

11.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPR1L register and DC1B<1:0> bits of the CCP1CON register. The CCPR1L contains the eight MSbs and the CCP1<1:0> bits of the CCP1CON register contain the two LSbs. CCPR1L and DC1B<1:0> bits of the CCP1CON register can be written to at any time. The duty cycle value is not latched into CCPR1H until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPR1H register is read-only.

Equation 11-2 is used to calculate the PWM pulse width.

Equation 11-3 is used to calculate the PWM duty cycle ratio.

EQUATION 11-2: PULSE WIDTH

$$\text{Pulse Width} = (CCPR1L:CCP1CON<5:4>) \cdot T_{osc} \cdot (TMR2 \text{ Prescale Value})$$

EQUATION 11-3: DUTY CYCLE RATIO

$$\text{Duty Cycle Ratio} = \frac{(CCPR1L:CCP1CON<5:4>)}{4(PR2 + 1)}$$

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (Fosc), or 2 bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPR1H and 2-bit latch, then the CCP1 pin is cleared (see Figure 11-1).

11.3.3 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is 10 bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 11-4.

EQUATION 11-4: PWM RESOLUTION

$$\text{Resolution} = \frac{\log[4(PR2 + 1)]}{\log(2)} \text{ bits}$$

Note: If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

TABLE 11-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 20 MHz)

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 11-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (Fosc = 8 MHz)

PWM Frequency	1.22 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

11.3.4 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the CCP1 pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

11.3.5 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 3.0 “Oscillator Module (With Fail-Safe Clock Monitor)”** for additional details.

11.3.6 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

11.3.7 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Disable the PWM pin (CCP1) output drivers by setting the associated TRIS bit.
2. Set the PWM period by loading the PR2 register.
3. Configure the CCP module for the PWM mode by loading the CCP1CON register with the appropriate values.
4. Set the PWM duty cycle by loading the CCPR1L register and DC1B bits of the CCP1CON register.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIR1 register.
 - Set the Timer2 prescale value by loading the T2CKPS bits of the T2CON register.
 - Enable Timer2 by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output after a new PWM cycle has started:
 - Wait until Timer2 overflows (TMR2IF bit of the PIR1 register is set).
 - Enable the CCP1 pin output driver by clearing the associated TRIS bit.

TABLE 11-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte (LSB)								xxxx xxxx	xxxx xxxx
CCPR1H	Capture/Compare/PWM Register 1 High Byte (MSB)								xxxx xxxx	xxxx xxxx
CMCON1	—	—	—	—	—	—	T1GSS	CMSYNC	---- --10	---- --10
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
T1CON	T1GINV	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0000 0000	0000 0000
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	xxxx xxxx
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the Capture and Compare.

TABLE 11-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
CCPR1L	Capture/Compare/PWM Register 1 Low Byte (LSB)								xxxx xxxx	xxxx xxxx
CCPR1H	Capture/Compare/PWM Register 1 High Byte (MSB)								xxxx xxxx	xxxx xxxx
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000x
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	-000 0000
PIR1	EEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	-000 0000
PR2	Timer2 Period Register								1111 1111	1111 1111
T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
TMR2	Timer2 Module Register								0000 0000	0000 0000
TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown. Shaded cells are not used by the PWM.

PIC12F683

NOTES:

12.0 SPECIAL FEATURES OF THE CPU

The PIC12F683 has a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving features and offer code protection.

These features are:

- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Oscillator Selection
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F683 has two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 64 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can use the Power-up Timer to provide at least a 64 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through:

- External Reset
- Watchdog Timer Wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 12-1).

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See “*PIC12F6XX/16F6XX Memory Programming Specification*” (DS41204) for more information.

12.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations as shown in Register 12-1. These bits are mapped in program memory location 2007h.

PIC12F683

REGISTER 12-1: CONFIG: CONFIGURATION WORD REGISTER

—	—	—	—	FCMEN	IESO	BOREN1	BORENO
bit 15				bit 8			

CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0
bit 7				bit 0			

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

P = Programmable'
'0' = Bit is cleared

U = Unimplemented bit, read as '0'
x = Bit is unknown

- bit 15-12 **Unimplemented:** Read as '1'
- bit 11 **FCMEN:** Fail-Safe Clock Monitor Enabled bit
1 = Fail-Safe Clock Monitor is enabled
0 = Fail-Safe Clock Monitor is disabled
- bit 10 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode is enabled
0 = Internal External Switchover mode is disabled
- bit 9-8 **BOREN<1:0>:** Brown-out Reset Selection bits⁽¹⁾
11 = BOR enabled
10 = BOR enabled during operation and disabled in Sleep
01 = BOR controlled by SBOREN bit of the PCON register
00 = BOR disabled
- bit 7 **CPD:** Data Code Protection bit⁽²⁾
1 = Data memory code protection is disabled
0 = Data memory code protection is enabled
- bit 6 **CP:** Code Protection bit⁽³⁾
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled
- bit 5 **MCLRE:** GP3/MCLR pin function select bit⁽⁴⁾
1 = GP3/MCLR pin function is MCLR
0 = GP3/MCLR pin function is digital input, MCLR internally tied to VDD
- bit 4 **PWRTE:** Power-up Timer Enable bit
1 = PWRT disabled
0 = PWRT enabled
- bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled and can be enabled by SWDTEN bit of the WDTCON register
- bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
110 = RCIO oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
100 = INTOSCO oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN
010 = HS oscillator: High-speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
000 = LP oscillator: Low-power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

- Note**
- 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
 - 2: The entire data EEPROM will be erased when the code protection is turned off.
 - 3: The entire program memory will be erased when the code protection is turned off.
 - 4: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

12.2 Calibration Bits

Brown-out Reset (BOR), Power-on Reset (POR) and 8 MHz internal oscillator (HFINTOSC) are factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2009h). The Calibration Word is not erased when using the specified bulk erase sequence in the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41244) and thus, does not require reprogramming.

12.3 Reset

The PIC12F683 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during Sleep
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

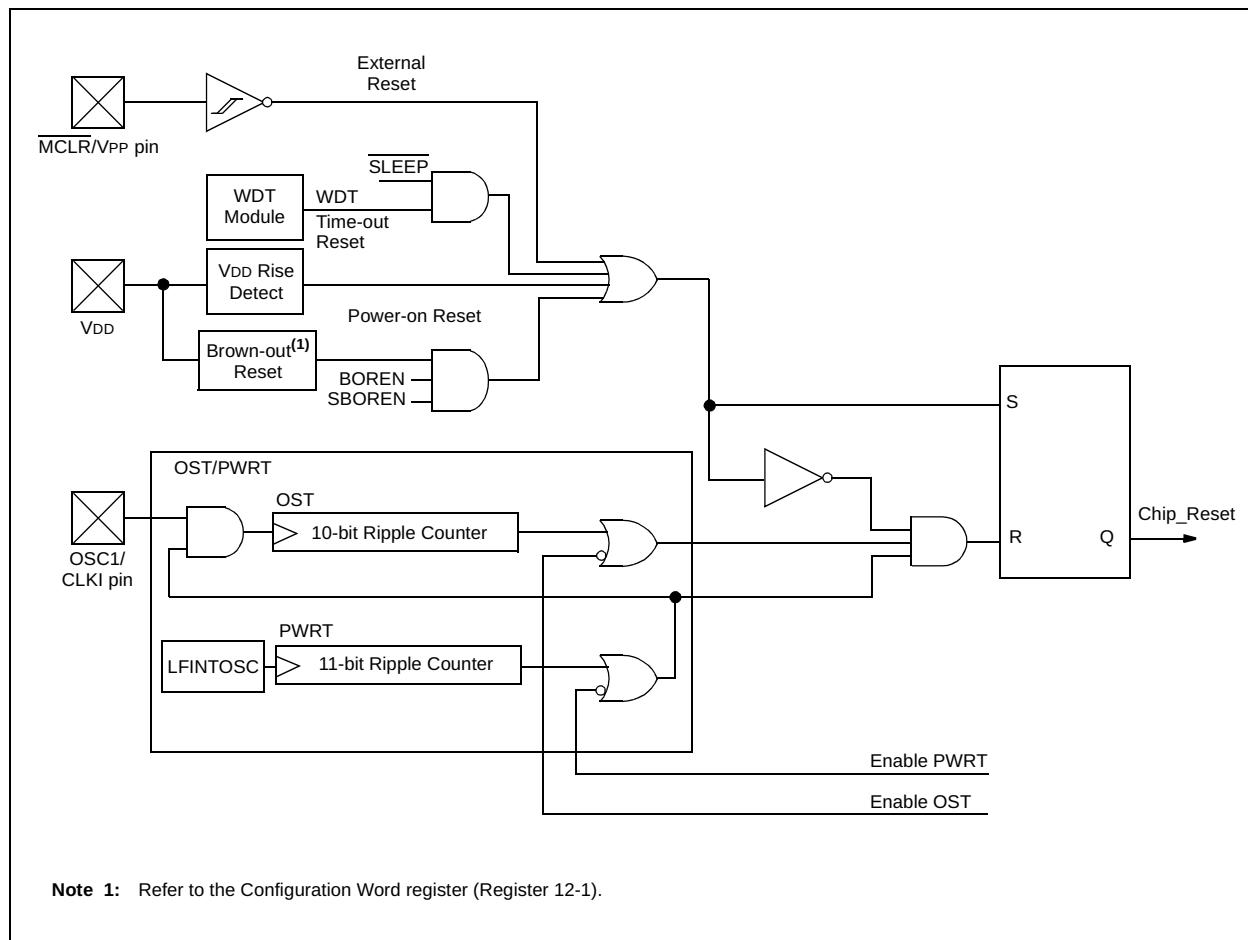
- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. TO and PD bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0 "Electrical Specifications"** for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



12.3.1 POWER-ON RESET

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply connect the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See **Section 15.0 “Electrical Specifications”** for details. If the BOR is enabled, the maximum rise time specification does not apply. The BOR circuitry will keep the device in Reset until VDD reaches VBOD (see **Section 12.3.4 “Brown-Out Reset (BOR)”**).

Note: The POR circuit does not produce an internal Reset when VDD declines. To re-enable the POR, VDD must reach Vss for a minimum of 100 μ s.

When the device starts normal operation (exits the Reset condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to the Application Note AN607, “Power-up Trouble Shooting” (DS00607).

12.3.2 MCLR

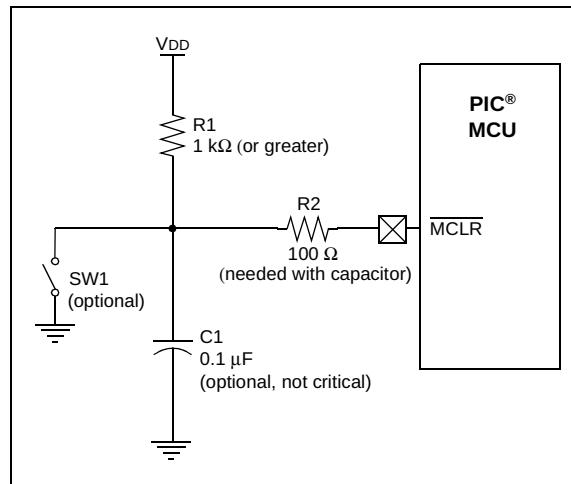
PIC12F683 has a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

Voltages applied to the MCLR pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 12-2, is suggested.

An internal MCLR option is enabled by clearing the MCLRE bit in the Configuration Word register. When MCLRE = 0, the Reset signal to the chip is generated internally. When the MCLRE = 1, the GP3/MCLR pin becomes an external Reset input. In this mode, the GP3/MCLR pin has a weak pull-up to VDD.

FIGURE 12-2: RECOMMENDED MCLR CIRCUIT



12.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 64 ms (nominal) time-out on power-up only, from POR or Brown-out Reset. The Power-up Timer operates from the 31 kHz LFINTOSC oscillator. For more information, see **Section 3.5 “Internal Clock Modes”**. The chip is kept in Reset as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A Configuration bit, PWRTE, can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should be enabled when Brown-out Reset is enabled, although it is not required.

The Power-up Timer delay will vary from chip-to-chip due to:

- VDD variation
- Temperature variation
- Process variation

See DC parameters for details (**Section 15.0 “Electrical Specifications”**).

Note: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a “low” level to the MCLR pin, rather than pulling this pin directly to Vss.

12.3.4 BROWN-OUT RESET (BOR)

The BOREN0 and BOREN1 bits in the Configuration Word register select one of four BOR modes. Two modes have been added to allow software or hardware control of the BOR enable. When $\text{BOREN}_{<1:0>} = 01$, the SBOREN bit of the PCON register enables/disables the BOR, allowing it to be controlled in software. By selecting $\text{BOREN}_{<1:0>} = 10$, the BOR is automatically disabled in Sleep to conserve power and enabled on wake-up. In this mode, the SBOREN bit is disabled. See Register 12-1 for the Configuration Word definition.

A brown-out occurs when VDD falls below VBOR for greater than parameter TBOR (see **Section 15.0 "Electrical Specifications"**). The brown-out condition will reset the device. This will occur regardless of VDD slew rate. A Brown-out Reset may not occur if VDD falls below VBOR for less than parameter TBOR.

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until VDD rises above VBOR (see Figure 12-3). If enabled, the Power-up Timer will be invoked by the Reset and keep the chip in Reset an additional 64 ms.

Note: The Power-up Timer is enabled by the PWRTE bit in the Configuration Word register.

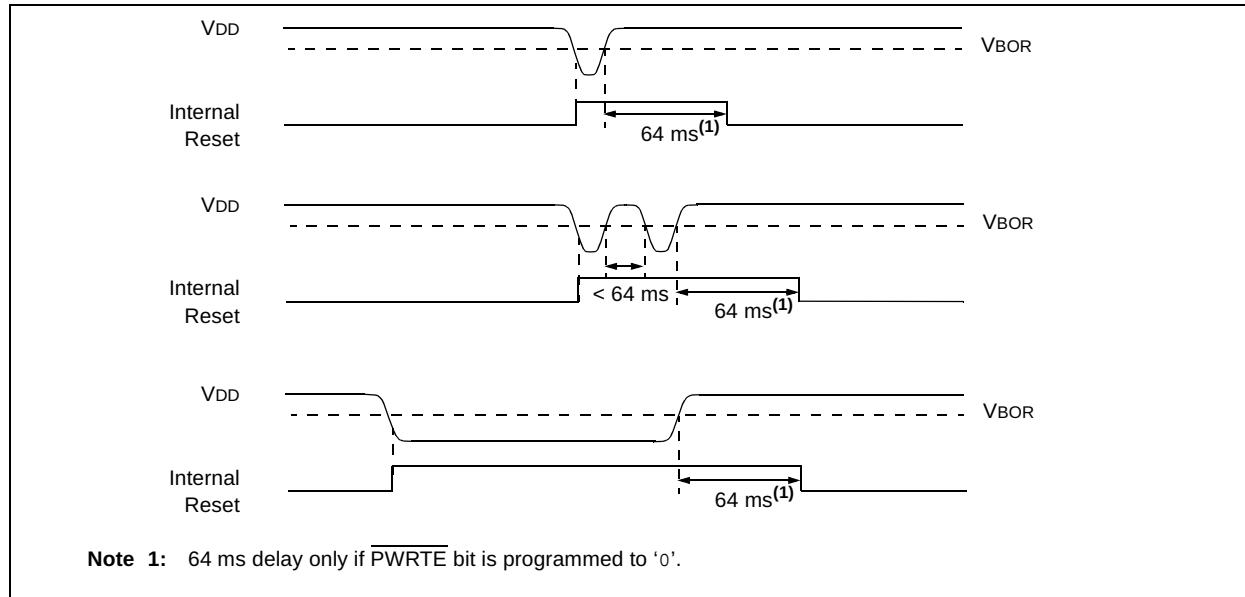
If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be re-initialized. Once VDD rises above VBOR, the Power-up Timer will execute a 64 ms Reset.

12.3.5 BOR CALIBRATION

The PIC12F683 stores the BOR calibration values in fuses located in the Calibration Word register (2008h). The Calibration Word register is not erased when using the specified bulk erase sequence in the "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) and thus, does not require reprogramming.

Note: Address 2008h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See "*PIC12F6XX/16F6XX Memory Programming Specification*" (DS41204) for more information.

FIGURE 12-3: BROWN-OUT SITUATIONS



PIC12F683

12.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences. The device can execute code from the INTOSC while OST is active by enabling Two-Speed Start-up or Fail-Safe Monitor (see **Section 3.7.2 “Two-Speed Start-up Sequence”** and **Section 3.8 “Fail-Safe Clock Monitor”**).

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then, bringing MCLR high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC12F683 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	
XT, HS, LP	TPWRT + 1024 • Tosc	1024 • Tosc	TPWRT + 1024 • Tosc	1024 • Tosc	1024 • Tosc
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	TO	PD	Condition
0	x	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	MCLR Reset during normal operation
u	u	1	0	MCLR Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR ⁽¹⁾	Value on all other Resets ⁽¹⁾
CONFIG ⁽²⁾	BOREN1	BORENO	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—
PCON			—	—	ULPWUE	SBOREN	—	—	POR	BOR	--01 --qq	--0u --uu
STATUS			IRP	RP1	RPO	TO	PD	Z	DC	C	0001 xxxx	000q quuu

Legend: u = unchanged, x = unknown, — = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

2: See Configuration Word register (Register 12-1) for operation of all register bits.

FIGURE 12-4: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR)

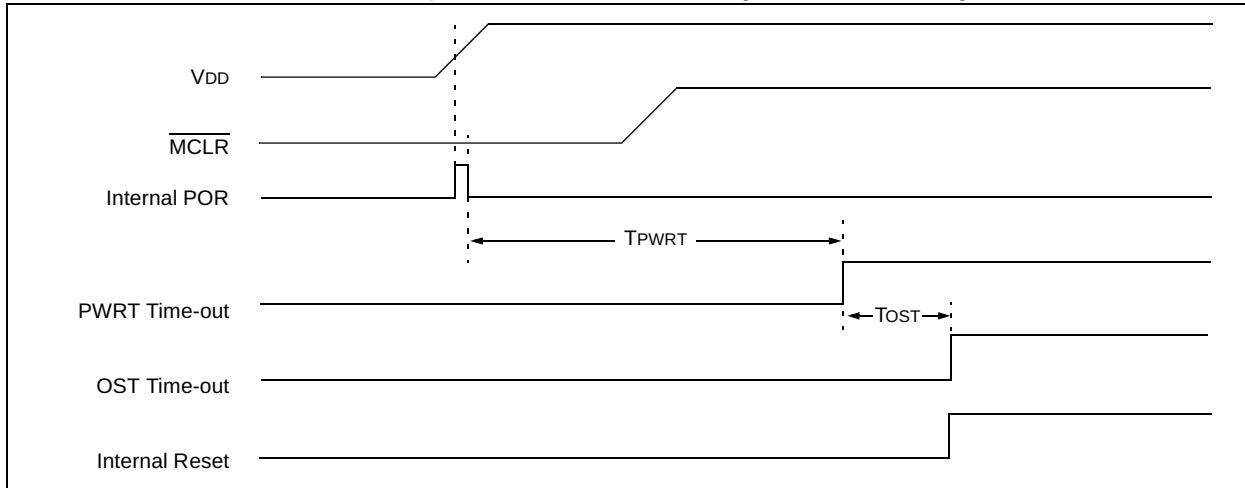


FIGURE 12-5: TIME-OUT SEQUENCE ON POWER-UP (DELAYED MCLR)

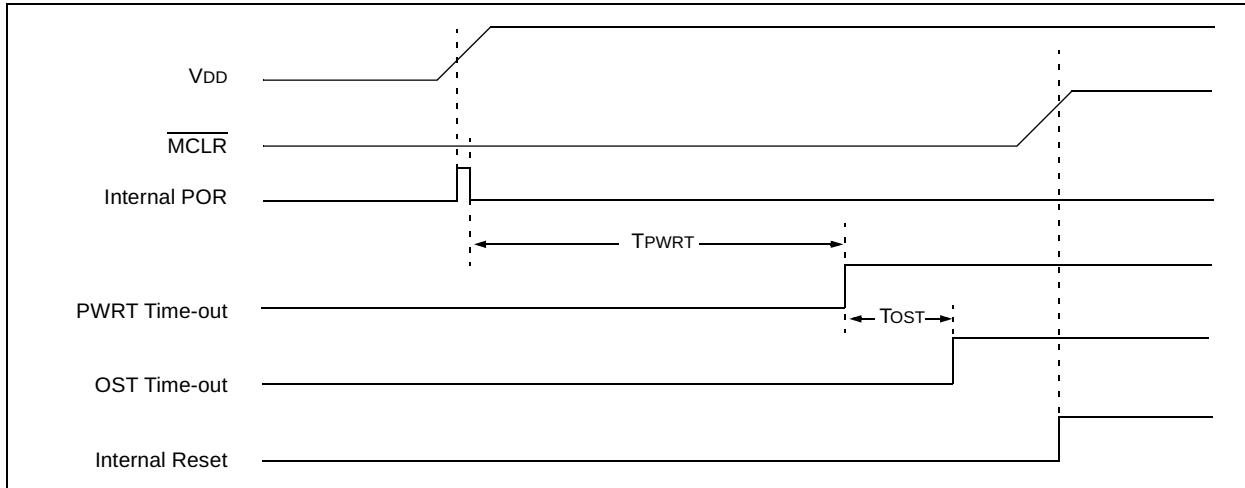
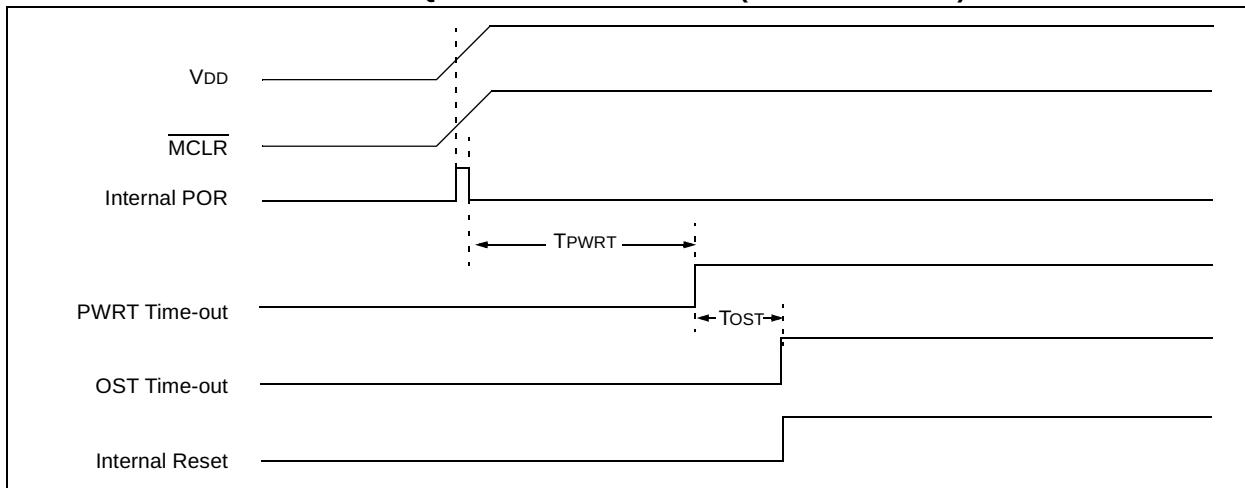


FIGURE 12-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR WITH VDD)



PIC12F683

TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--x0 x000	--x0 x000	--uu uuuu
PCLATH	0Ah/8Ah	---0 0000	---0 0000	---u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
PIR1	0Ch	0000 0000	0000 0000	uuuu uuuu ⁽²⁾
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	10h	0000 0000	uuuu uuuu	-uuu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2CON	12h	-000 0000	-000 0000	-uuu uuuu
CCPR1L	13h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	15h	--00 0000	--00 0000	--uu uuuu
WDTCON	18h	---0 1000	---0 1000	---u uuuu
CMCON0	19h	0000 0000	0000 0000	uuuu uuuu
CMCON1	20h	---- --10	---- --10	---- --uu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADC0N0	1Fh	00-- 0000	00-- 0000	uu-- uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	0000 0000	0000 0000	uuuu uuuu
PCON	8Eh	--01 --0x	--0u --uu ^(1,5)	--uu --uu
OSCCON	8Fh	-110 q000	-110 q000	-uuu uuuu
OSCTUNE	90h	---0 0000	---u uuuu	---u uuuu
PR2	92h	1111 1111	1111 1111	1111 1111
WPU	95h	--11 -111	--11 -111	uuuu uuuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
VRC0N	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDAT	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 12-4: INITIALIZATION CONDITION FOR REGISTERS (CONTINUED)

Register	Address	Power-on Reset	MCLR Reset WDT Reset Brown-out Reset ⁽¹⁾	Wake-up from Sleep through Interrupt Wake-up from Sleep through WDT Time-out
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	----	----	----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ANSEL	9Fh	-000 1111	-000 1111	-uuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).

3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

4: See Table 12-5 for Reset value for specific condition.

5: If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

TABLE 12-5: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	--01 --0x
MCLR Reset during Normal Operation	000h	000u uuuu	--0u --uu
MCLR Reset during Sleep	000h	0001 0uuu	--0u --uu
WDT Reset	000h	0000 uuuu	--0u --uu
WDT Wake-up	PC + 1	uuu0 0uuu	--uu --uu
Brown-out Reset	000h	0001 1uuu	--01 --10
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	--uu --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and Global Interrupt Enable bit, GIE, is set, the PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

12.4 Interrupts

The PIC12F683 has multiple interrupt sources:

- External Interrupt GP2/INT
- Timer0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- EEPROM Data Write Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt Request Register 1 (PIR1) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

The Global Interrupt Enable bit, GIE of the INTCON register, enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in the INTCON register and PIE1 register. GIE is cleared on Reset.

When an interrupt is serviced, the following actions occur automatically:

- The GIE is cleared to disable any further interrupt.
- The return address is pushed onto the stack.
- The PC is loaded with 0004h.

The Return from Interrupt instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT Pin Interrupt
- GPIO Change Interrupt
- Timer0 Overflow Interrupt

The peripheral interrupt flags are contained in the PIR1 register. The corresponding interrupt enable bit is contained in the PIE1 register.

The following interrupt flags are contained in the PIR1 register:

- EEPROM Data Write Interrupt
- A/D Interrupt
- Comparator Interrupt
- Timer1 Overflow Interrupt
- Timer2 Match Interrupt
- Fail-Safe Clock Monitor Interrupt
- CCP Interrupt

For external interrupt events, such as the INT pin or GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 12-8). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts, which were ignored, are still pending to be serviced when the GIE bit is set again.

For additional information on Timer1, Timer2, comparators, ADC, data EEPROM or Enhanced CCP modules, refer to the respective peripheral section.

12.4.1 GP2/INT INTERRUPT

The external interrupt on the GP2/INT pin is edge-triggered; either on the rising edge if the INTEDG bit of the OPTION register is set, or the falling edge, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit of the INTCON register is set. This interrupt can be disabled by clearing the INTE control bit of the INTCON register. The INTF bit must be cleared by software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from Sleep, if the INTE bit was set prior to going into Sleep. See **Section 12.7 “Power-Down Mode (Sleep)**” for details on Sleep and Figure 12-10 for timing of wake-up from Sleep through GP2/INT interrupt.

Note: The ANSEL and CMCON0 registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read ‘0’ and cannot generate an interrupt.

12.4.2 TIMER0 INTERRUPT

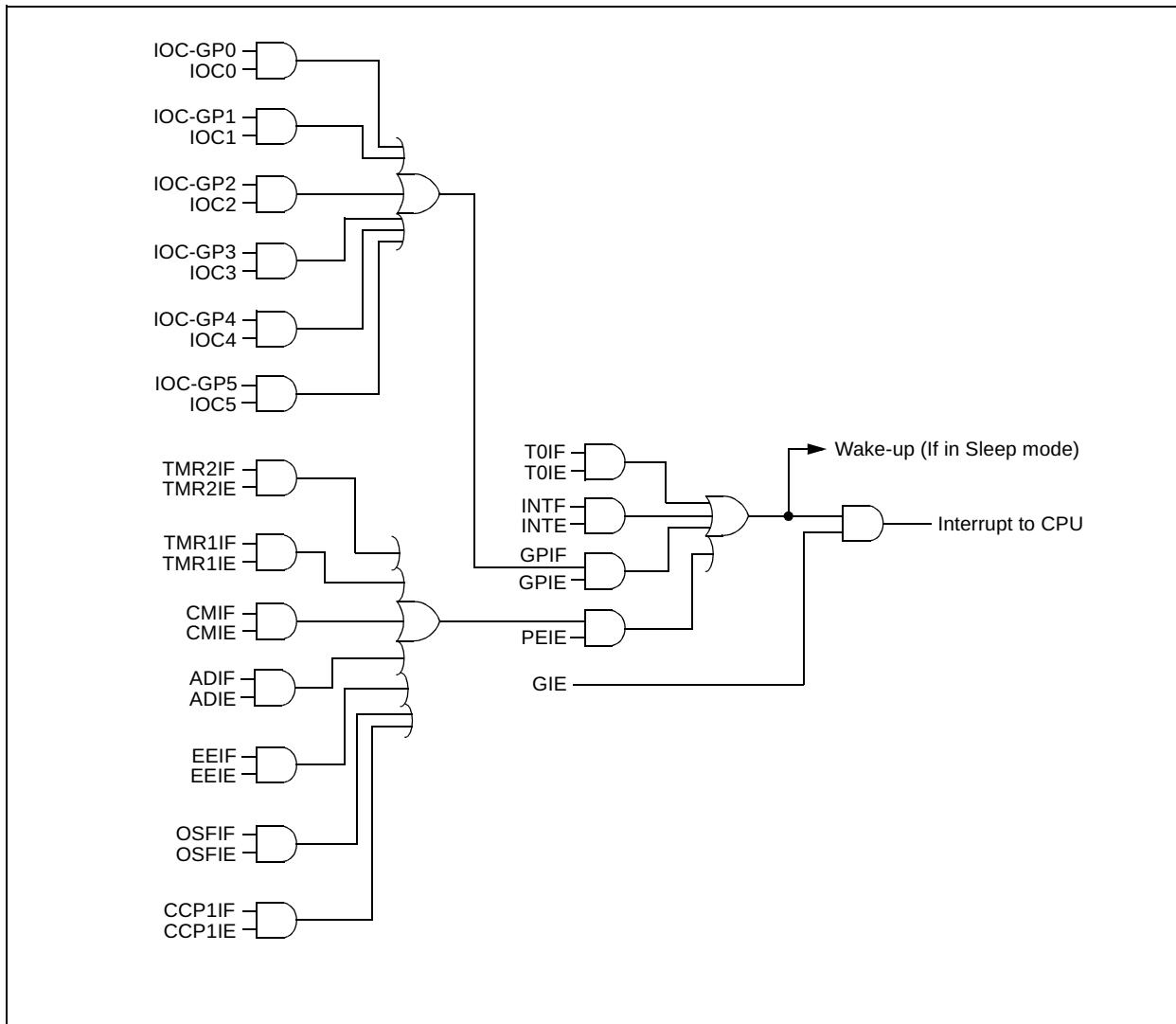
An overflow (FFh → 00h) in the TMRO register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing the TOIE bit of the INTCON register. See **Section 5.0 “Timer0 Module”** for operation of the Timer0 module.

12.4.3 GPIO INTERRUPT

An input change on GPIO change sets the GPIF bit of the INTCON register. The interrupt can be enabled/disabled by setting/clearing the GPIE bit of the INTCON register. Plus, individual pins can be configured through the IOC register.

Note: If a change on the I/O pin should occur when any GPIO operation is being executed, then the GPIF interrupt flag may not get set.

FIGURE 12-7: INTERRUPT LOGIC



PIC12F683

FIGURE 12-8: INT PIN INTERRUPT TIMING

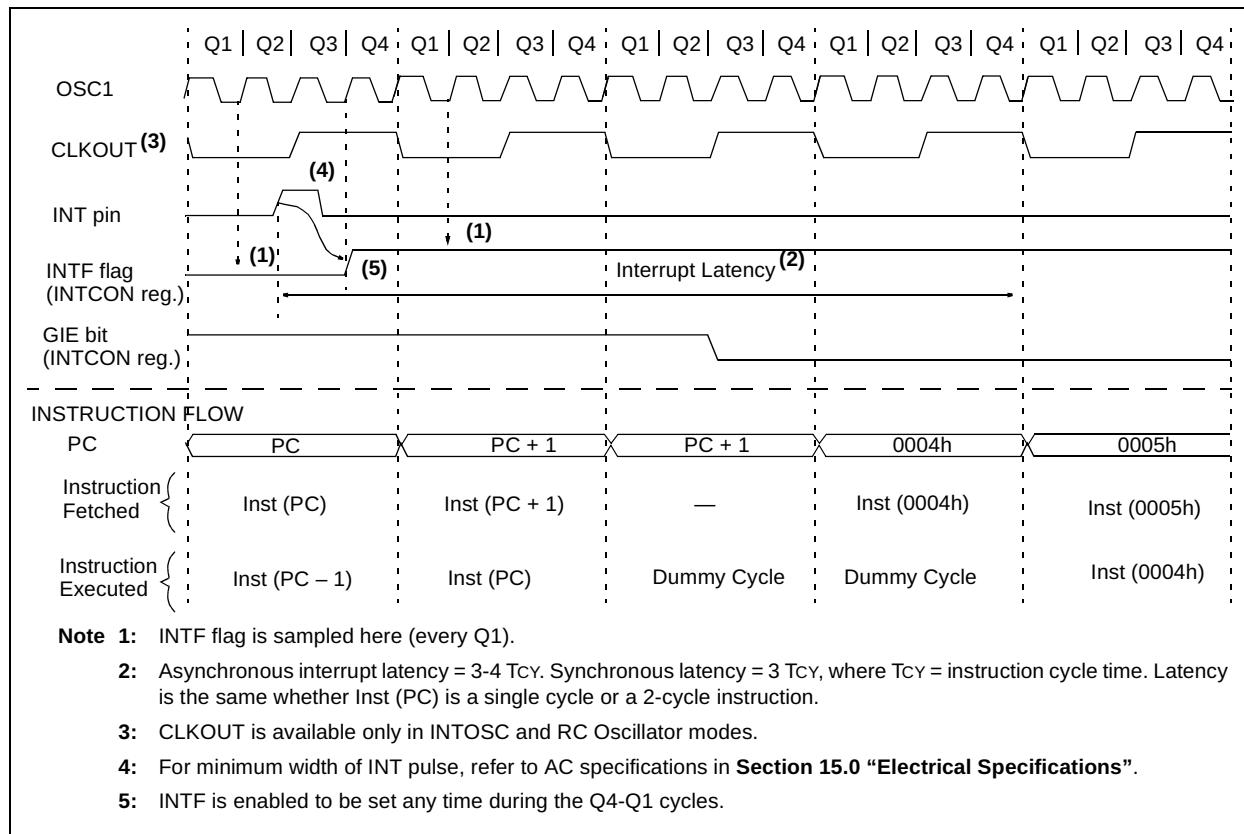


TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 0000
IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
PIR1	EEEIF	ADIF	CCP1IF	—	CMIF	OSFIF	TMR2IF	TMR1IF	000- 0000	000- 0000
PIE1	EEIE	ADIE	CCP1IE	—	CMIE	OSFIE	TMR2IE	TMR1IE	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, -- = unimplemented read as '0', q = value depends upon condition.

Shaded cells are not used by the interrupt module.

12.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (e.g., W and STATUS registers). This must be implemented in software.

Since the lower 16 bytes of all banks are common in the PIC12F683 (see Figure 2-2), temporary holding registers, W_TEMP and STATUS_TEMP, should be placed in here. These 16 locations do not require banking and therefore, makes it easier to context save and restore. The same code shown in Example 12-1 can be used to:

- Store the W register.
- Store the STATUS register.
- Execute the ISR code.
- Restore the Status (and Bank Select Bit register).
- Restore the W register.

Note: The PIC12F683 normally does not require saving the PCLATH. However, if computed GOTO's are used in the ISR and the main code, the PCLATH must be saved and restored in the ISR.

EXAMPLE 12-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF  W_TEMP           ;Copy W to TEMP register
SWAPF   STATUS,W         ;Swap status to be saved into W
                      ;Swaps are used because they do not affect the status bits
MOVWF   STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)                  ;Insert user code here
:
SWAPF   STATUS_TEMP,W   ;Swap STATUS_TEMP register into W
                      ;(sets bank to original state)
MOVWF   STATUS           ;Move W into STATUS register
SWAPF   W_TEMP,F         ;Swap W_TEMP
SWAPF   W_TEMP,W         ;Swap W_TEMP into W
```

12.6 Watchdog Timer (WDT)

The WDT has the following features:

- Operates from the LFINTOSC (31 kHz)
- Contains a 16-bit prescaler
- Shares an 8-bit prescaler with Timer0
- Time-out period is from 1 ms to 268 seconds
- Configuration bit and software controlled

WDT is cleared under certain conditions described in Table 12-7.

12.6.1 WDT OSCILLATOR

The WDT derives its time base from the 31 kHz LFINTOSC. The LTS bit of the OSCCON register does not reflect that the LFINTOSC is enabled.

The value of WDTCON is '--- 0 1000' on all Resets. This gives a nominal time base of 17 ms.

Note: When the Oscillator Start-up Timer (OST) is invoked, the WDT is held in Reset, because the WDT Ripple Counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

12.6.2 WDT CONTROL

The WDTE bit is located in the Configuration Word register. When set, the WDT runs continuously.

When the WDTE bit in the Configuration Word register is set, the SWDTEN bit of the WDTCON register has no effect. If WDTE is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits of the OPTION register have the same function as in previous versions of the PIC12F683 Family of microcontrollers. See [Section 5.0 “Timer0 Module”](#) for more information.

FIGURE 12-9: WATCHDOG TIMER BLOCK DIAGRAM

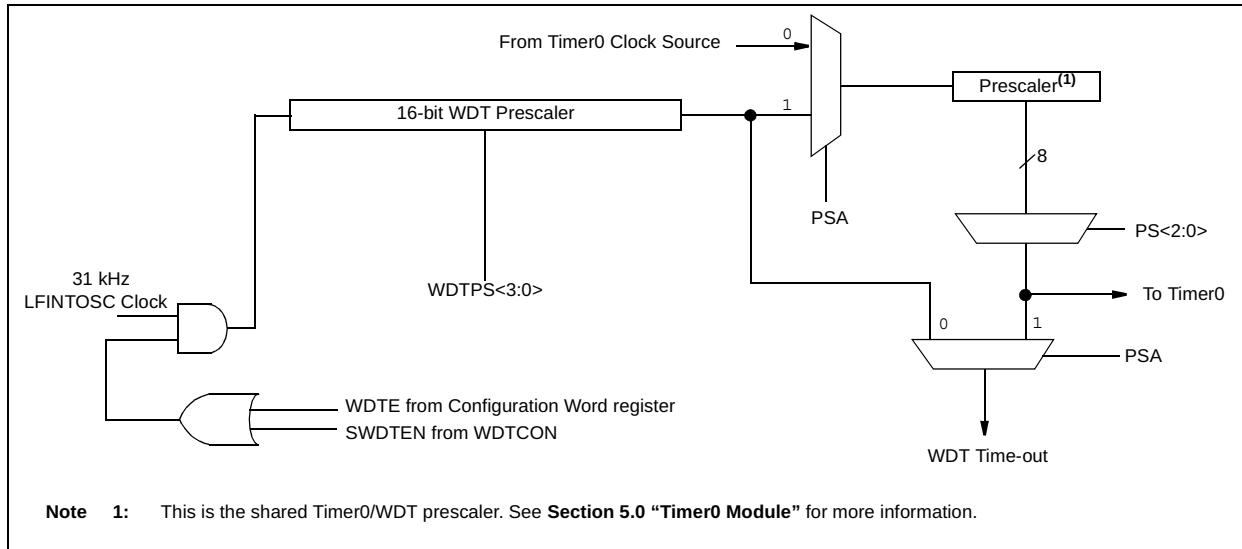


TABLE 12-7: WDT STATUS

Conditions	WDT
WDTE = 0	
CLRWDT Command	Cleared
Oscillator Fail Detected	
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, EXTCLK	
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST

REGISTER 12-2: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

0000 = 1:32

0001 = 1:64

0010 = 1:128

0011 = 1:256

0100 = 1:512 (Reset value)

0101 = 1:1024

0110 = 1:2048

0111 = 1:4096

1000 = 1:8192

1001 = 1:16384

1010 = 1:32768

1011 = 1:65536

1100 = Reserved

1101 = Reserved

1110 = Reserved

1111 = Reserved

bit 0 **SWDTEN:** Software Enable or Disable the Watchdog Timer⁽¹⁾

1 = WDT is turned on

0 = WDT is turned off (Reset value)

Note 1: If WDTE Configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE Configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

TABLE 12-8: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
WDTCON	—	—	—	WDTPS3	WDTPS2	WSTPS1	WDTPS0	SWDTEN	---0 1000	---0 1000
OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
CONFIG	CPD	CP	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	—	—

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 12-1 for operation of all Configuration Word register bits.

12.7 Power-Down Mode (Sleep)

The Power-down mode is entered by executing a `SLEEP` instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running.
- `PD` bit in the STATUS register is cleared.
- `TO` bit is set.
- Oscillator driver is turned off.
- I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD or Vss, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are high-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The `TOCKI` input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The `MCLR` pin must be at a logic high level.

Note: It should be noted that a Reset generated by a WDT time-out does not drive `MCLR` pin low.

12.7.1 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. External Reset input on `MCLR` pin.
2. Watchdog Timer wake-up (if WDT was enabled).
3. Interrupt from GP2/INT pin, GPIO change or a peripheral interrupt.

The first event will cause a device Reset. The two latter events are considered a continuation of program execution. The `TO` and `PD` bits in the STATUS register can be used to determine the cause of a device Reset. The `PD` bit, which is set on power-up, is cleared when Sleep is invoked. `TO` bit is cleared if WDT wake-up occurred.

The following peripheral interrupts can wake the device from Sleep:

1. Timer1 interrupt. Timer1 must be operating as an asynchronous counter.
2. ECCP Capture mode interrupt.
3. A/D conversion (when A/D clock source is FRC).
4. EEPROM write operation completion.
5. Comparator output changes state.
6. Interrupt-on-change.
7. External Interrupt from INT pin.

Other peripherals cannot generate interrupts since during Sleep, no on-chip clocks are present.

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a NOP after the `SLEEP` instruction.

Note: If the global interrupts are disabled (GIE is cleared) and any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from Sleep.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

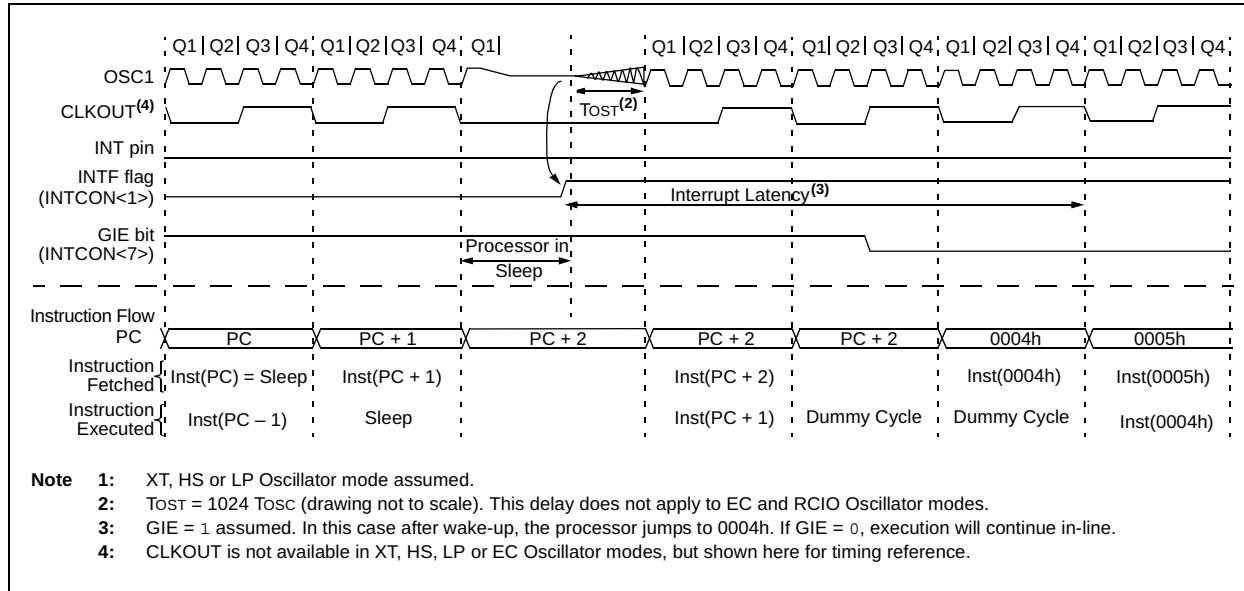
12.7.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a NOP. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will not be cleared, the `TO` bit will not be set and the `PD` bit will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from Sleep. The `SLEEP` instruction is executed. Therefore, the WDT and WDT prescaler and postscaler (if enabled) will be cleared, the `TO` bit will be set and the `PD` bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the `PD` bit. If the `PD` bit is set, the `SLEEP` instruction was executed as a NOP.

To ensure that the WDT is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction. See Figure 12-10 for more details.

FIGURE 12-10: WAKE-UP FROM SLEEP THROUGH INTERRUPT

12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using ICSP™ for verification purposes.

Note: The entire data EEPROM and Flash program memory will be erased when the code protection is turned off. See the “*PIC12F6XX/16F6XX Memory Programming Specification*” (DS41204) for more information.

12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

PIC12F683

12.10 In-Circuit Serial Programming™

The PIC12F683 microcontrollers can be serially programmed while in the end application circuit. This is simply done with five connections for:

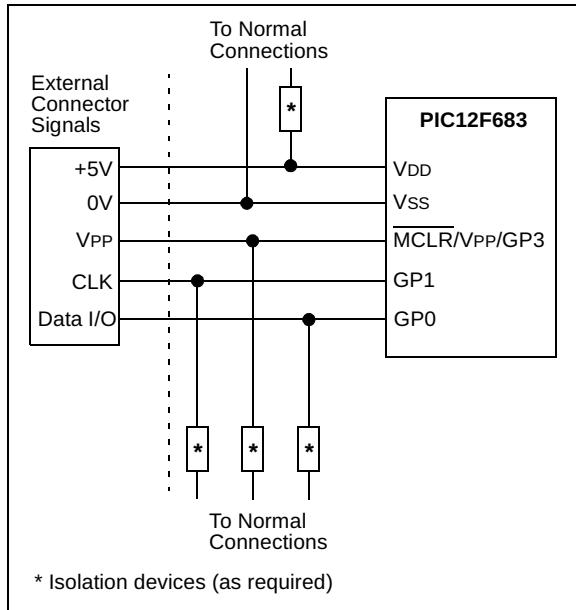
- clock
- data
- power
- ground
- programming voltage

This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH. See the "PIC12F6XX/16F6XX Memory Programming Specification" (DS41204) for more information. GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in Program/Verify mode.

A typical In-Circuit Serial Programming connection is shown in Figure 12-11.

FIGURE 12-11: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



12.11 In-Circuit Debugger

Since in-circuit debugging requires access to three pins, MPLAB® ICD 2 development with a 14-pin device is not practical. A special 14-pin PIC12F683 ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

A special debugging adapter allows the ICD device to be used in place of a PIC12F683 device. The debugging adapter is the only source of the ICD device.

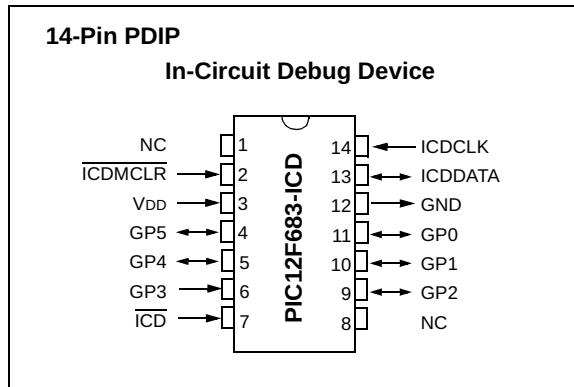
When the ICD pin on the PIC12F683 ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 12-9 shows which features are consumed by the background debugger.

TABLE 12-9: DEBUGGER RESOURCES

Resource	Description
Stack	1 level
Program Memory	Address 0h must be NOP 700h-7FFh

For more information, see "MPLAB® ICD 2 In-Circuit Debugger User's Guide" (DS51331), available on Microchip's web site (www.microchip.com).

FIGURE 12-12: 14-PIN ICD PINOUT



13.0 INSTRUCTION SET SUMMARY

The PIC12F683 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

Table 13-2 lists the instructions recognized by the MPASM™ assembler.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution time of 1 μ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

13.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF PORTA instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended consequence of clearing the condition that set the RAIF flag.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
C	Carry bit
DC	Digit carry bit
Z	Zero bit
PD	Power-down bit

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations			
13	8	7	6 0
OPCODE	d	f (FILE #)	
 d = 0 for destination W d = 1 for destination f f = 7-bit file register address			
Bit-oriented file register operations			
13	10	9	7 6 0
OPCODE	b (BIT #)	f (FILE #)	
 b = 3-bit bit address f = 7-bit file register address			
Literal and control operations			
General			
13	8	7	0
OPCODE		k (literal)	
 k = 8-bit immediate value			
CALL and GOTO instructions only			
13	11	10	0
OPCODE		k (literal)	
 k = 11-bit immediate value			

PIC12F683

TABLE 13-2: PIC12F683 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes
			MSb	Lsb				
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z 1, 2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z 1, 2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z 2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z 1, 2
DECFSZ	f, d	Decrement f	1	00	0011	dfff	ffff	Z 1, 2
DECF	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff	1, 2, 3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z 1, 2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff	1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z 1, 2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z 1, 2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff	Z 1, 2
NOP	-	No Operation	1	00	0000	0xx0	0000	
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C 1, 2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C 1, 2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z 1, 2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff	1, 2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z 1, 2
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff	1, 2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff	1, 2
BTFC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff	3
BTFS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff	3
LITERAL AND CONTROL OPERATIONS								
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C, DC, Z
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk	
CLRWD	-	Clear Watchdog Timer	1	00	0000	0110	0100	TO, PD
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z
MOVlw	k	Move literal to W	1	11	00xx	kkkk	kkkk	
RETFIE	-	Return from interrupt	2	00	0000	0000	1001	
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk	
RETURN	-	Return from Subroutine	2	00	0000	0000	1000	
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	TO, PD
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC, Z
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z

- Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

13.2 Instruction Descriptions

ADDLW Add literal and W

Syntax:	[<i>label</i>] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

BCF Bit Clear f

Syntax:	[<i>label</i>] BCF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$0 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ADDWF Add W and f

Syntax:	[<i>label</i>] ADDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

BSF Bit Set f

Syntax:	[<i>label</i>] BSF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$1 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW AND literal with W

Syntax:	[<i>label</i>] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .AND. (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BTFSC Bit Test f, Skip if Clear

Syntax:	[<i>label</i>] BTFSC f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

ANDWF AND W with f

Syntax:	[<i>label</i>] ANDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .AND. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

PIC12F683

BTFSS	Bit Test f, Skip if Set	CLRWDT	Clear Watchdog Timer
Syntax:	[<i>label</i>] BTFSS f,b	Syntax:	[<i>label</i>] CLRWDT
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$	Operands:	None
Operation:	skip if $(f) = 1$	Operation:	$00h \rightarrow WDT$ $0 \rightarrow \underline{WDT}$ prescaler, $1 \rightarrow \underline{\underline{TO}}$ $1 \rightarrow \underline{PD}$
Status Affected:	None	Status Affected:	$\overline{\underline{TO}}, \overline{PD}$
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.	Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{\underline{TO}}$ and \overline{PD} are set.
CALL	Call Subroutine	COMF	Complement f
Syntax:	[<i>label</i>] CALL k	Syntax:	[<i>label</i>] COMF f,d
Operands:	$0 \leq k \leq 2047$	Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(PC)+1 \rightarrow TOS,$ $k \rightarrow PC<10:0>$, $(PCLATH<4:3>) \rightarrow PC<12:11>$	Operation:	$(\bar{f}) \rightarrow (\text{destination})$
Status Affected:	None	Status Affected:	Z
Description:	Call Subroutine. First, return address ($PC + 1$) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits $<10:0>$. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.	Description:	The contents of register 'f' are complemented. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.
CLRF	Clear f	DECf	Decrement f
Syntax:	[<i>label</i>] CLRF f	Syntax:	[<i>label</i>] DECf f,d
Operands:	$0 \leq f \leq 127$	Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$00h \rightarrow (f)$ $1 \rightarrow Z$	Operation:	$(f) - 1 \rightarrow (\text{destination})$
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.	Description:	Decrement register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.
CLRW	Clear W		
Syntax:	[<i>label</i>] CLRW		
Operands:	None		
Operation:	$00h \rightarrow (W)$ $1 \rightarrow Z$		
Status Affected:	Z		
Description:	W register is cleared. Zero bit (Z) is set.		

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow \text{PC} <10:0>$ $\text{PCLATH} <4:3> \rightarrow \text{PC} <12:11>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .OR. k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .OR. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

PIC12F683

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{dest})$
Status Affected:	Z
Description:	The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.
Words:	1
Cycles:	1
<u>Example:</u>	MOVF FSR, 0
After Instruction	
W = value in FSR register	
Z = 1	

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
<u>Example:</u>	MOVW OPTION F
Before Instruction	
OPTION = 0xFF W = 0x4F	
After Instruction	
OPTION = 0x4F W = 0x4F	

MOVLW	Move literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
<u>Example:</u>	MOVLW 0x5A
After Instruction	
W = 0x5A	

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
<u>Example:</u>	NOP

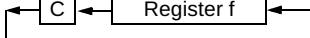
RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>RETFIE After Interrupt PC = TOS GIE = 1</pre>

RETLW	Return with literal in W
Syntax:	[<i>label</i>] RETLW <i>k</i>
Operands:	0 ≤ <i>k</i> ≤ 255
Operation:	<i>k</i> → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the eight bit literal ' <i>k</i> '. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Words:	1
Cycles:	2
<u>Example:</u>	<pre>CALL TABLE;W contains table ;offset value • ;W now has table value • • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table</pre>

Before Instruction
 W = 0x07
 After Instruction
 W = value of k8

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

PIC12F683

RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RLF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'. 

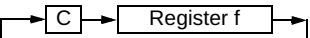
Words: 1
Cycles: 1
Example: RLF REG1,0

Before Instruction

REG1	=	1110 0110
C	=	0

After Instruction

REG1	=	1110 0110
W	=	1100 1100
C	=	1

RRF	Rotate Right f through Carry
Syntax:	[<i>label</i>] RRF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. 

SLEEP	Enter Sleep mode
Syntax:	[<i>label</i>] SLEEP
Operands:	None
Operation:	$00h \rightarrow \text{WDT}$, $0 \rightarrow \text{WDT prescaler}$, $1 \rightarrow \overline{\text{TO}}$, $0 \rightarrow \overline{\text{PD}}$
Status Affected:	$\overline{\text{TO}}, \overline{\text{PD}}$
Description:	The power-down Status bit, $\overline{\text{PD}}$ is cleared. Time-out Status bit, $\overline{\text{TO}}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWF	Subtract W from f								
Syntax:	[<i>label</i>] SUBWF f,d								
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$								
Operation:	$(f) - (W) \rightarrow (\text{destination})$								
Status Affected:	C, DC, Z								
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.								
<table border="1"> <tr> <td>C = 0</td> <td>W > f</td> </tr> <tr> <td>C = 1</td> <td>W ≤ f</td> </tr> <tr> <td>DC = 0</td> <td>$W<3:0> > f<3:0>$</td> </tr> <tr> <td>DC = 1</td> <td>$W<3:0> \leq f<3:0>$</td> </tr> </table>		C = 0	W > f	C = 1	W ≤ f	DC = 0	$W<3:0> > f<3:0>$	DC = 1	$W<3:0> \leq f<3:0>$
C = 0	W > f								
C = 1	W ≤ f								
DC = 0	$W<3:0> > f<3:0>$								
DC = 1	$W<3:0> \leq f<3:0>$								

XORLW	Exclusive OR literal with W
Syntax:	[<i>label</i>] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .XOR. k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

SWAPF	Swap Nibbles in f
Syntax:	[<i>label</i>] SWAPF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (\text{destination}<7:4>),$ $(f<7:4>) \rightarrow (\text{destination}<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORWF	Exclusive OR W with f
Syntax:	[<i>label</i>] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .XOR. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

PIC12F683

NOTES:

14.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C18 and MPLAB C30 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD 2
- Device Programmers
 - PICSTART® Plus Development Programmer
 - MPLAB PM3 Device Programmer
 - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

14.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (assembly or C)
 - Mixed assembly and C
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

14.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

14.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

14.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

14.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

14.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

14.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

14.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

14.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart® battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest "Product Selector Guide" (DS00148) for the complete list of demonstration, development and evaluation kits.

15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

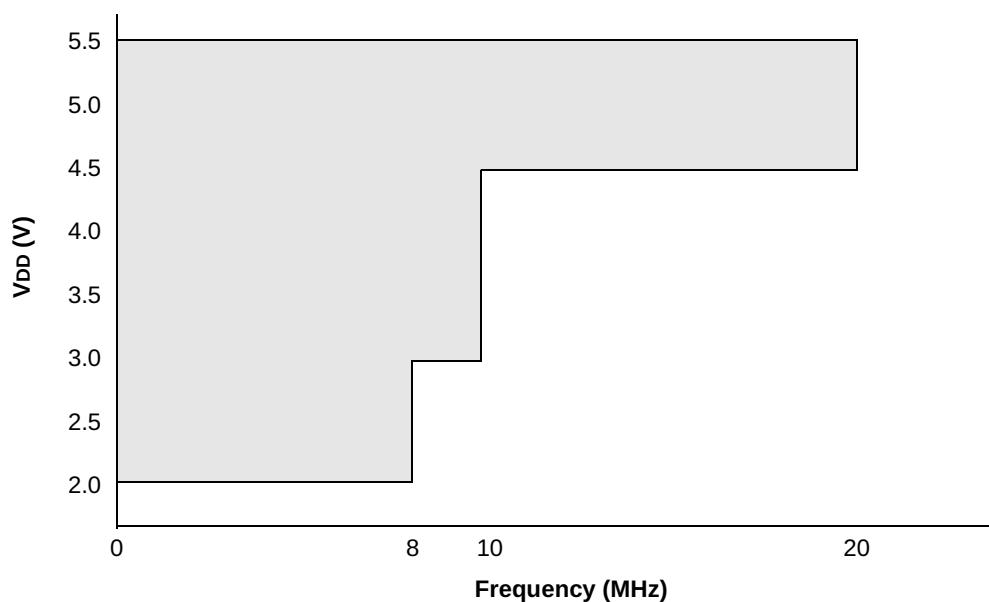
Ambient temperature under bias.....	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to Vss	-0.3V to +6.5V
Voltage on MCLR with respect to Vss	-0.3V to +13.5V
Voltage on all other pins with respect to Vss	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of Vss pin	95 mA
Maximum current into VDD pin	95 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by GPIO.....	90 mA
Maximum current sourced GPIO.....	90 mA

Note 1: Power dissipation is calculated as follows: P_{DIS} = V_{DD} x {I_{DD} - \sum I_{OH}} + \sum {(V_{DD} - V_{OH}) x I_{OH}} + \sum (V_{OL} x I_{OL}).

[†] NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

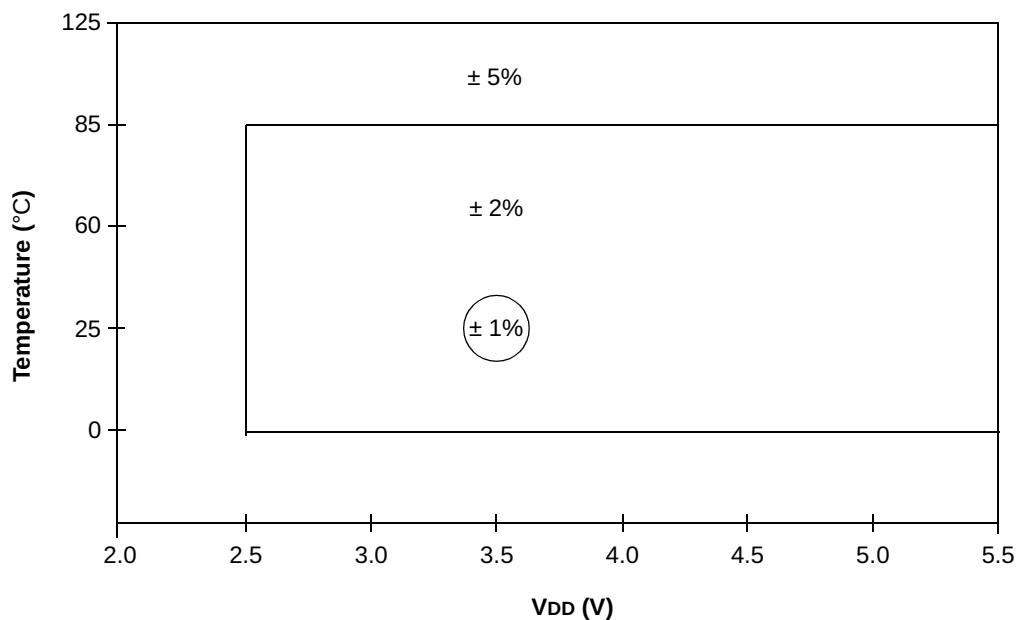
PIC12F683

**FIGURE 15-1: PIC12F683 VOLTAGE-FREQUENCY GRAPH,
 $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$**



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

FIGURE 15-2: HFINTOSC FREQUENCY ACCURACY OVER DEVICE V_{DD} AND TEMPERATURE



15.1 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	2.0	—	5.5	V	Fosc < = 8 MHz: HFINTOSC, EC
			2.0	—	5.5	V	Fosc < = 4 MHz
			3.0	—	5.5	V	Fosc < = 10 MHz
			4.5	—	5.5	V	Fosc < = 20 MHz
D002*	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	Device in Sleep mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See Section 12.3.1 “Power-on Reset” for details.
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 12.3.1 “Power-on Reset” for details.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

PIC12F683

15.2 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)^(1, 2)	—	11	16	µA	2.0	Fosc = 32 kHz LP Oscillator mode
		—	18	28	µA	3.0	
		—	35	54	µA	5.0	
D011*		—	140	240	µA	2.0	Fosc = 1 MHz XT Oscillator mode
		—	220	380	µA	3.0	
		—	380	550	µA	5.0	
D012		—	260	360	µA	2.0	Fosc = 4 MHz XT Oscillator mode
		—	420	650	µA	3.0	
		—	0.8	1.1	mA	5.0	
D013*		—	130	220	µA	2.0	Fosc = 1 MHz EC Oscillator mode
		—	215	360	µA	3.0	
		—	360	520	µA	5.0	
D014		—	220	340	µA	2.0	Fosc = 4 MHz EC Oscillator mode
		—	375	550	µA	3.0	
		—	0.65	1.0	mA	5.0	
D015		—	8	20	µA	2.0	Fosc = 31 kHz LFINTOSC mode
		—	16	40	µA	3.0	
		—	31	65	µA	5.0	
D016*		—	340	450	µA	2.0	Fosc = 4 MHz HFINTOSC mode
		—	500	700	µA	3.0	
		—	0.8	1.2	mA	5.0	
D017		—	410	650	µA	2.0	Fosc = 8 MHz HFINTOSC mode
		—	700	950	µA	3.0	
		—	1.30	1.65	mA	5.0	
D018		—	230	400	µA	2.0	Fosc = 4 MHz EXTRC mode ⁽³⁾
		—	400	680	µA	3.0	
		—	0.63	1.1	mA	5.0	
D019		—	2.6	3.25	mA	4.5	Fosc = 20 MHz HS Oscillator mode
		—	2.8	3.35	mA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula $IR = VDD/2REXT$ (mA) with REXT in kΩ.

15.3 DC Characteristics: PIC12F683-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020	Power-down Base Current(IPD)⁽²⁾	—	0.05	1.2	µA	2.0	WDT, BOR, Comparators, VREF and T1OSC disabled -40°C ≤ TA ≤ +25°C
		—	0.15	1.5	µA	3.0	
		—	0.35	1.8	µA	5.0	
		—	150	500	nA	3.0	
D021		—	1.0	2.2	µA	2.0	WDT Current ⁽¹⁾
		—	2.0	4.0	µA	3.0	
		—	3.0	7.0	µA	5.0	
D022		—	42	60	µA	3.0	BOR Current ⁽¹⁾
		—	85	122	µA	5.0	
D023		—	32	45	µA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	µA	3.0	
		—	120	160	µA	5.0	
D024		—	30	36	µA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	55	µA	3.0	
		—	75	95	µA	5.0	
D025*		—	39	47	µA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	72	µA	3.0	
		—	98	124	µA	5.0	
D026		—	4.5	7.0	µA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	5.0	8.0	µA	3.0	
		—	6.0	12	µA	5.0	
D027		—	0.30	1.6	µA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	1.9	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

PIC12F683

15.4 DC Characteristics: PIC12F683-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						V _{DD}	Note
D020E	Power-down Base Current (IPD)⁽²⁾	—	0.05	9	μA	2.0	WDT, BOR, Comparators, V _{REF} and T1OSC disabled
		—	0.15	11	μA	3.0	
		—	0.35	15	μA	5.0	
D021E		—	1	17.5	μA	2.0	WDT Current ⁽¹⁾
		—	2	19	μA	3.0	
		—	3	22	μA	5.0	
D022E		—	42	65	μA	3.0	BOR Current ⁽¹⁾
		—	85	127	μA	5.0	
D023E		—	32	45	μA	2.0	Comparator Current ⁽¹⁾ , both comparators enabled
		—	60	78	μA	3.0	
		—	120	160	μA	5.0	
D024E		—	30	70	μA	2.0	CVREF Current ⁽¹⁾ (high range)
		—	45	90	μA	3.0	
		—	75	120	μA	5.0	
D025E*		—	39	91	μA	2.0	CVREF Current ⁽¹⁾ (low range)
		—	59	117	μA	3.0	
		—	98	156	μA	5.0	
D026E		—	4.5	25	μA	2.0	T1OSC Current ⁽¹⁾ , 32.768 kHz
		—	5	30	μA	3.0	
		—	6	40	μA	5.0	
D027E		—	0.30	12	μA	3.0	A/D Current ⁽¹⁾ , no conversion in progress
		—	0.36	16	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD}.

15.5 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D033A	VIL	Input Low Voltage I/O Port: with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
			Vss	—	0.15 VDD	V	2.0V ≤ VDD ≤ 4.5V
		with Schmitt Trigger buffer	Vss	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		MCLR, OSC1 (RC mode) ⁽¹⁾	Vss	—	0.2 VDD	V	
		OSC1 (XT and LP modes)	Vss	—	0.3	V	
		OSC1 (HS mode)	Vss	—	0.3 VDD	V	
D040 D040A D041 D042 D043 D043A D043B	VIH	Input High Voltage I/O ports: with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
			0.25 VDD + 0.8	—	VDD	V	2.0V ≤ VDD ≤ 4.5V
		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	2.0V ≤ VDD ≤ 5.5V
		MCLR	0.8 VDD	—	VDD	V	
		OSC1 (XT and LP modes)	1.6	—	VDD	V	
		OSC1 (HS mode)	0.7 VDD	—	VDD	V	
		OSC1 (RC mode)	0.9 VDD	—	VDD	V	(Note 1)
D060 D061 D063	IIL	Input Leakage Current⁽²⁾ I/O ports	—	± 0.1	± 1	µA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
		MCLR ⁽³⁾	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD
		OSC1	—	± 0.1	± 5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
D070*	IPUR	GPIO Weak Pull-up Current	50	250	400	µA	VDD = 5.0V, VPIN = VSS
D080	VOL	Output Low Voltage ⁽⁵⁾ I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
D090	Voh	Output High Voltage ⁽⁶⁾ I/O ports	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: See **Section 10.4.1 "Using the Data EEPROM"** for additional information.

5: Including OSC2 in CLKOUT mode.

PIC12F683

15.5 DC Characteristics: PIC12F683-I (Industrial) PIC12F683-E (Extended) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	IULP	Ultra Low-Power Wake-Up Current	—	200	—	nA	See Application Note AN879, "Using the Microchip Ultra Low-Power Wake-up Module" (DS00879)
D101*	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101A*	CIO	All I/O pins	—	—	50	pF	
Data EEPROM Memory							
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	V _{MIN}	—	5.5	V	Using EECON1 to read/write V _{MIN} = Minimum operating voltage
D122	TDEW	Erase/Write Cycle Time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽⁴⁾	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
Program Flash Memory							
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	V _{MIN}	—	5.5	V	V _{MIN} = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 4:** See **Section 10.4.1 "Using the Data EEPROM"** for additional information.
- 5:** Including OSC2 in CLKOUT mode.

15.6 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$					
Param No.	Sym	Characteristic	Typ	Units	Conditions
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	84.6	$^{\circ}\text{C}/\text{W}$	8-pin PDIP package
			163.0	$^{\circ}\text{C}/\text{W}$	8-pin SOIC package
			52.4	$^{\circ}\text{C}/\text{W}$	8-pin DFN-S 4x4x0.9 mm package
			46.3	$^{\circ}\text{C}/\text{W}$	8-pin DFN-S 6x5 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	41.2	$^{\circ}\text{C}/\text{W}$	8-pin PDIP package
			38.8	$^{\circ}\text{C}/\text{W}$	8-pin SOIC package
			3.0	$^{\circ}\text{C}/\text{W}$	8-pin DFN-S 4x4x0.9 mm package
			2.6	$^{\circ}\text{C}/\text{W}$	8-pin DFN-S 6x5 mm package
TH03	T_J	Junction Temperature	150	$^{\circ}\text{C}$	For derated power calculations
TH04	PD	Power Dissipation	—	W	$\text{PD} = \text{PINTERNAL} + \text{PI/O}$
TH05	PINTERNAL	Internal Power Dissipation	—	W	$\text{PINTERNAL} = \text{IDD} \times \text{VDD}$ (NOTE 1)
TH06	PI/O	I/O Power Dissipation	—	W	$\text{PI/O} = \sum (\text{IOL} * \text{VOL}) + \sum (\text{IOH} * (\text{VDD} - \text{VOH}))$
TH07	PDER	Derated Power	—	W	$\text{PDER} = (T_J - \text{TA})/\theta_{JA}$ (NOTE 2, 3)

Note 1: IDD is current to run the chip alone without driving any load on the output pins.

2: TA = Ambient Temperature.

3: Maximum allowable power dissipation is the lower value of either the absolute maximum total power dissipation or derated power (PDER).

PIC12F683

15.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

2. TppS

T	
F	Frequency

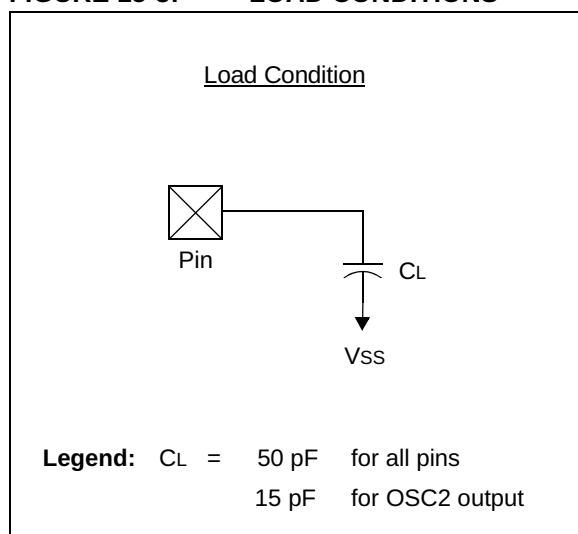
Lowercase letters (pp) and their meanings:

pp		T	
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	<u>RD</u>
cs	<u>CS</u>	rw	<u>RD or WR</u>
di	SDI	sc	SCK
do	SDO	ss	<u>SS</u>
dt	Data in	t0	T0CKI
io	I/O PORT	t1	T1CKI
mc	<u>MCLR</u>	wr	<u>WR</u>

Uppercase letters and their meanings:

S		T	
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 15-3: LOAD CONDITIONS



15.8 AC Characteristics: PIC12F683 (Industrial, Extended)

FIGURE 15-4: CLOCK TIMING

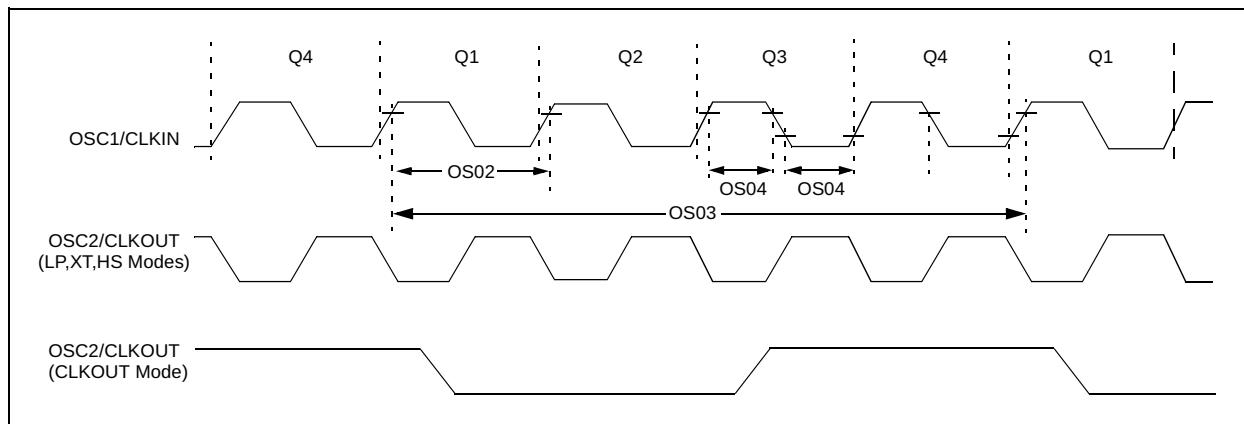


TABLE 15-1: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)

Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS01	FOSC	External CLKIN Frequency ⁽¹⁾	DC	—	37	kHz	LP Oscillator mode
			DC	—	4	MHz	XT Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	20	MHz	EC Oscillator mode
		Oscillator Frequency ⁽¹⁾	—	32.768	—	kHz	LP Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			1	—	20	MHz	HS Oscillator mode
			DC	—	4	MHz	RC Oscillator mode
OS02	Tosc	External CLKIN Period ⁽¹⁾	27	—	•	μs	LP Oscillator mode
			250	—	•	ns	XT Oscillator mode
			50	—	•	ns	HS Oscillator mode
			50	—	•	ns	EC Oscillator mode
		Oscillator Period ⁽¹⁾	—	30.5	—	μs	LP Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	1,000	ns	HS Oscillator mode
			250	—	—	ns	RC Oscillator mode
OS03	Tcy	Instruction Cycle Time ⁽¹⁾	200	Tcy	DC	ns	Tcy = 4/Fosc
OS04*	TosH, TosL	External CLKIN High, External CLKIN Low	2	—	—	μs	LP oscillator
			100	—	—	ns	XT oscillator
			20	—	—	ns	HS oscillator
OS05*	TosR, TosF	External CLKIN Rise, External CLKIN Fall	0	—	•	ns	LP oscillator
			0	—	•	ns	XT oscillator
			0	—	•	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

PIC12F683

TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic	Freq. Tolerance	Min	Typ†	Max	Units	Conditions
OS06	TWARM	Internal Oscillator Switch when running ⁽³⁾	—	—	—	2	Tosc	Slowest clock
OS07	Tsc	Fail-Safe Sample Clock Period ⁽¹⁾	—	—	21	—	ms	LFINTOSC/64
OS08	HFosc	Internal Calibrated HFINTOSC Frequency ⁽²⁾	$\pm 1\%$ $\pm 2\%$ $\pm 5\%$	7.92 7.84 7.60	8.0 8.0 8.0	8.08 8.16 8.40	MHz MHz MHz	$\text{VDD} = 3.5\text{V}, 25^{\circ}\text{C}$ $2.5\text{V} \leq \text{VDD} \leq 5.5\text{V}, 0^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ $2.0\text{V} \leq \text{VDD} \leq 5.5\text{V}, -40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C} (\text{Ind.}), -40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C} (\text{Ext.})$
OS09*	LFosc	Internal Uncalibrated LFINTOSC Frequency	—	15	31	45	kHz	
OS10*	Tiosc ST	HFINTOSC Oscillator Wake-up from Sleep Start-up Time	—	5.5	12	24	μs	$\text{VDD} = 2.0\text{V}, -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$
			—	3.5	7	14		$\text{VDD} = 3.0\text{V}, -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$
			—	3	6	11		$\text{VDD} = 5.0\text{V}, -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.
- 2:** To ensure these oscillator frequency tolerances, VDD and Vss must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.
- 3:** By design.

FIGURE 15-5: CLKOUT AND I/O TIMING

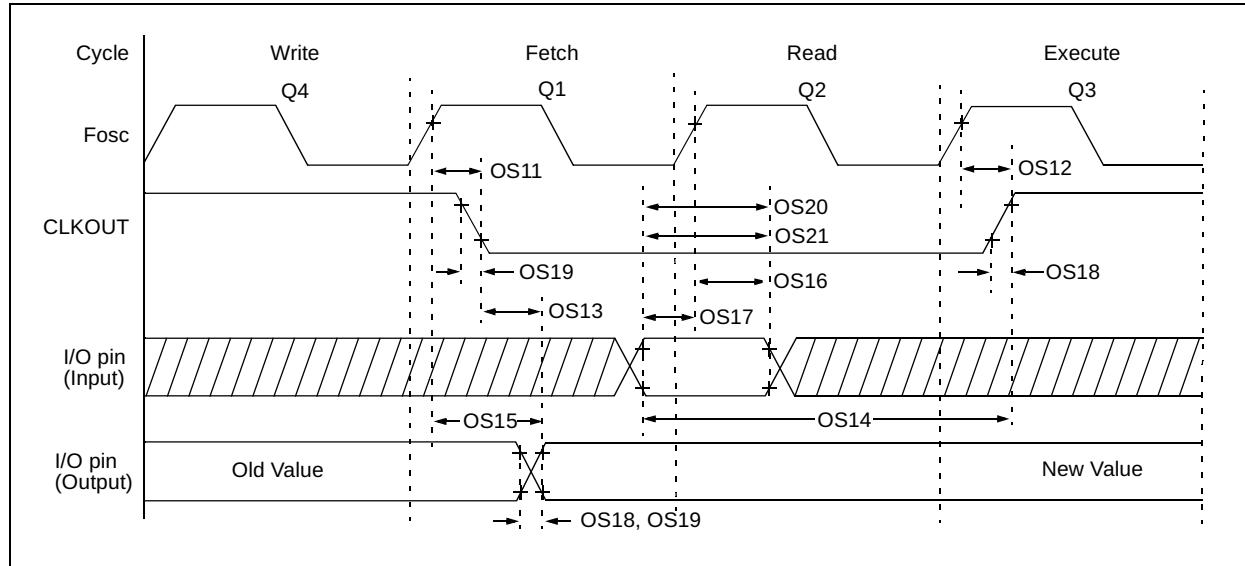


TABLE 15-3: CLKOUT AND I/O TIMING PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
OS11	TosH2ckL	Fosc \uparrow to CLKOUT \downarrow (1)	—	—	70	ns	VDD = 5.0V
OS12	TosH2ckH	Fosc \uparrow to CLKOUT \uparrow (1)	—	—	72	ns	VDD = 5.0V
OS13	TckL2ioV	CLKOUT \downarrow to Port out valid (1)	—	—	20	ns	
OS14	TioV2ckH	Port input valid before CLKOUT \uparrow (1)	Tosc + 200 ns	—	—	ns	
OS15*	TosH2ioV	Fosc \uparrow (Q1 cycle) to Port out valid	—	50	70	ns	VDD = 5.0V
OS16	TosH2iol	Fosc \uparrow (Q2 cycle) to Port input invalid (I/O in hold time)	50	—	—	ns	VDD = 5.0V
OS17	TioV2osH	Port input valid to Fosc \uparrow (Q2 cycle) (I/O in setup time)	20	—	—	ns	
OS18	TioR	Port output rise time (2)	—	15 40	72 32	ns	VDD = 2.0V VDD = 5.0V
OS19	TioF	Port output fall time (2)	—	28 15	55 30	ns	VDD = 2.0V VDD = 5.0V
OS20*	TINP	INT pin input high or low time	25	—	—	ns	
OS21*	TGPP	GPIO interrupt-on-change new input level time	Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.

2: Includes OSC2 in CLKOUT mode.

PIC12F683

FIGURE 15-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

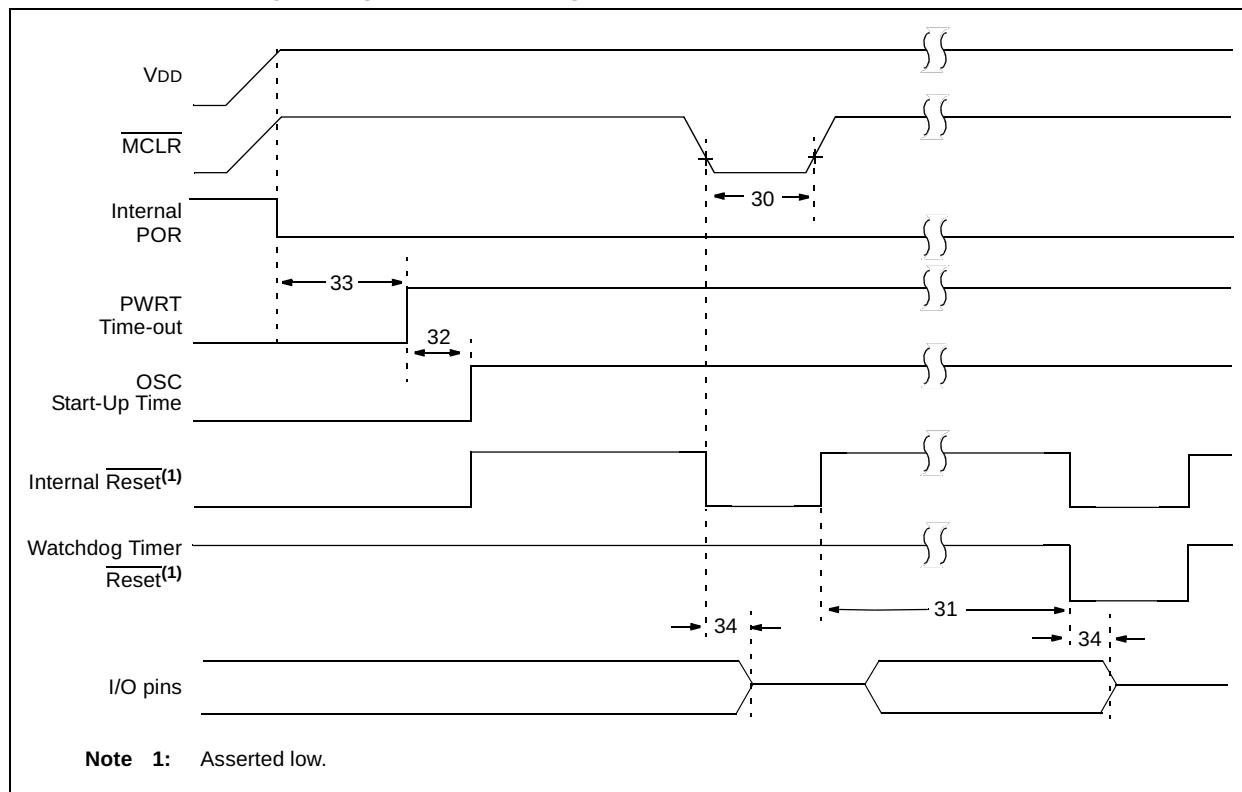


FIGURE 15-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS

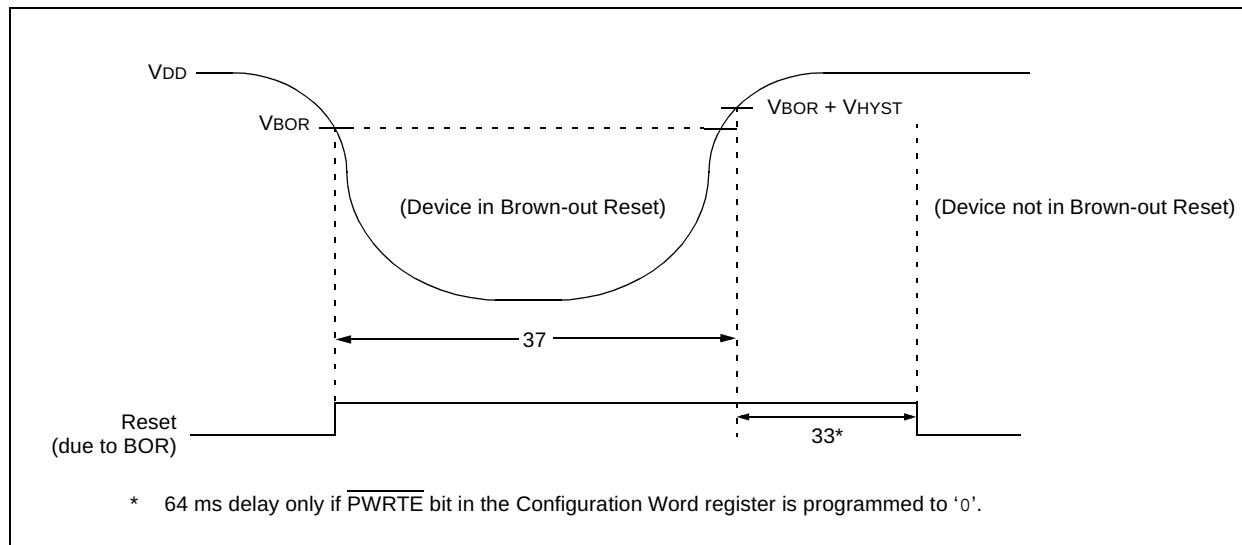


TABLE 15-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)							
Operating Temperature -40°C ≤ TA ≤ +125°C							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	T _{MCL}	MCLR Pulse Width (low)	2 5	— —	— —	μs μs	V _{DD} = 5V, -40°C to +85°C V _{DD} = 5V
31	T _{WDT}	Watchdog Timer Time-out Period (No Prescaler)	10 10	16 16	29 31	ms ms	V _{DD} = 5V, -40°C to +85°C V _{DD} = 5V
32	T _{OSS}	Oscillation Start-up Timer Period ^(1, 2)	—	1024	—	T _{osc}	(NOTE 3)
33*	T _{PWRT}	Power-up Timer Period	40	65	140	ms	
34*	T _{I/OZ}	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
35	V _{BOR}	Brown-out Reset Voltage	2.0	—	2.2	V	(NOTE 4)
36*	V _{HYST}	Brown-out Reset Hysteresis	—	50	—	mV	
37*	T _{BOR}	Brown-out Reset Minimum Detection Period	100	—	—	μs	V _{DD} ≤ V _{BOR}

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (T_{CY}) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: By design.

3: Period of the slower clock.

4: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

PIC12F683

FIGURE 15-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

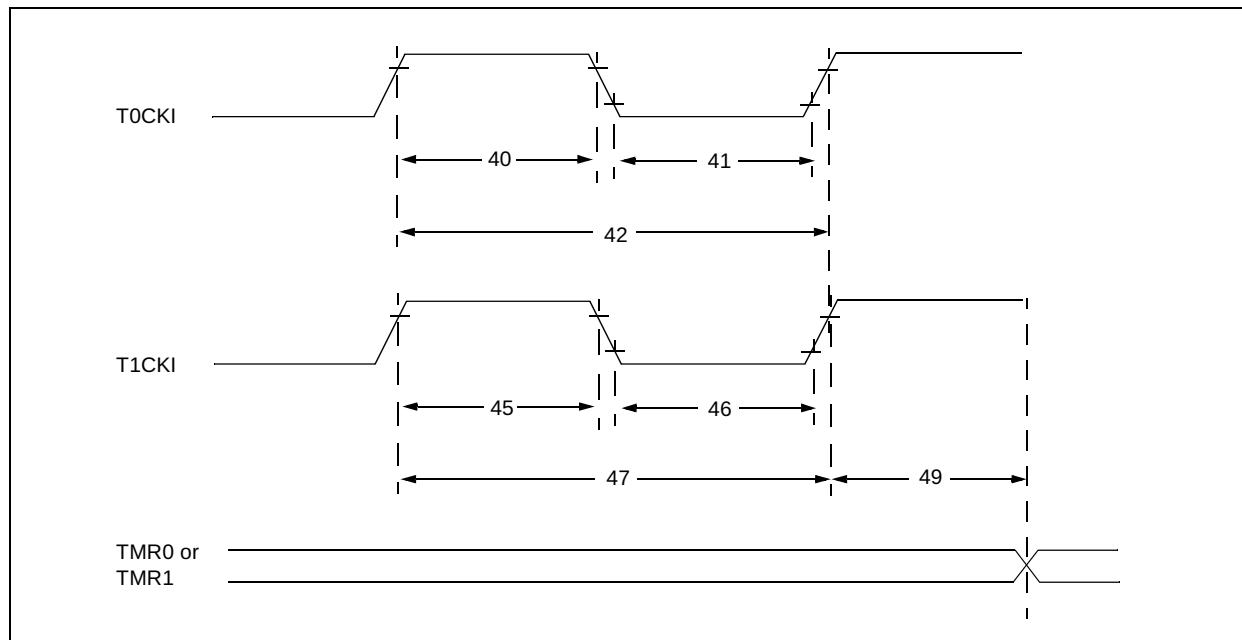


TABLE 15-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	T _{T0H}	T0CKI High Pulse Width	No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	T _{T0L}	T0CKI Low Pulse Width	No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	T _{T0P}	T0CKI Period		Greater of: 20 or $\frac{\text{T}_{CY} + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	T _{T1H}	T1CKI High Time	Synchronous, No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	T _{T1L}	T1CKI Low Time	Synchronous, No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	T _{T1P}	T1CKI Input Period	Synchronous	Greater of: 30 or $\frac{\text{T}_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	F _{T1}	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		—	32.768	—	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 T _{osc}	—	7 T _{osc}	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-9: CAPTURE/COMPARE/PWM TIMINGS (ECCP)

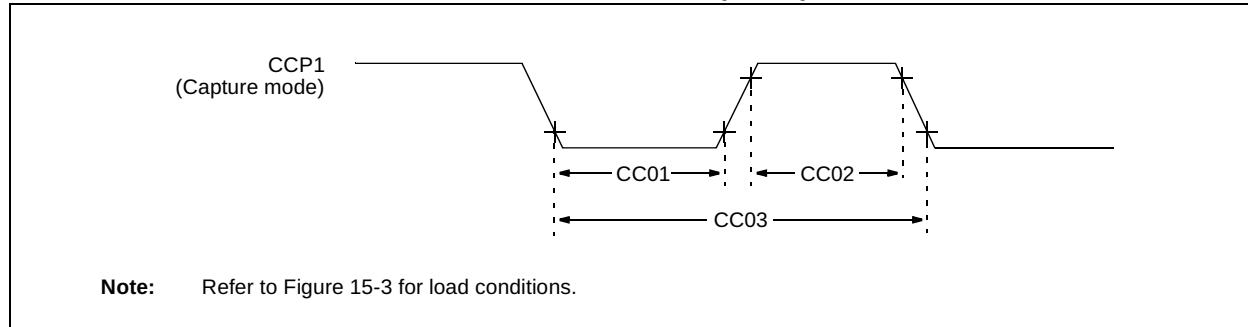


TABLE 15-6: CAPTURE/COMPARE/PWM REQUIREMENTS (ECCP)

Standard Operating Conditions (unless otherwise stated) Operating Temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$								
Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
CC01*	TccL	CCP1 Input Low Time	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCP1 Input High Time	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCP1 Input Period		$\frac{3\text{Tcy} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC12F683

TABLE 15-7: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)								
Operating Temperature -40°C ≤ TA ≤ +125°C								
Param No.	Sym	Characteristics		Min	Typ†	Max	Units	Comments
CM01	Vos	Input Offset Voltage		—	± 5.0	± 10	mV	(VDD - 1.5)/2
CM02	VCM	Input Common Mode Voltage		0	—	VDD - 1.5	V	
CM03*	CMRR	Common Mode Rejection Ratio		+55	—	—	dB	
CM04*	TRT	Response Time	Falling	—	150	600	ns	(NOTE 1)
			Rising	—	200	1000	ns	
CM05*	TMC2coV	Comparator Mode Change to Output Valid		—	—	10	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Response time is measured with one comparator input at (VDD - 1.5)/2 - 100 mV to (VDD - 1.5)/2 + 20 mV.

TABLE 15-8: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Operating temperature -40°C ≤ TA ≤ +125°C							
Param No.	Sym	Characteristics	Min	Typ†	Max	Units	Comments
CV01*	CLSB	Step Size ⁽²⁾	— —	VDD/24 VDD/32	— —	V V	Low Range (VRR = 1) High Range (VRR = 0)
CV02*	CACC	Absolute Accuracy	— —	— —	± 1/2 ± 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
CV03*	CR	Unit Resistor Value (R)	—	2k	—	Ω	
CV04*	CST	Settling Time ⁽¹⁾	—	—	10	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

2: See Section 8.11 "Comparator Voltage Reference" for more information.

TABLE 15-9: PIC12F683 A/D CONVERTER (ADC) CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD01	NR	Resolution	—	—	10 bits	bit	
AD02	EIL	Integral Error	—	—	± 1	LSb	$\text{VREF} = 5.12\text{V}$
AD03	EDL	Differential Error	—	—	± 1	LSb	No missing codes to 10 bits $\text{VREF} = 5.12\text{V}$
AD04	Eoff	Offset Error	—	—	± 1	LSb	$\text{VREF} = 5.12\text{V}$
AD07	Egn	Gain Error	—	—	± 1	LSb	$\text{VREF} = 5.12\text{V}$
AD06	VREF	Reference Voltage ⁽³⁾	2.2	—	—	V	Absolute minimum to ensure 1 LSb accuracy
AD06A			2.7	—	VDD	V	
AD07	Vain	Full-Scale Range	Vss	—	VREF	V	
AD08	Zain	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
AD09*	Iref	VREF Input Current ⁽³⁾	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN.
			—	—	50	μA	During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF or VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

PIC12F683

TABLE 15-10: PIC12F683 A/D CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$							
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
AD130*	TAD	A/D Clock Period	1.6	—	9.0	μs	Tosc-based, VREF $\geq 3.0\text{V}$
		A/D Internal RC Oscillator Period	3.0	—	9.0	μs	Tosc-based, VREF full range ADCS<1:0> = 11 (ADRC mode)
AD131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	Set GO/DONE bit to new data in A/D Result register.
AD132*	TACQ	Acquisition Time	—	11.5	—	μs	—
AD133*	TAMP	Amplifier Settling Time	—	—	5	μs	—
AD134	TGO	Q4 to A/D Clock Start	—	Tosc/2	—	—	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.
			—	Tosc/2 + Tcy	—	—	

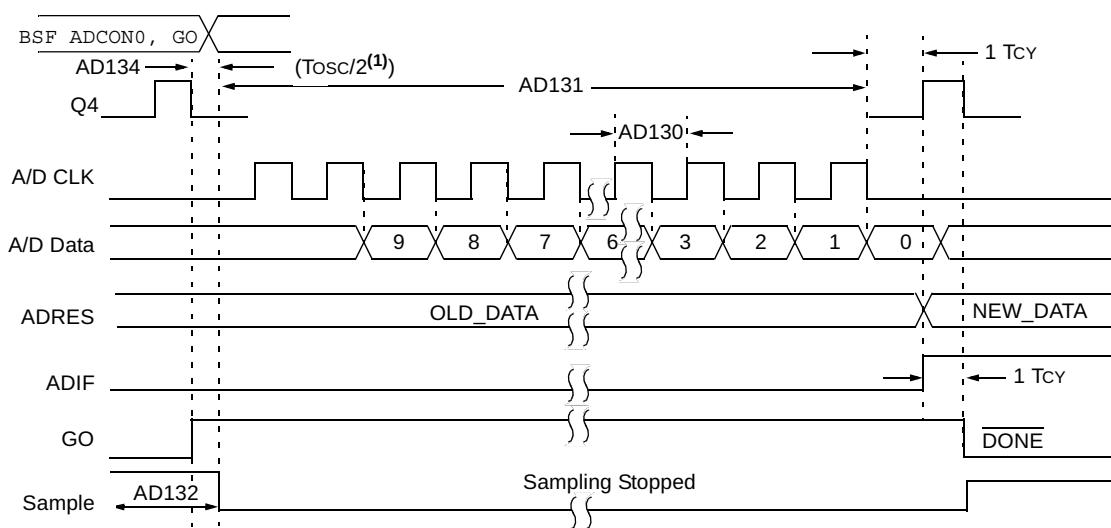
* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRESH and ADRESL registers may be read on the following Tcy cycle.

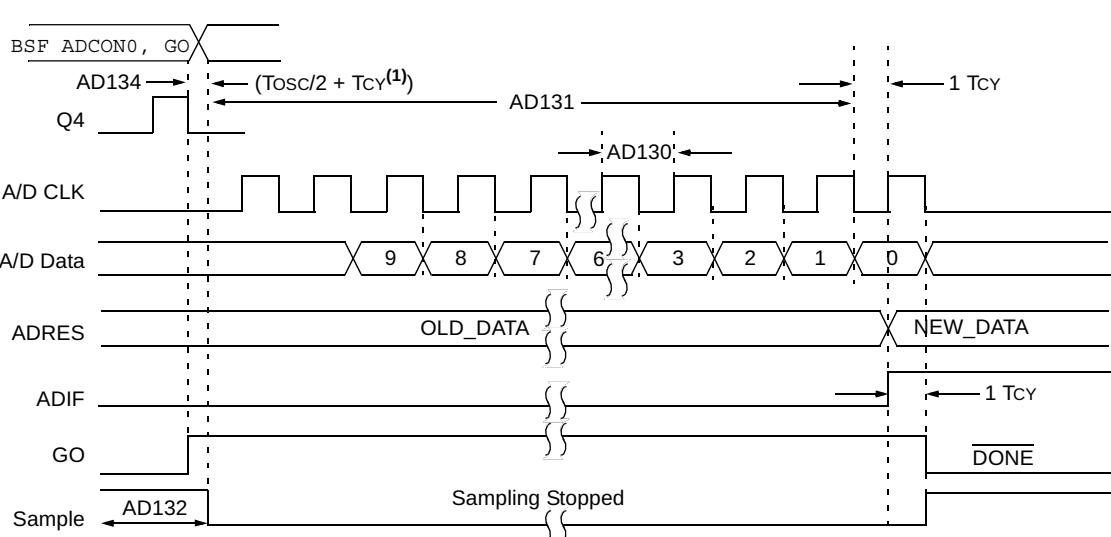
2: See **Section 9.3 “A/D Acquisition Requirements”** for minimum conditions.

FIGURE 15-10: PIC12F683 A/D CONVERSION TIMING (NORMAL MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

FIGURE 15-11: PIC12F683 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

PIC12F683

NOTES:

16.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

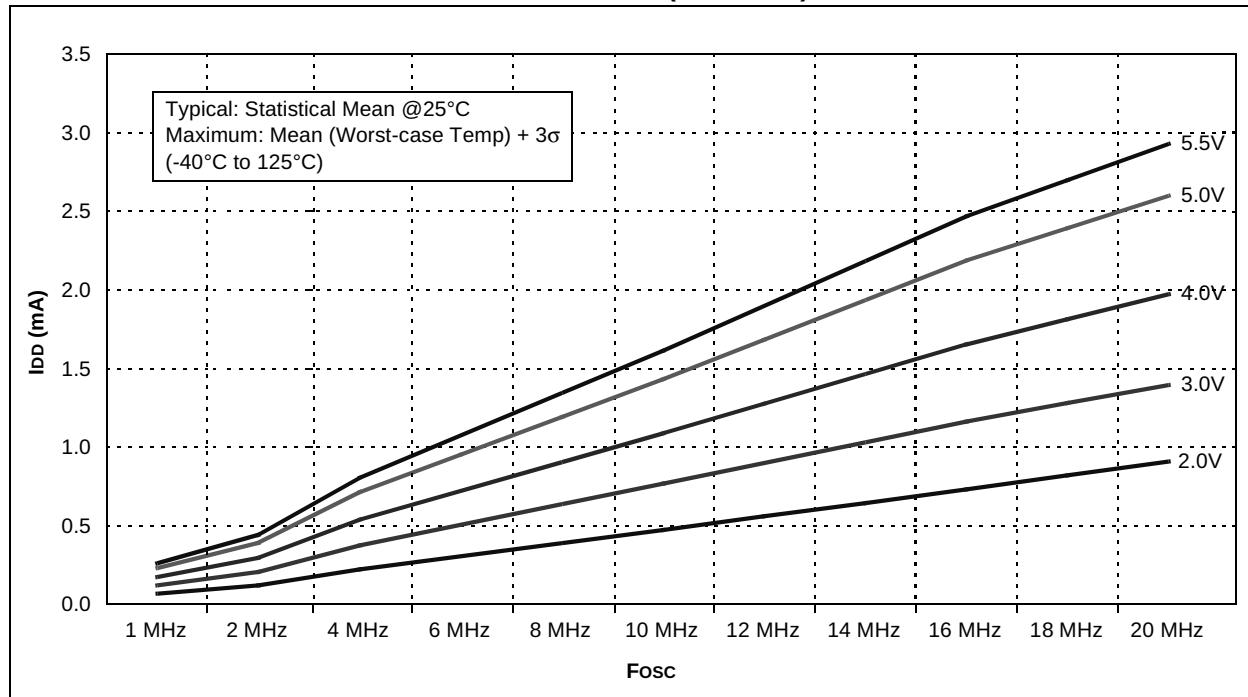
The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 16-1: TYPICAL IDD vs. Fosc OVER V_{DD} (EC MODE)



PIC12F683

FIGURE 16-2: MAXIMUM IDD VS. FOSC OVER VDD (EC MODE)

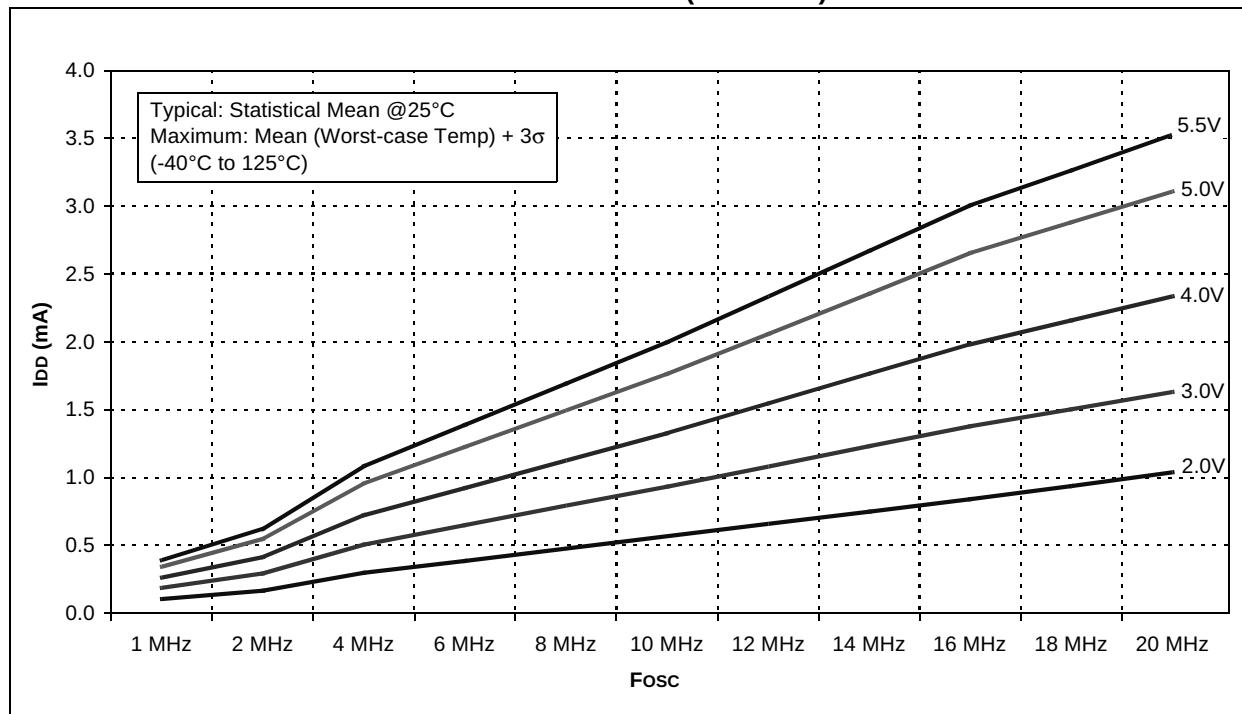


FIGURE 16-3: TYPICAL IDD VS. FOSC OVER VDD (HS MODE)

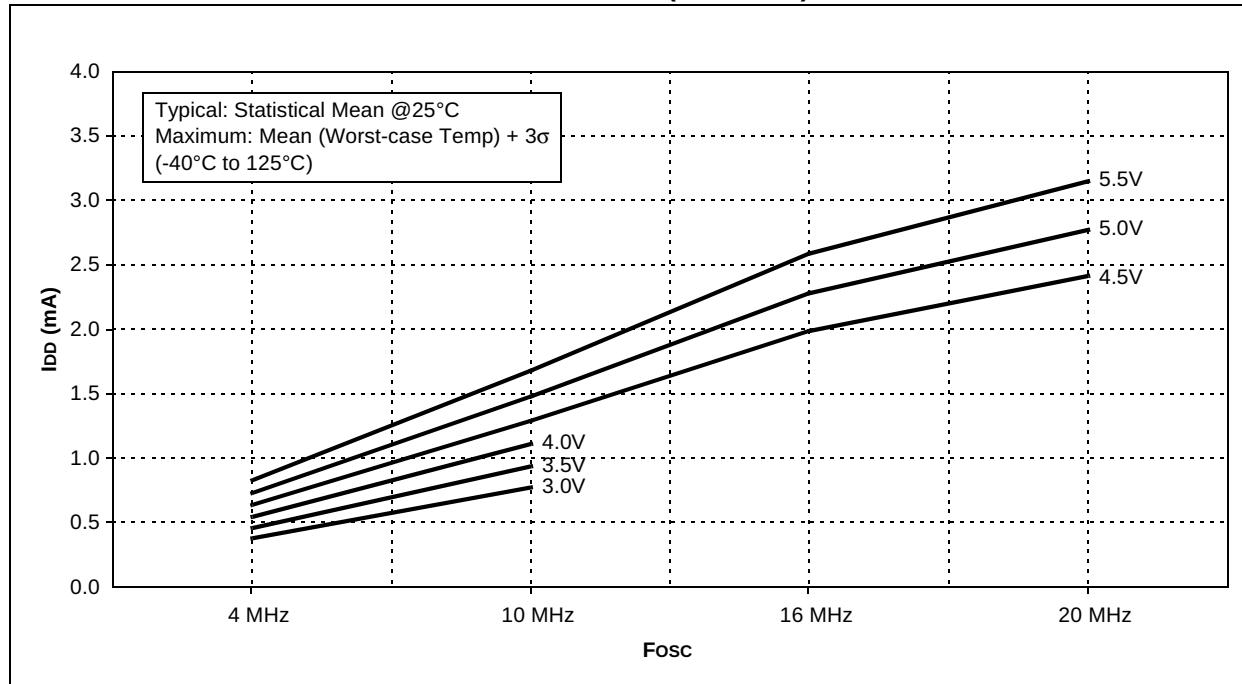
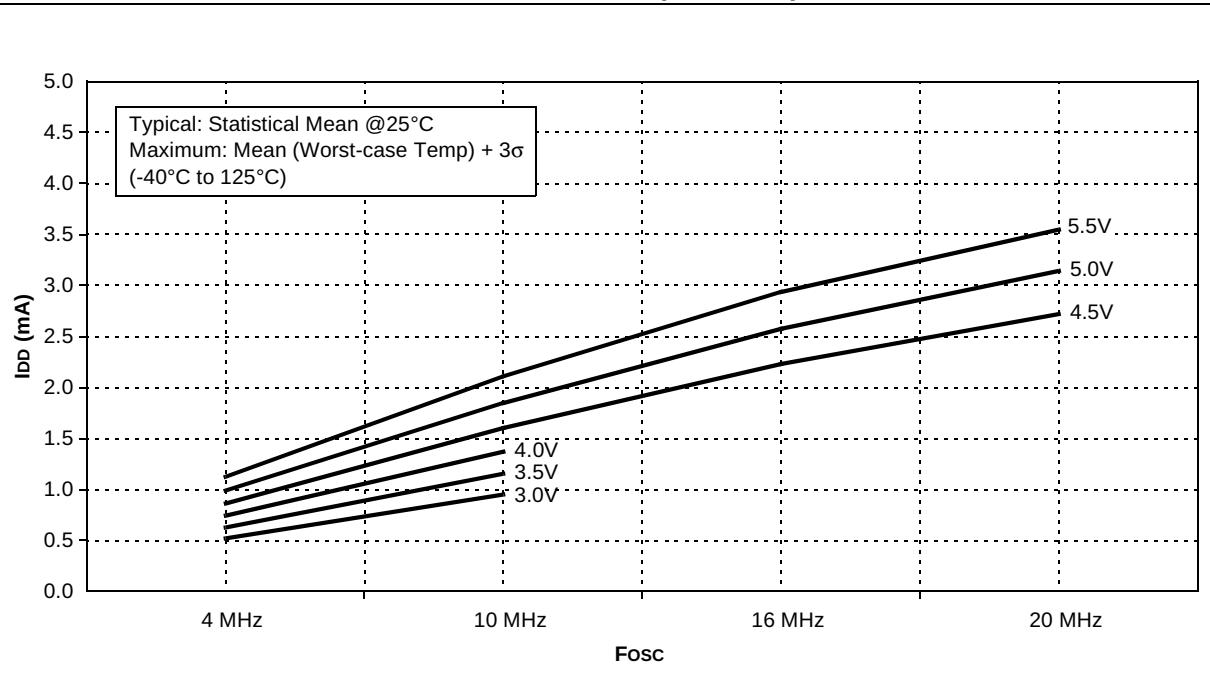
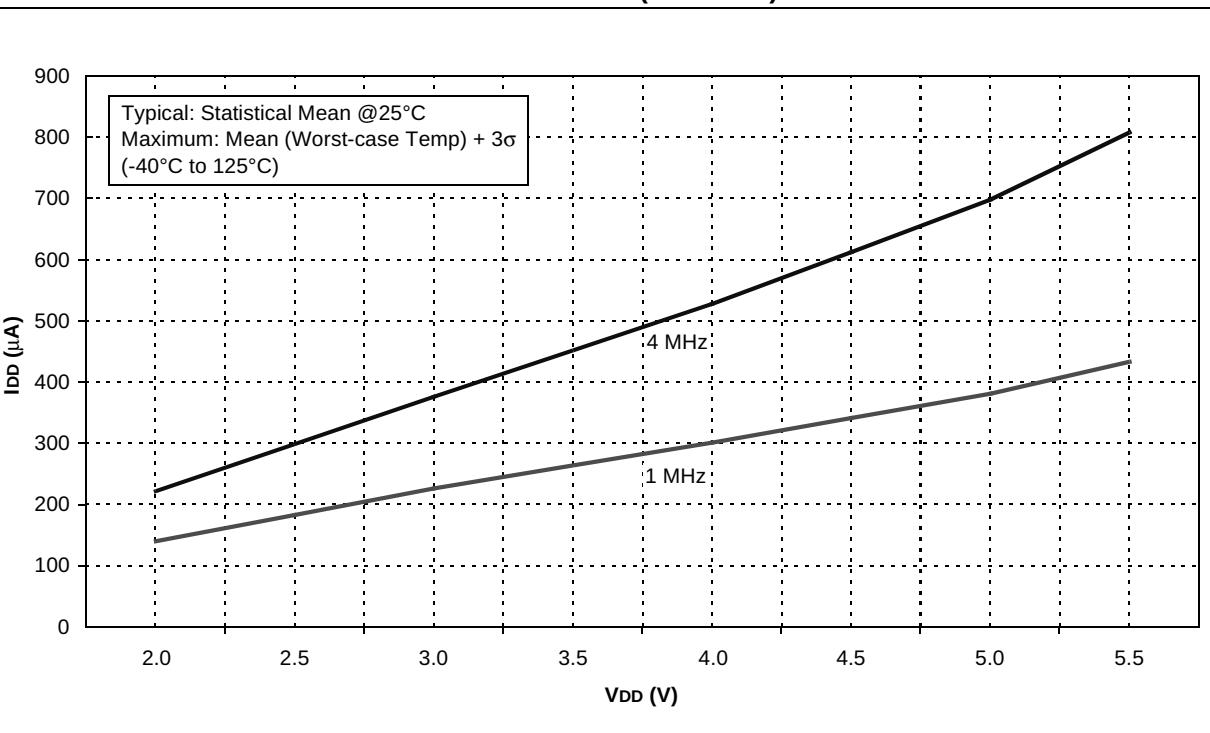


FIGURE 16-4: MAXIMUM IDD vs. Fosc OVER VDD (HS MODE)**FIGURE 16-5: TYPICAL IDD vs. VDD OVER Fosc (XT MODE)**

PIC12F683

FIGURE 16-6: MAXIMUM IDD VS. VDD OVER Fosc (XT MODE)

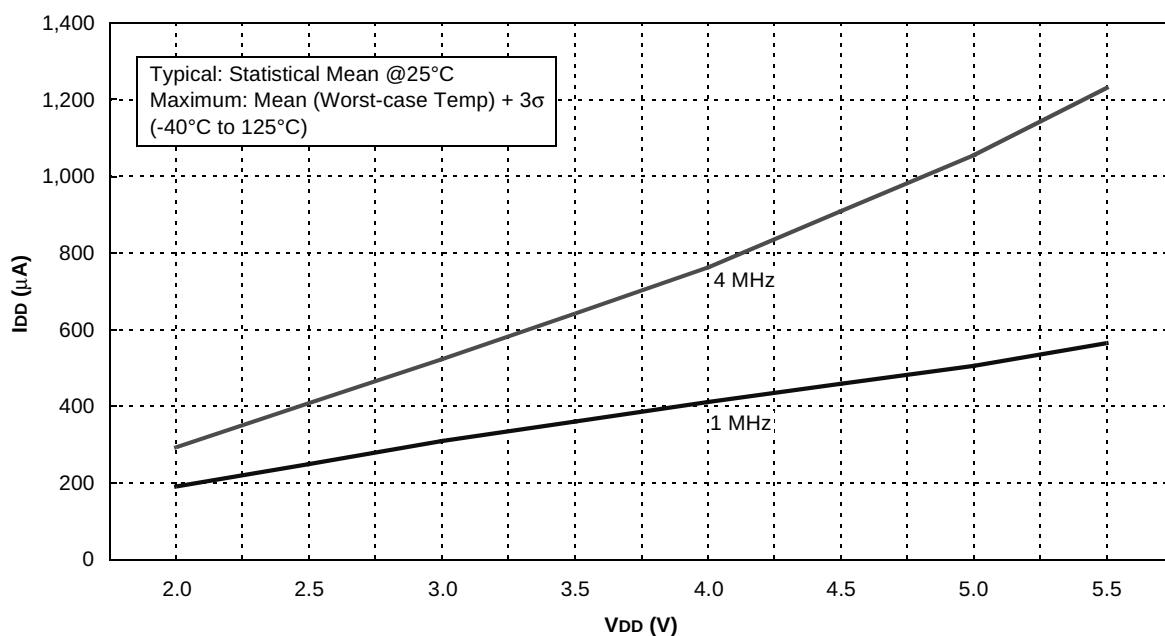


FIGURE 16-7: TYPICAL IDD VS. VDD OVER Fosc (EXT RC MODE)

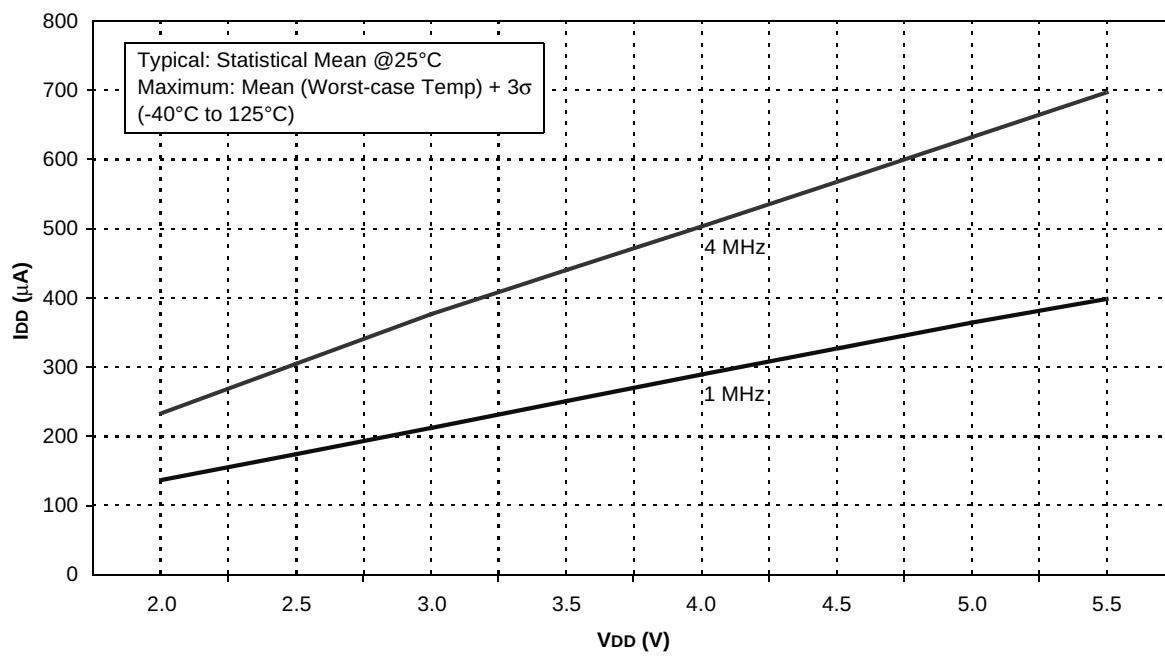
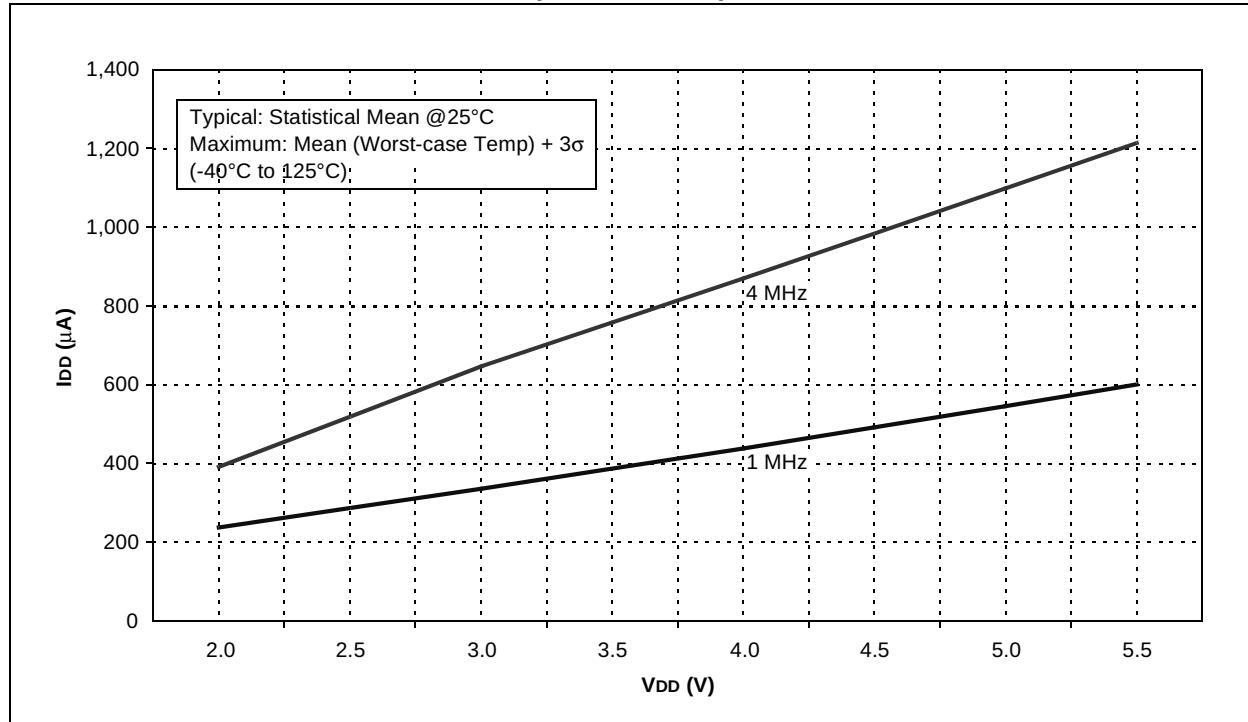
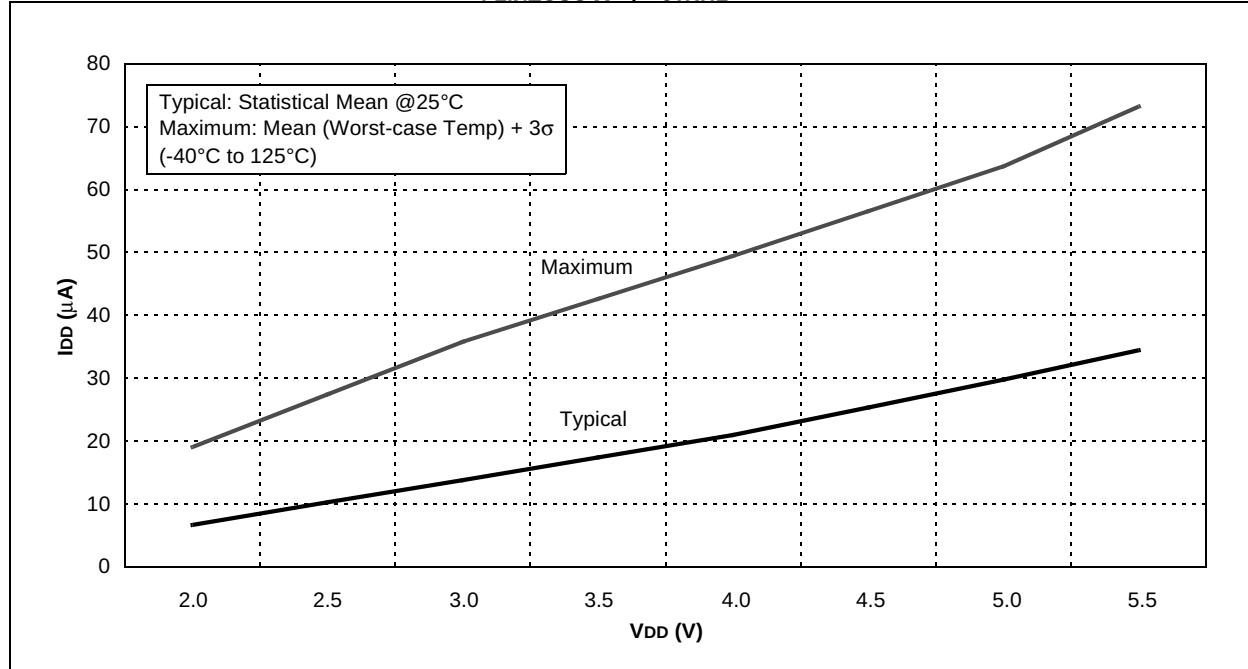


FIGURE 16-8: MAXIMUM IDD vs. VDD (EXTRC MODE)**FIGURE 16-9: IDD vs. VDD OVER Fosc (LFINTOSC MODE, 31 kHz)**

PIC12F683

FIGURE 16-10: IDD vs. VDD (LP MODE)

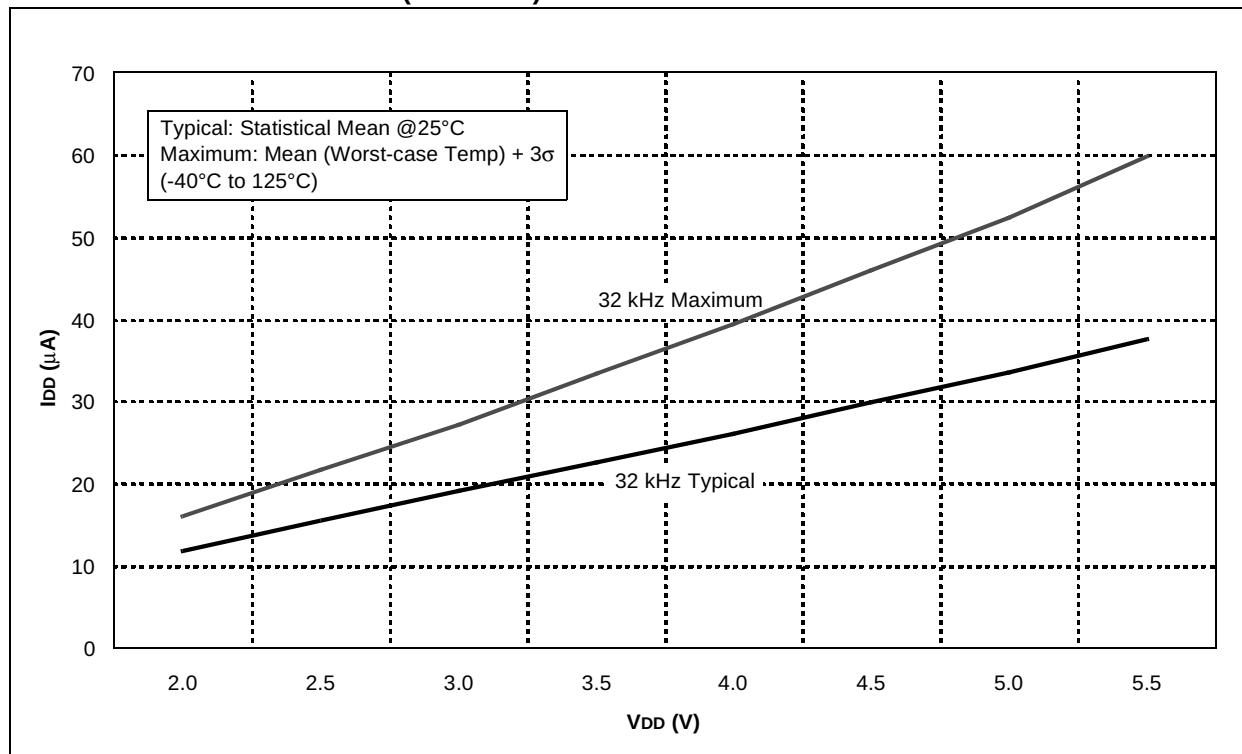


FIGURE 16-11: TYPICAL IDD vs. FOSC OVER VDD (HFINTOSC MODE)

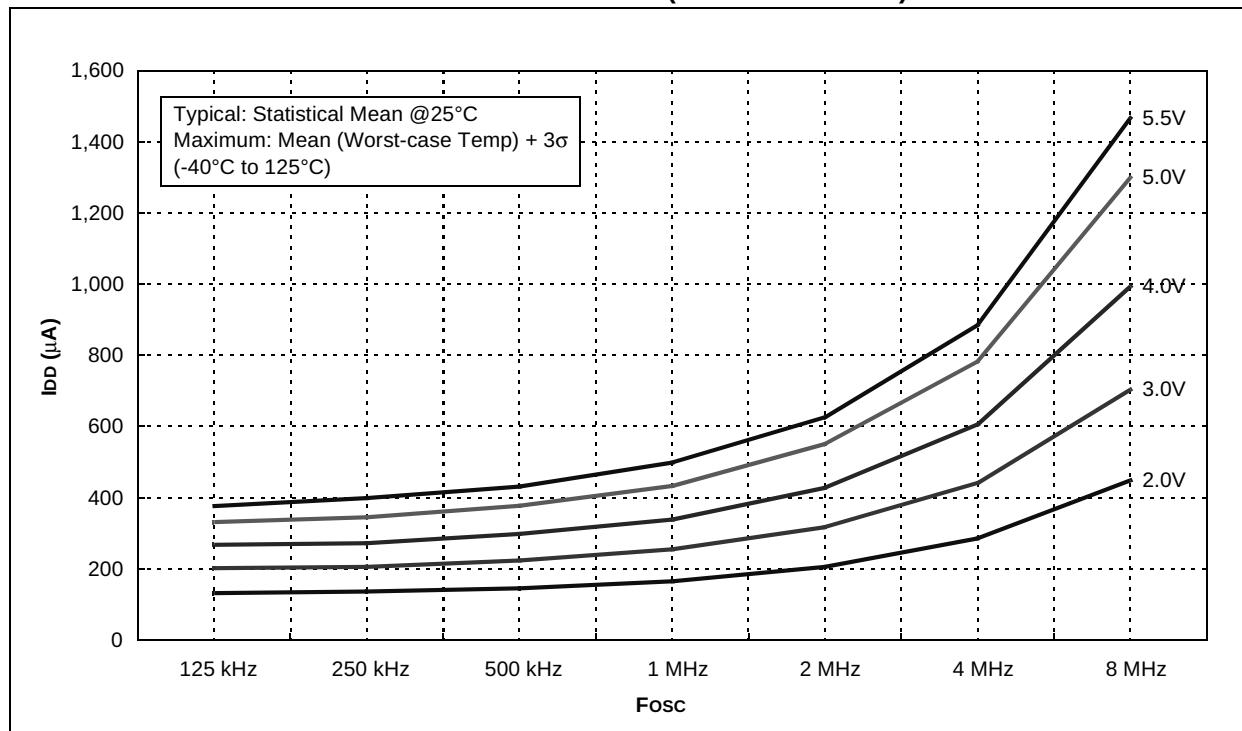


FIGURE 16-12: MAXIMUM IDD vs. Fosc OVER VDD (HFINTOSC MODE)

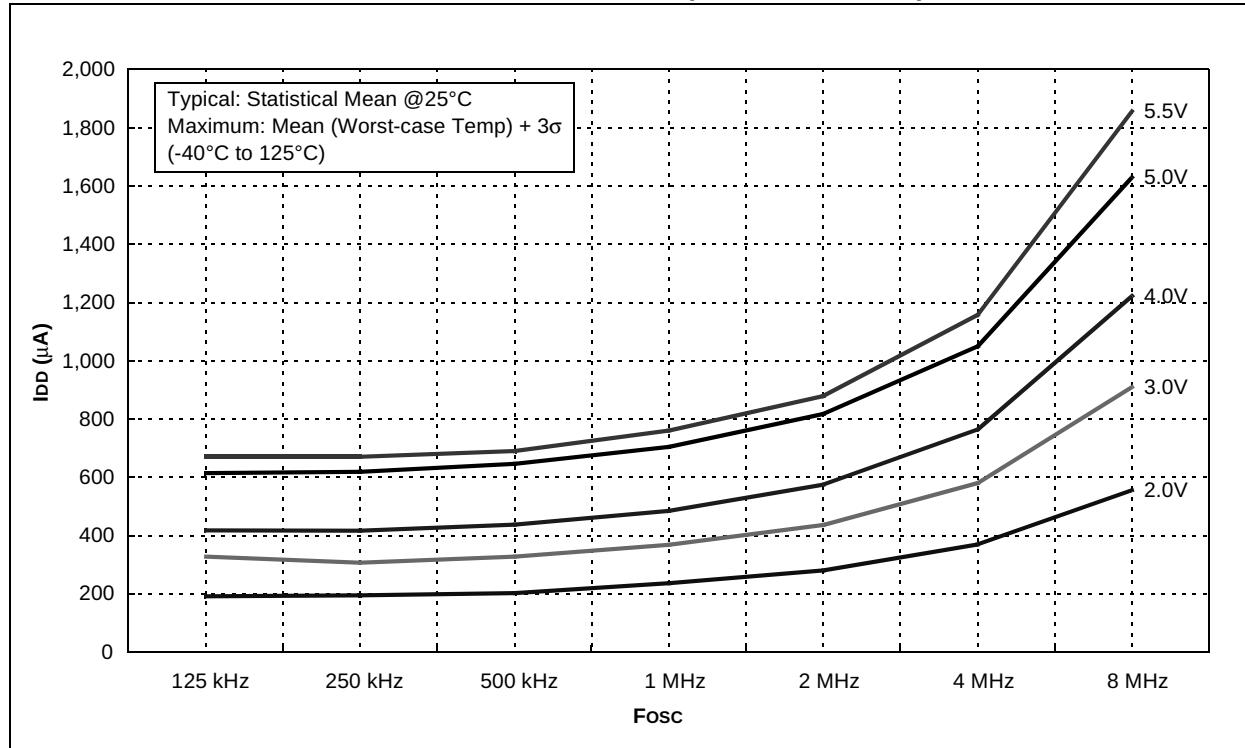
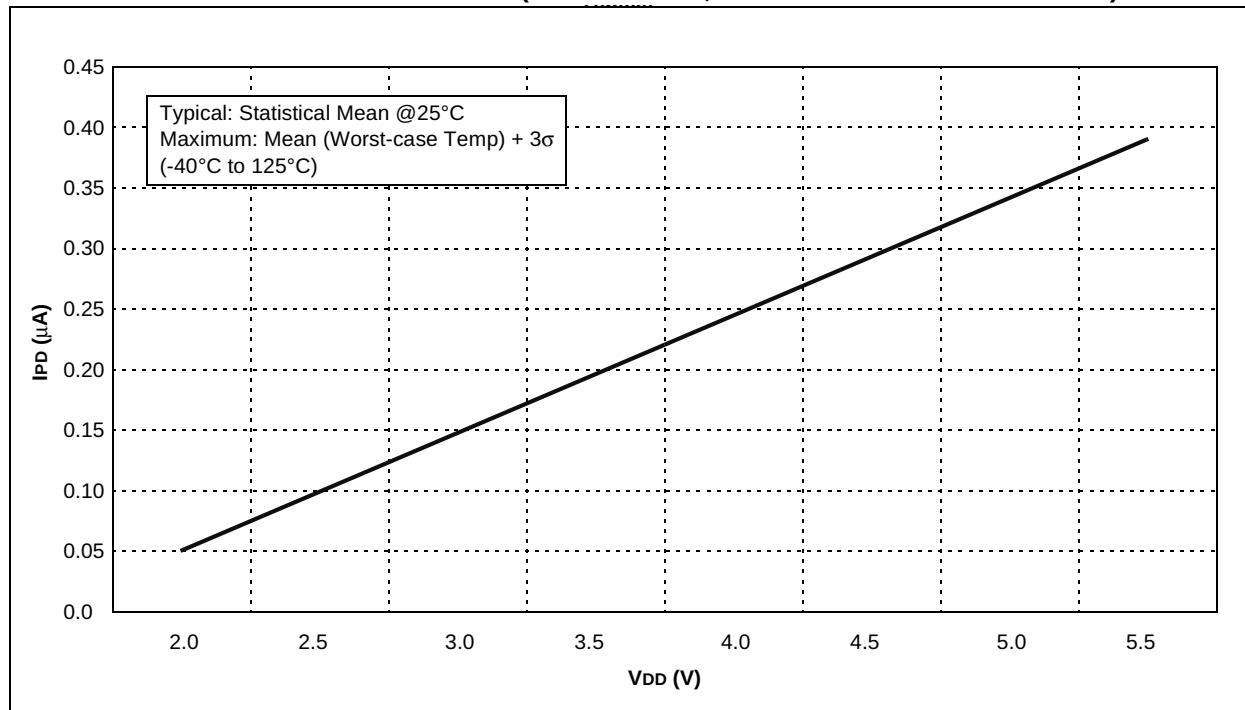


FIGURE 16-13: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)



PIC12F683

FIGURE 16-14: MAXIMUM IPD VS. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)

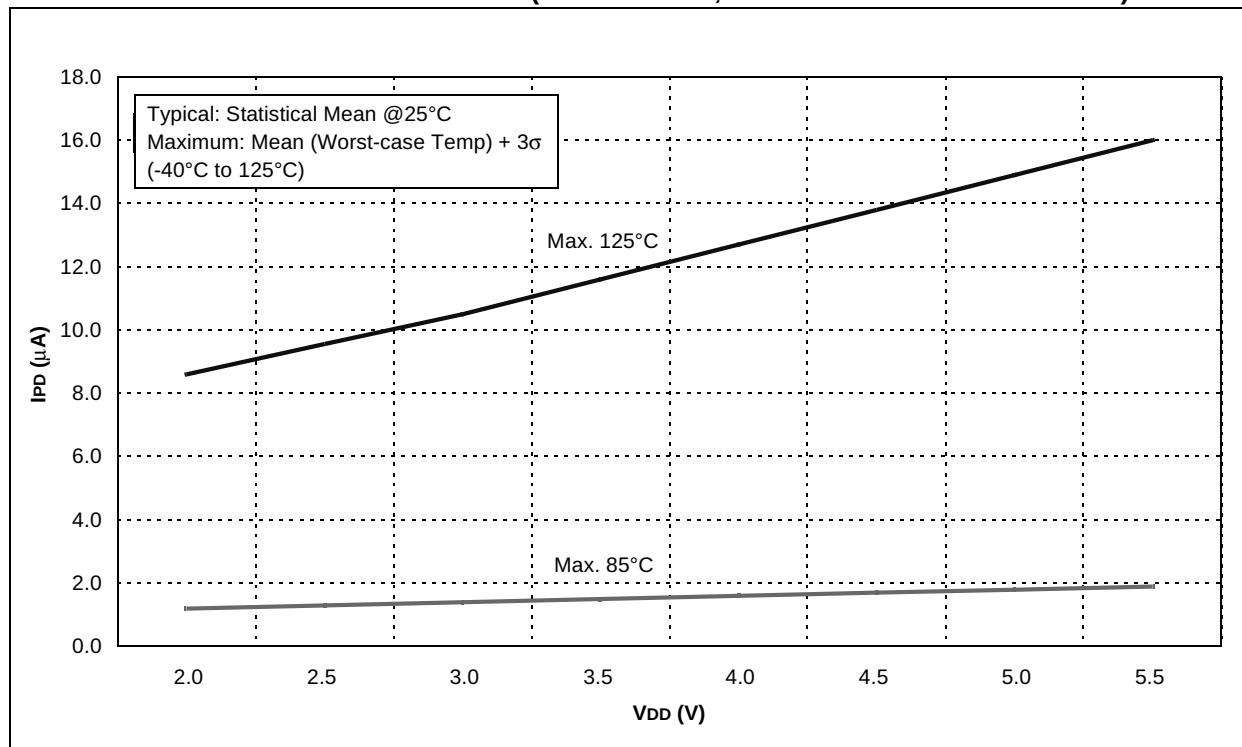


FIGURE 16-15: COMPARATOR IPD VS. VDD (BOTH COMPARATORS ENABLED)

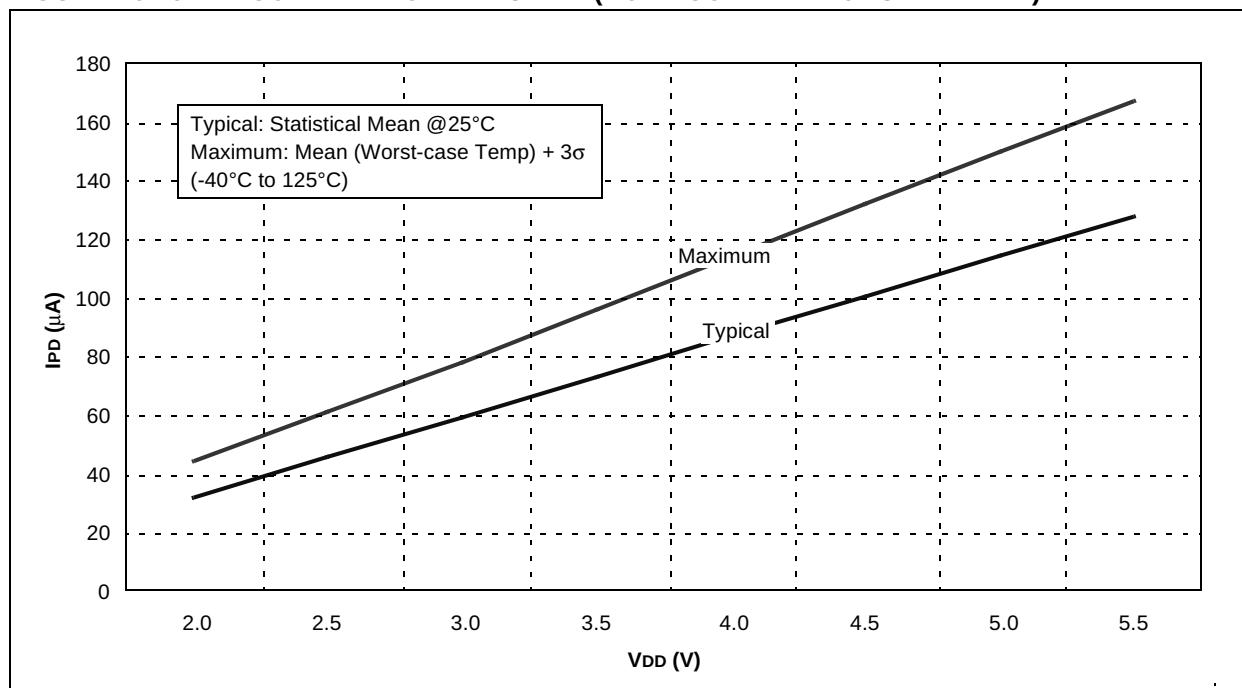
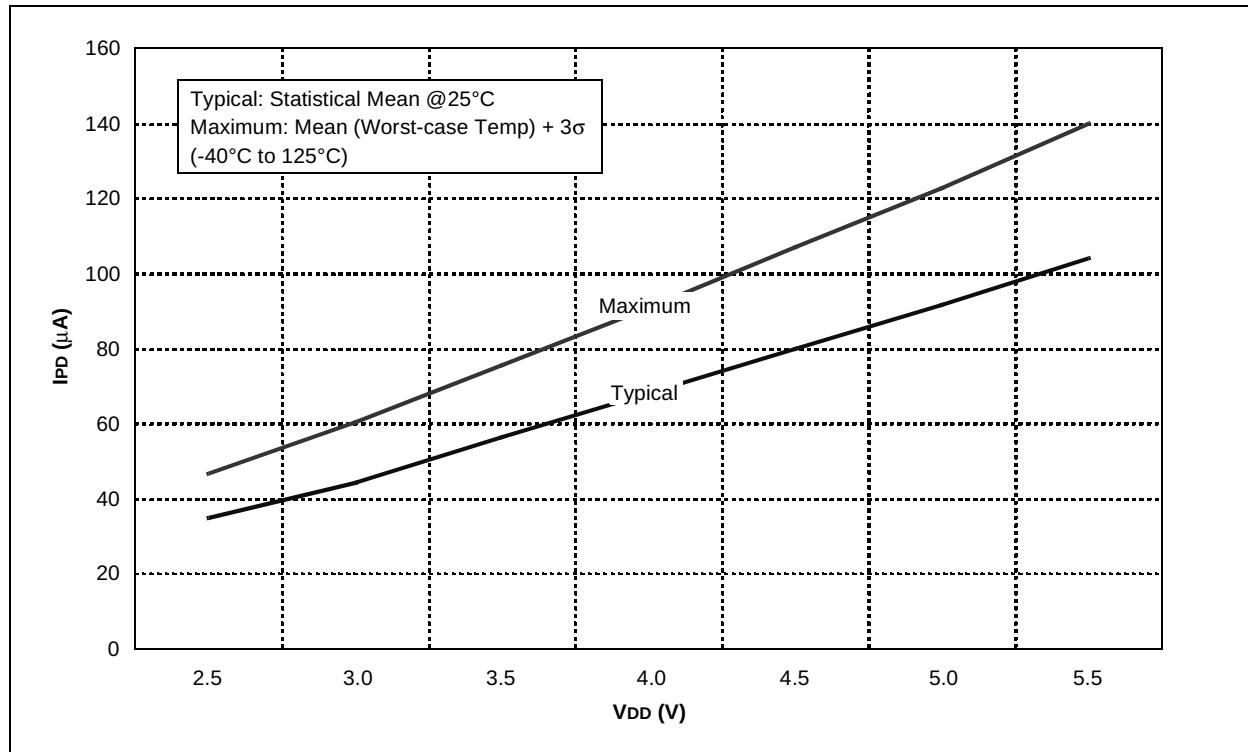
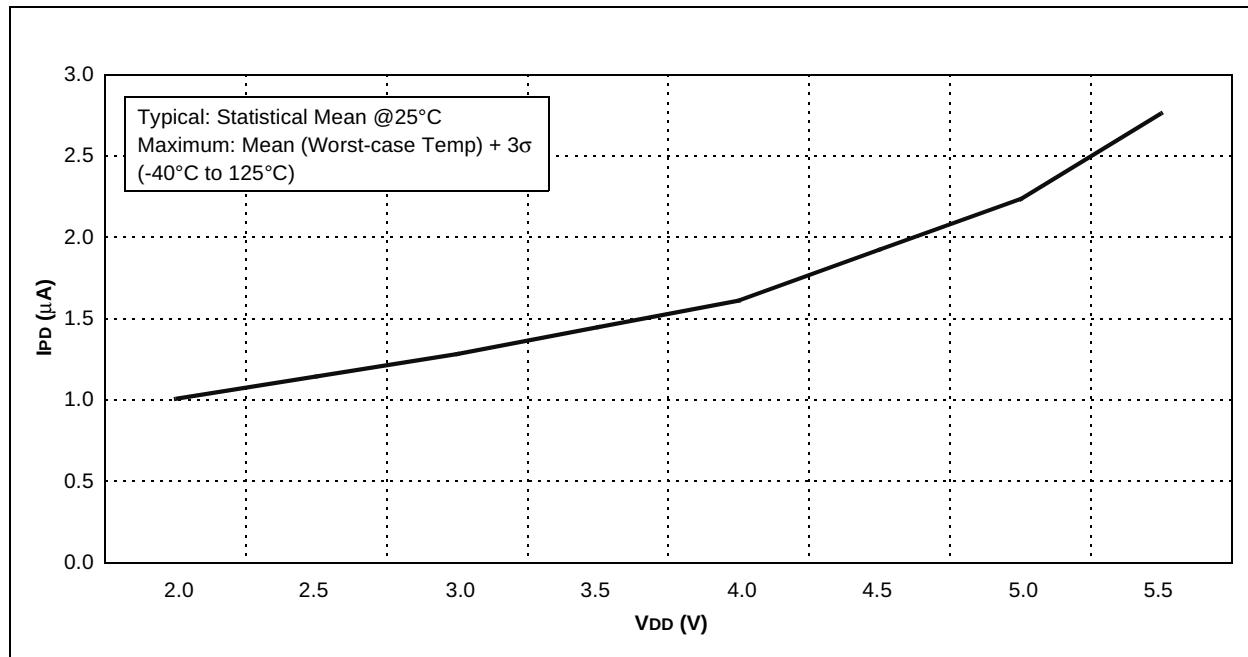


FIGURE 16-16: BOR IPD VS. VDD OVER TEMPERATURE**FIGURE 16-17: TYPICAL WDT IPD VS. VDD OVER TEMPERATURE**

PIC12F683

FIGURE 16-18: MAXIMUM WDT IPD VS. VDD OVER TEMPERATURE

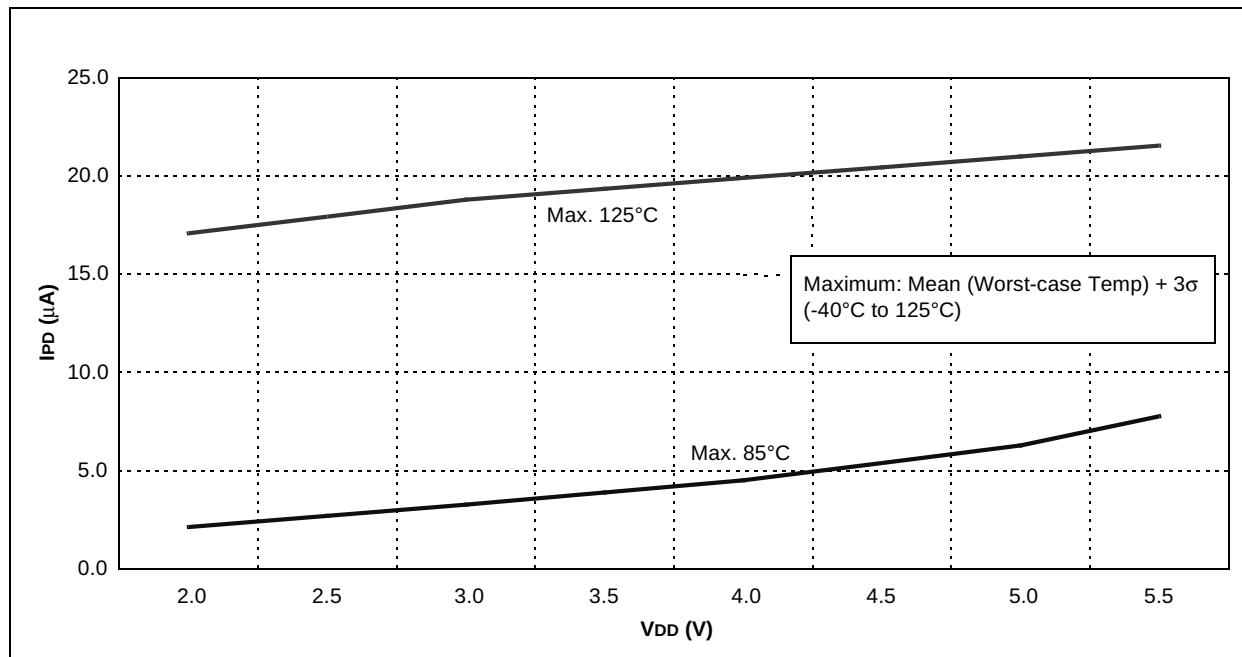


FIGURE 16-19: WDT PERIOD VS. VDD OVER TEMPERATURE

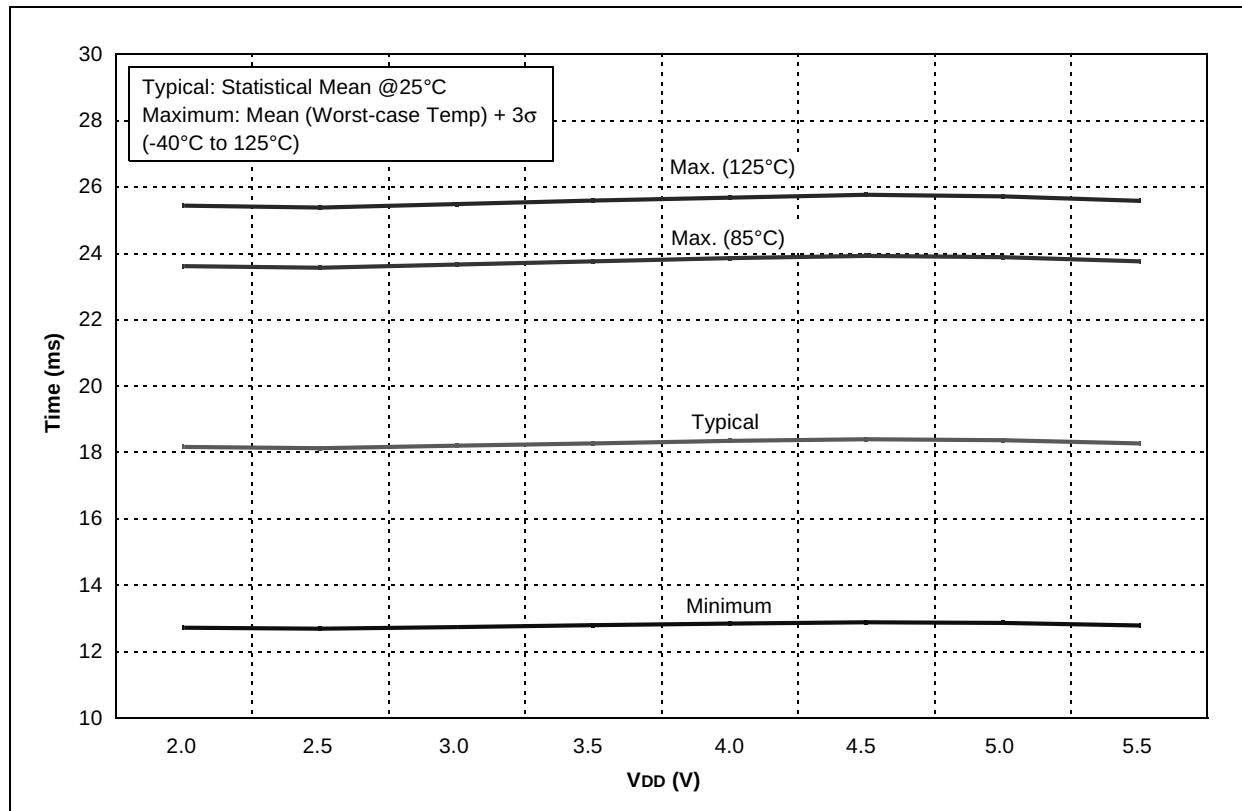


FIGURE 16-20: WDT PERIOD vs. TEMPERATURE OVER V_{DD} (5.0V)

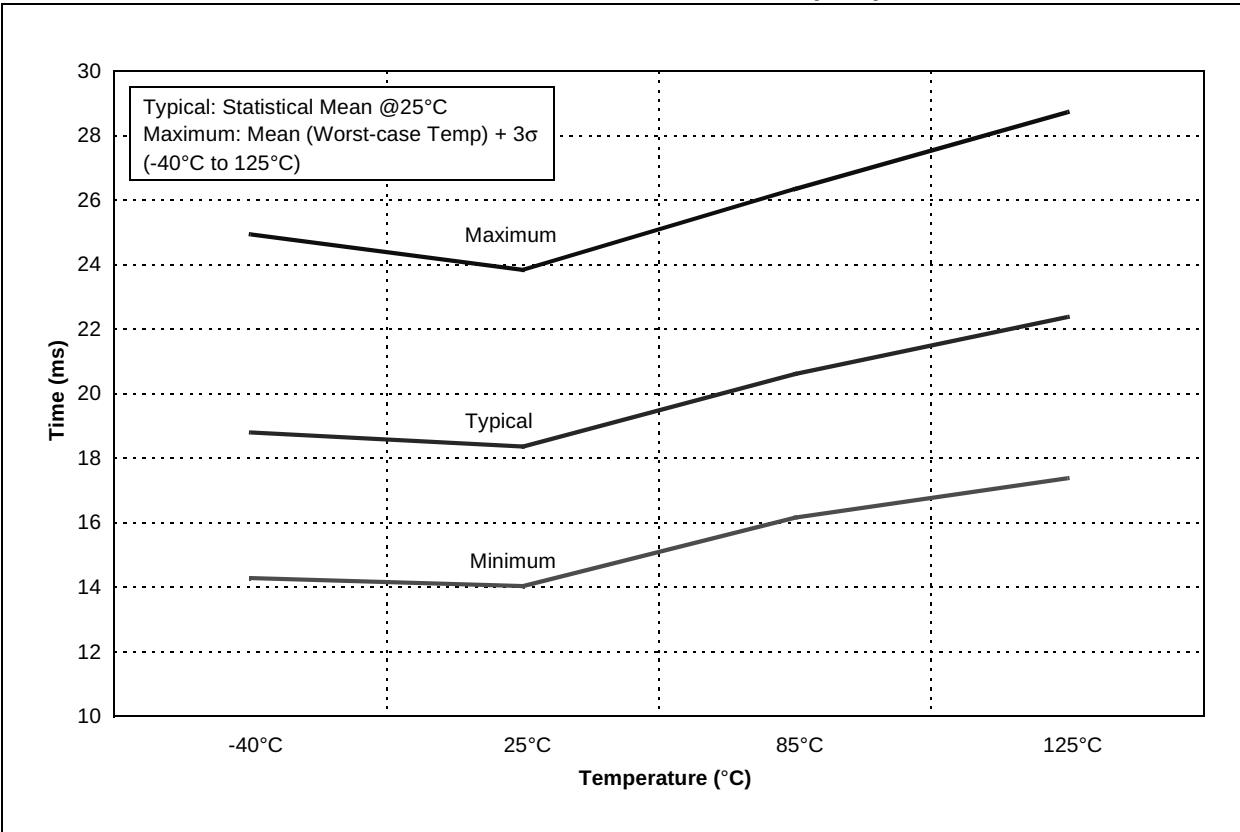
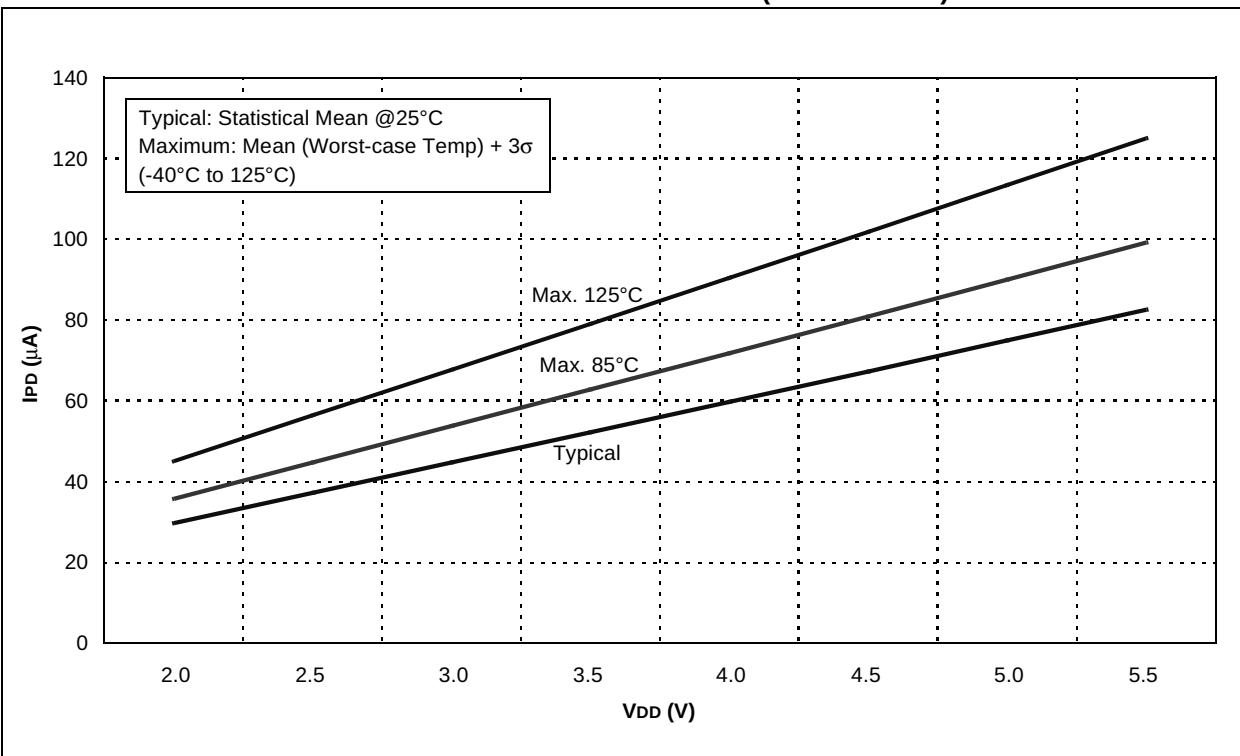


FIGURE 16-21: CVREF IPD VS. V_{DD} OVER TEMPERATURE (HIGH RANGE)



PIC12F683

FIGURE 16-22: CVREF IPD VS. VDD OVER TEMPERATURE (LOW RANGE)

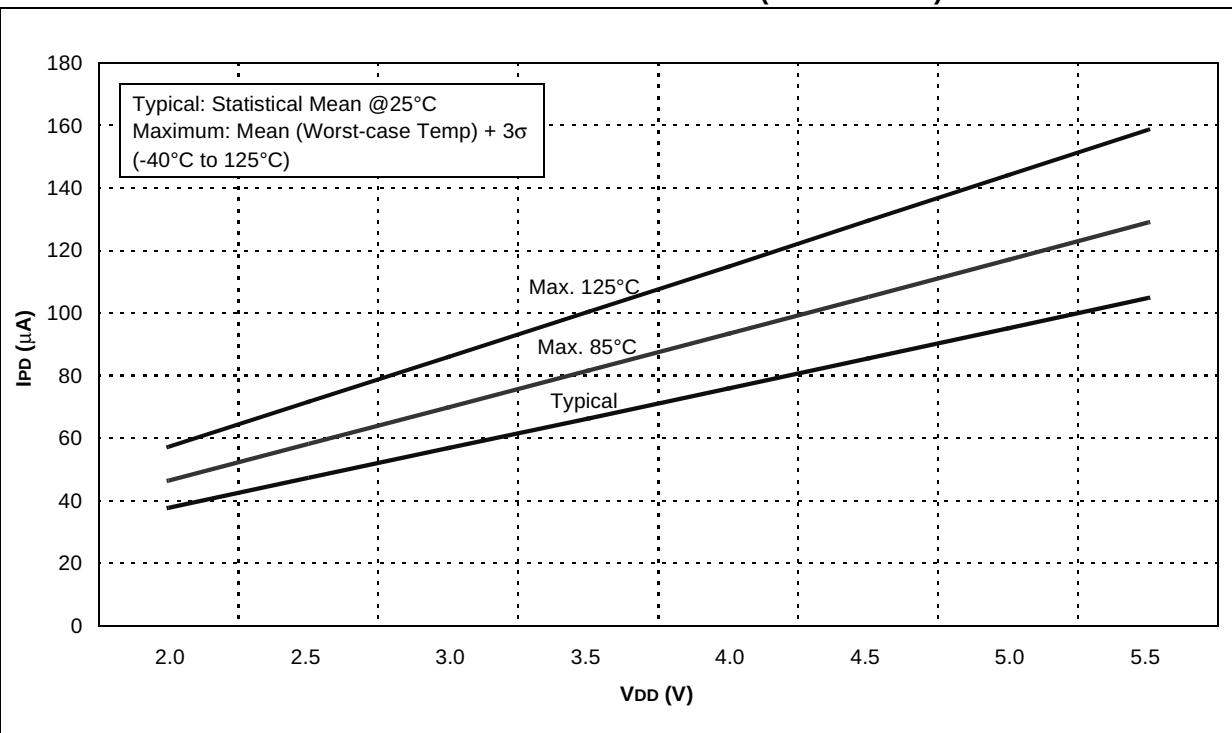


FIGURE 16-23: VOL VS. IOL OVER TEMPERATURE (VDD = 3.0V)

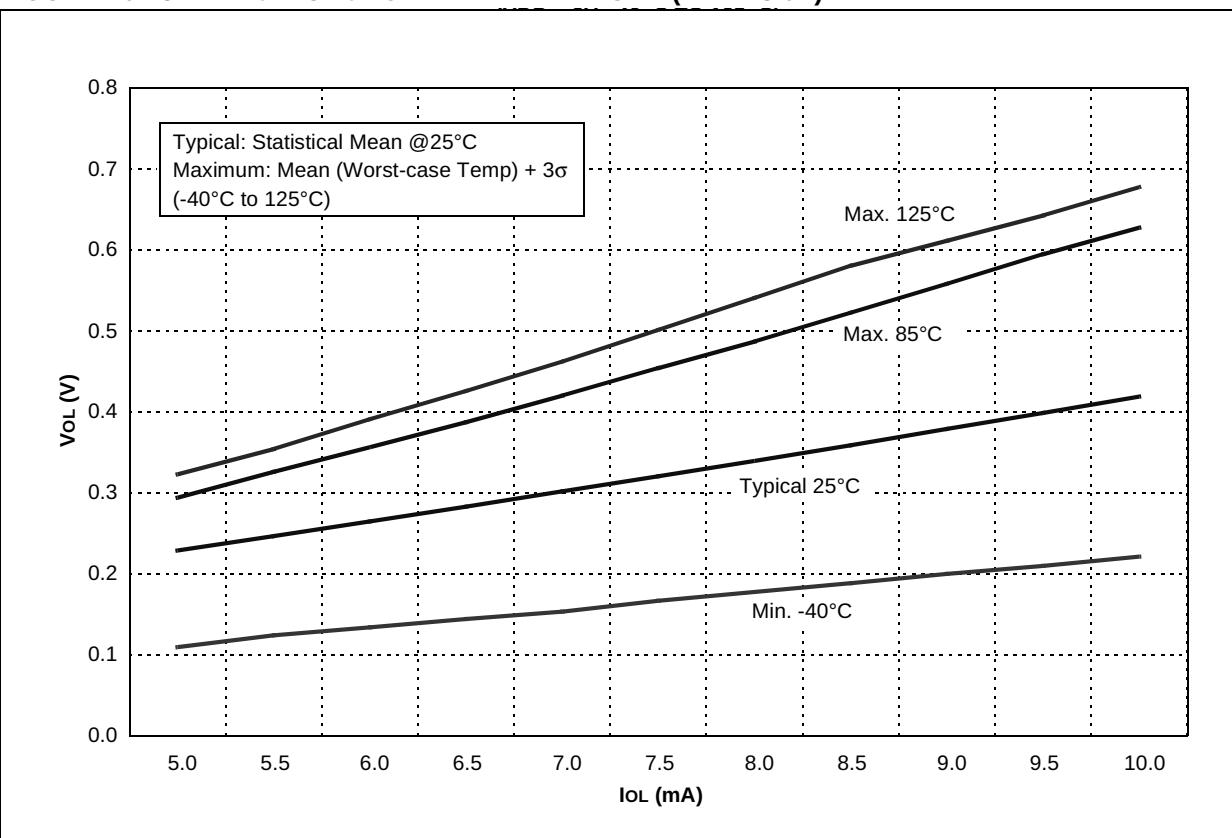


FIGURE 16-24: VOL vs. IO_L OVER TEMPERATURE (V_{DD} = 5.0V)

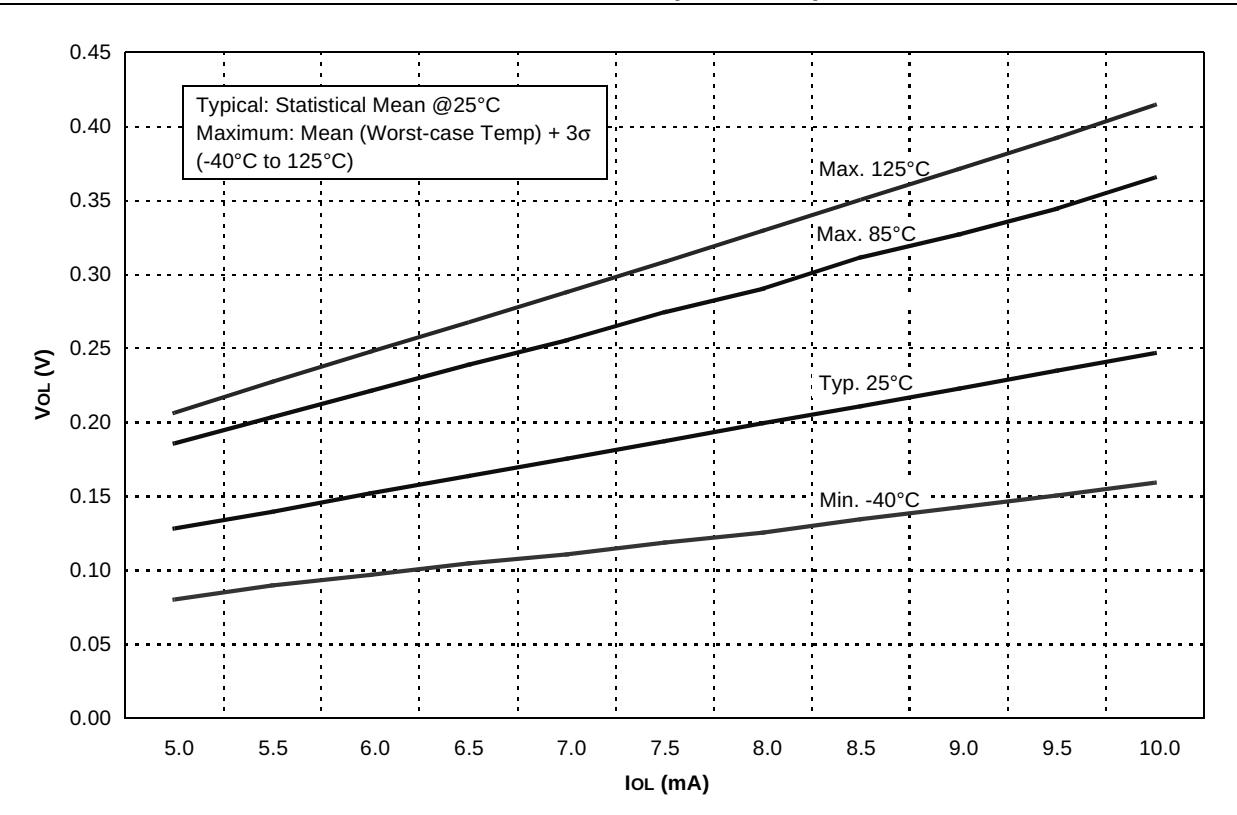
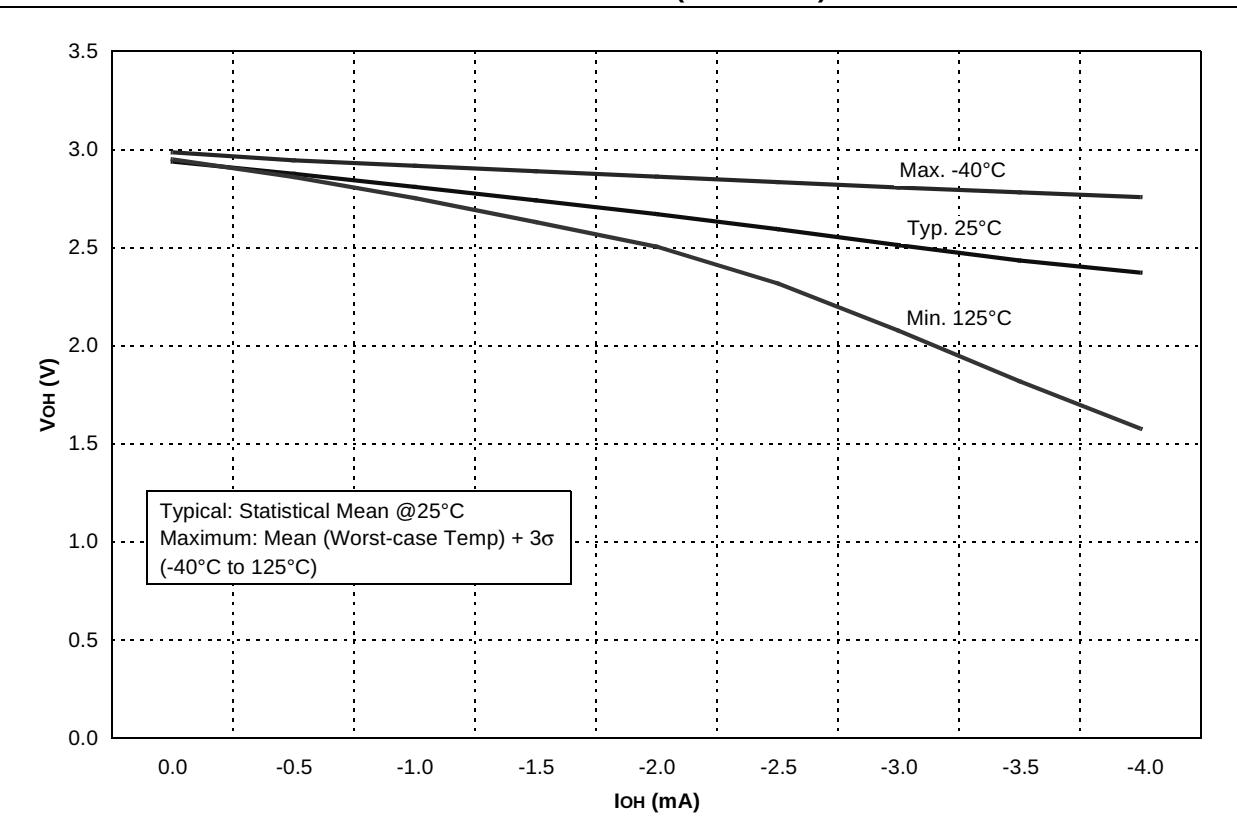


FIGURE 16-25: VOH vs. IO_H OVER TEMPERATURE (V_{DD} = 3.0V)



PIC12F683

FIGURE 16-26: V_{OH} vs. I_{OH} OVER TEMPERATURE ($V_{DD} = 5.0V$)

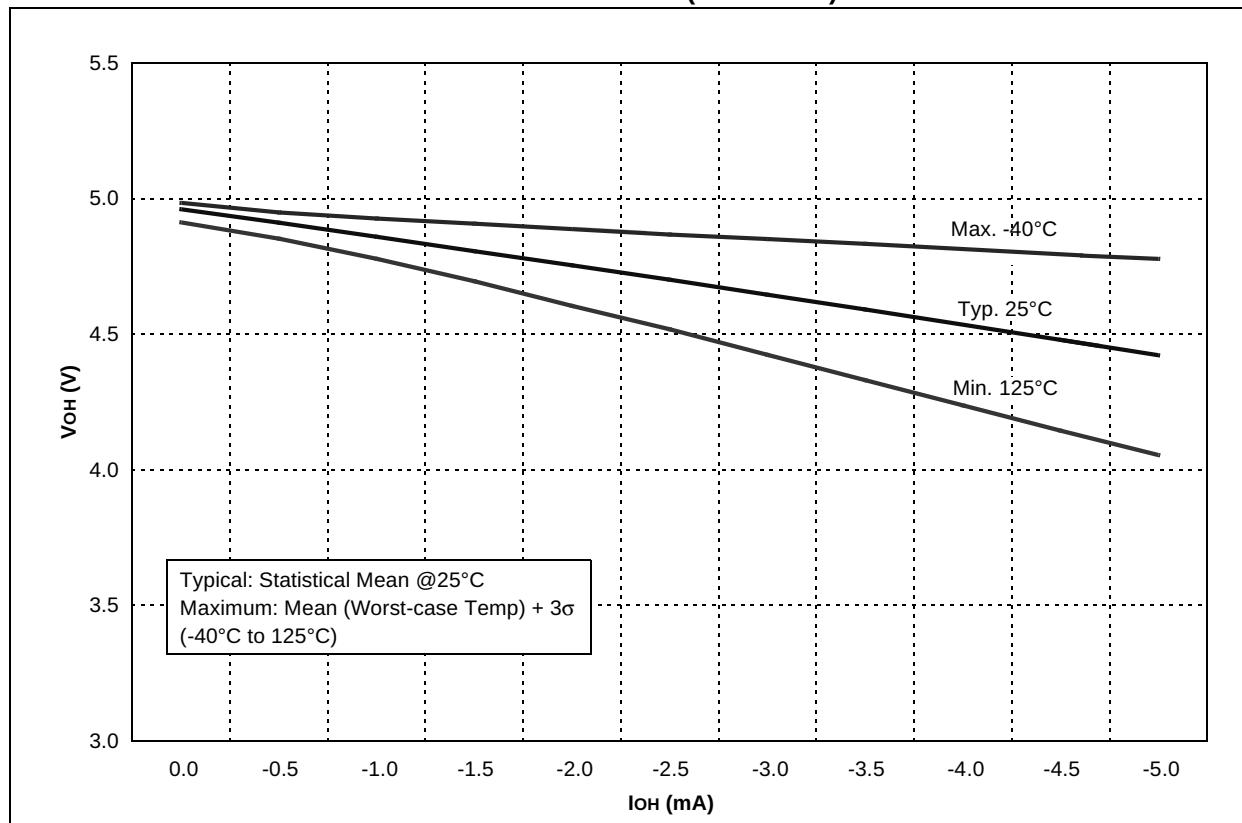


FIGURE 16-27: TTL INPUT THRESHOLD V_{IN} vs. V_{DD} OVER TEMPERATURE

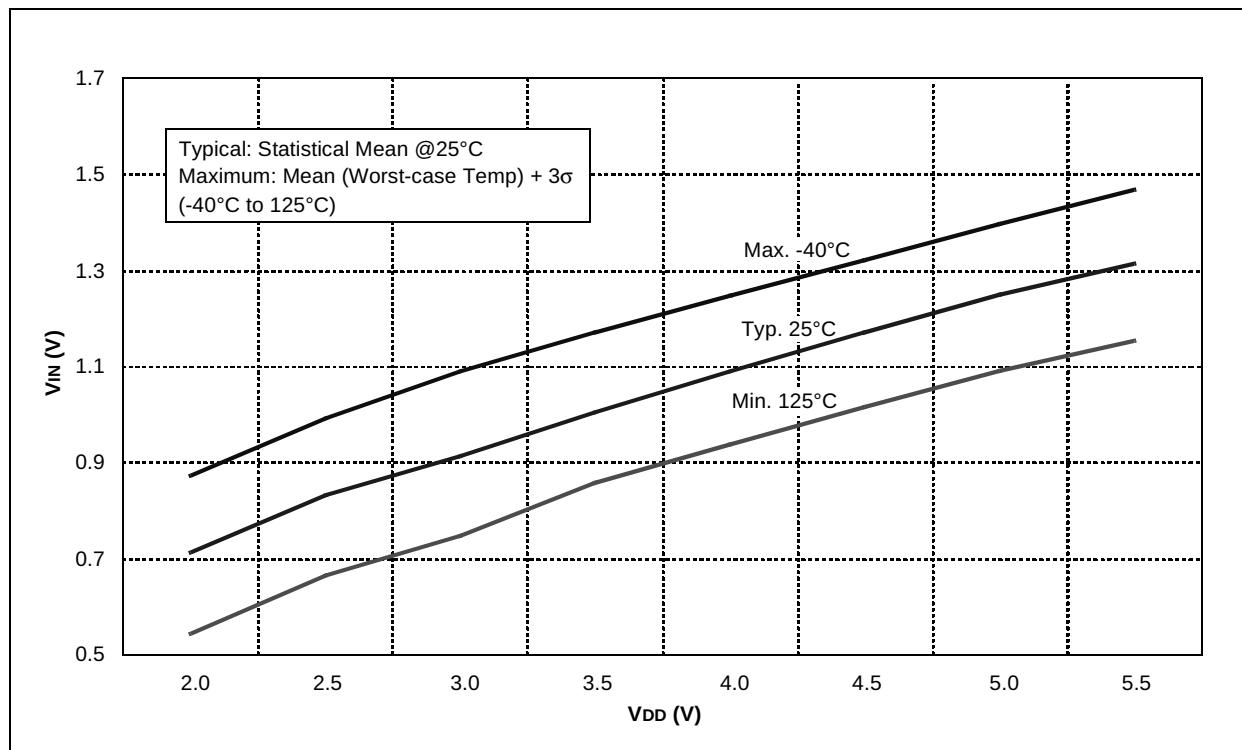


FIGURE 16-28: SCHMITT TRIGGER INPUT THRESHOLD V_{IN} VS. V_{DD} OVER TEMPERATURE

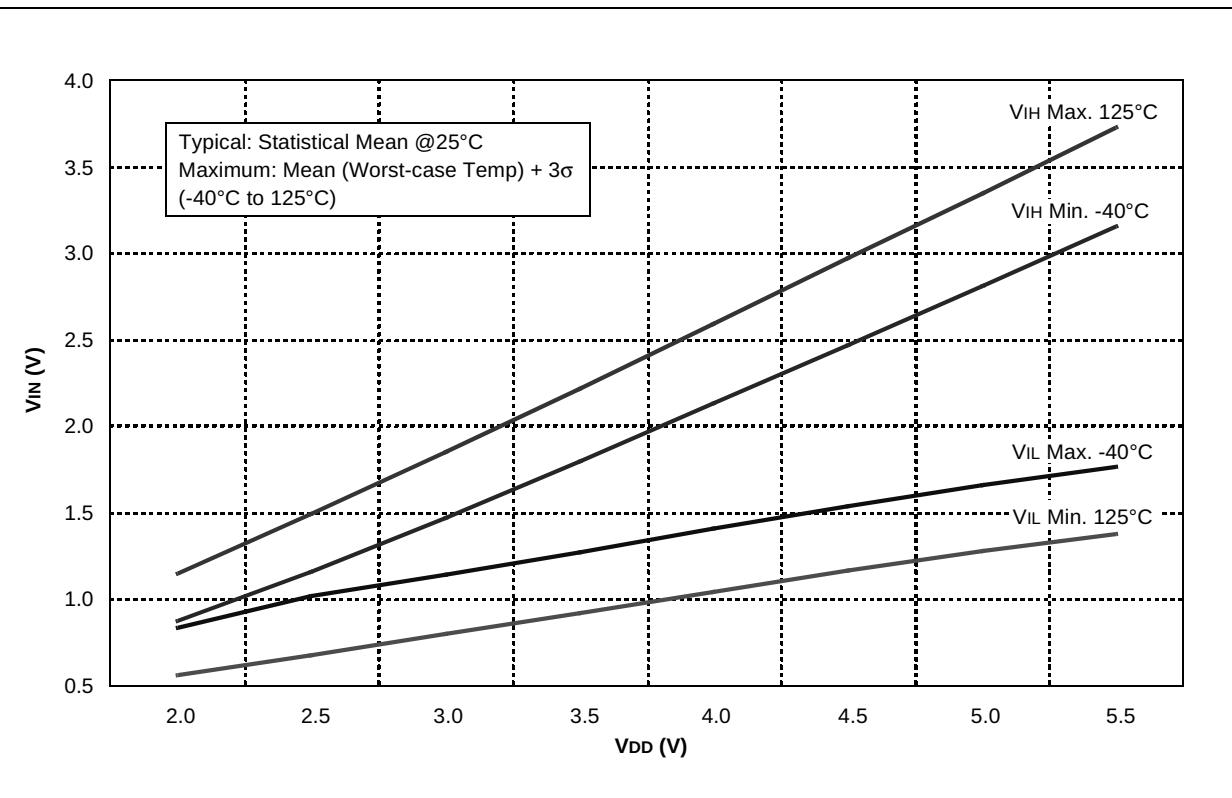
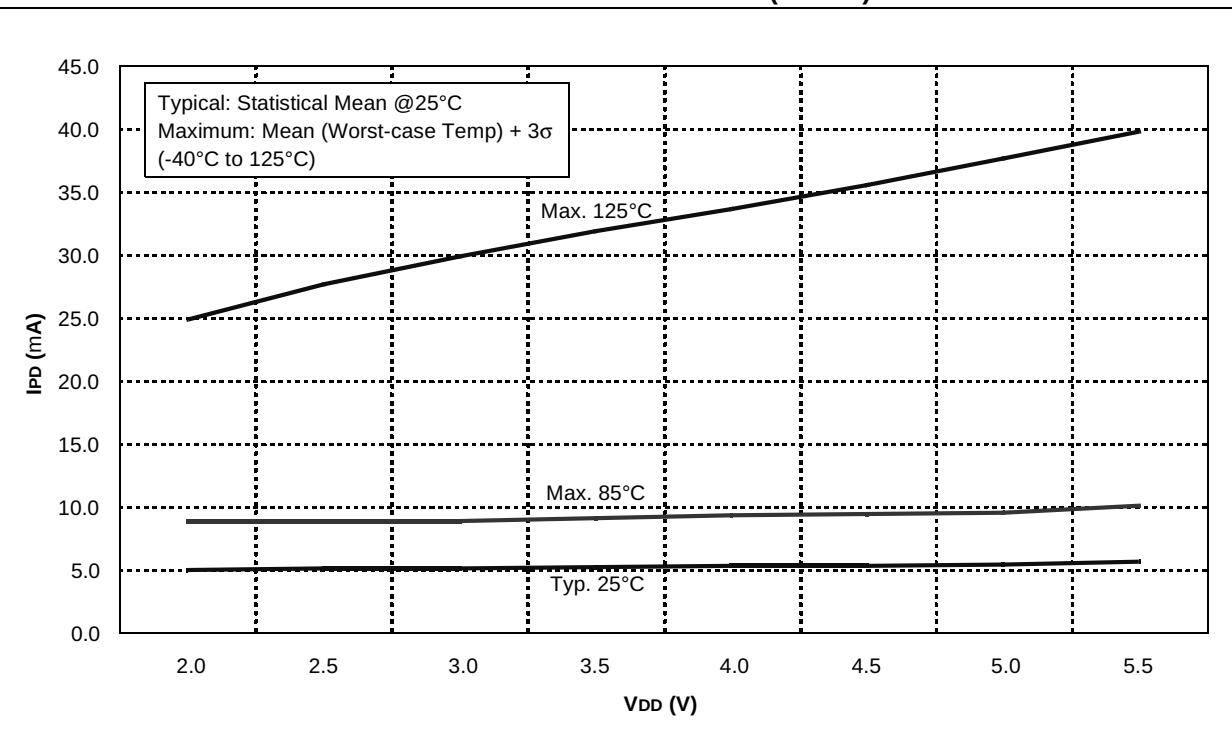


FIGURE 16-29: T1OSC IPD VS. V_{DD} OVER TEMPERATURE (32 kHz)



PIC12F683

FIGURE 16-30: COMPARATOR RESPONSE TIME (RISING EDGE)

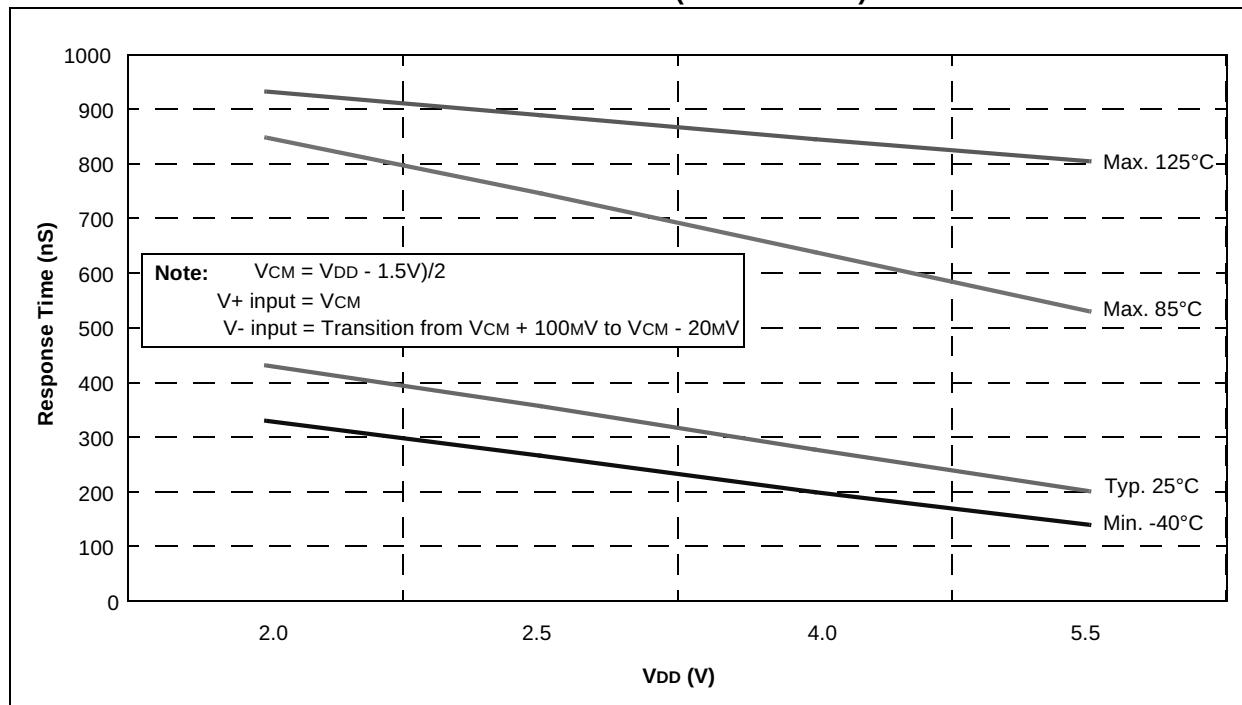


FIGURE 16-31: COMPARATOR RESPONSE TIME (FALLING EDGE)

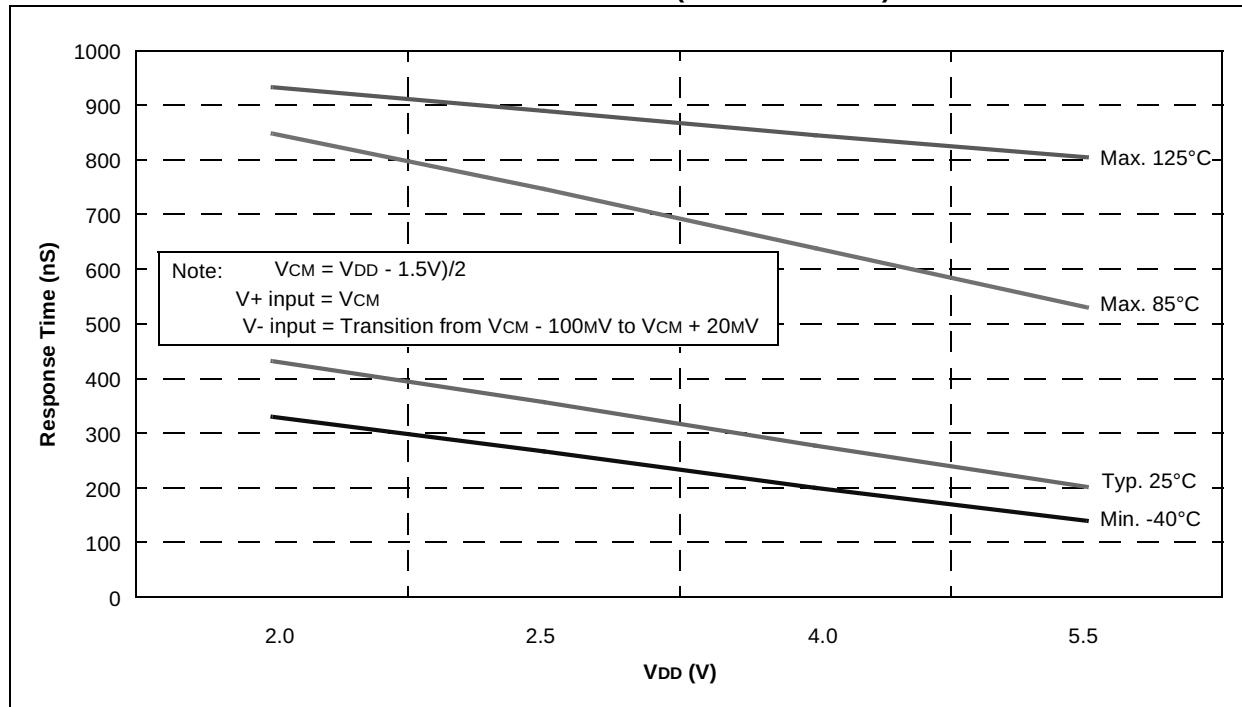


FIGURE 16-32: LFINTOSC FREQUENCY vs. VDD OVER TEMPERATURE (31 kHz)

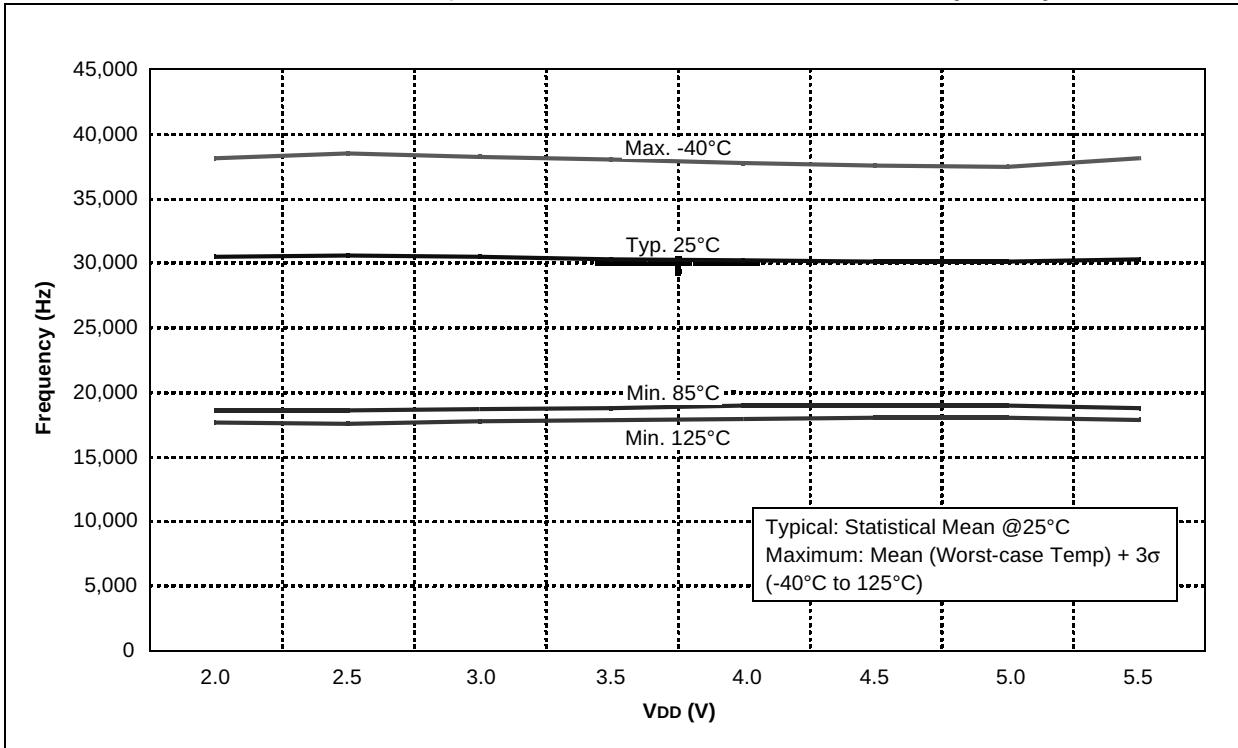
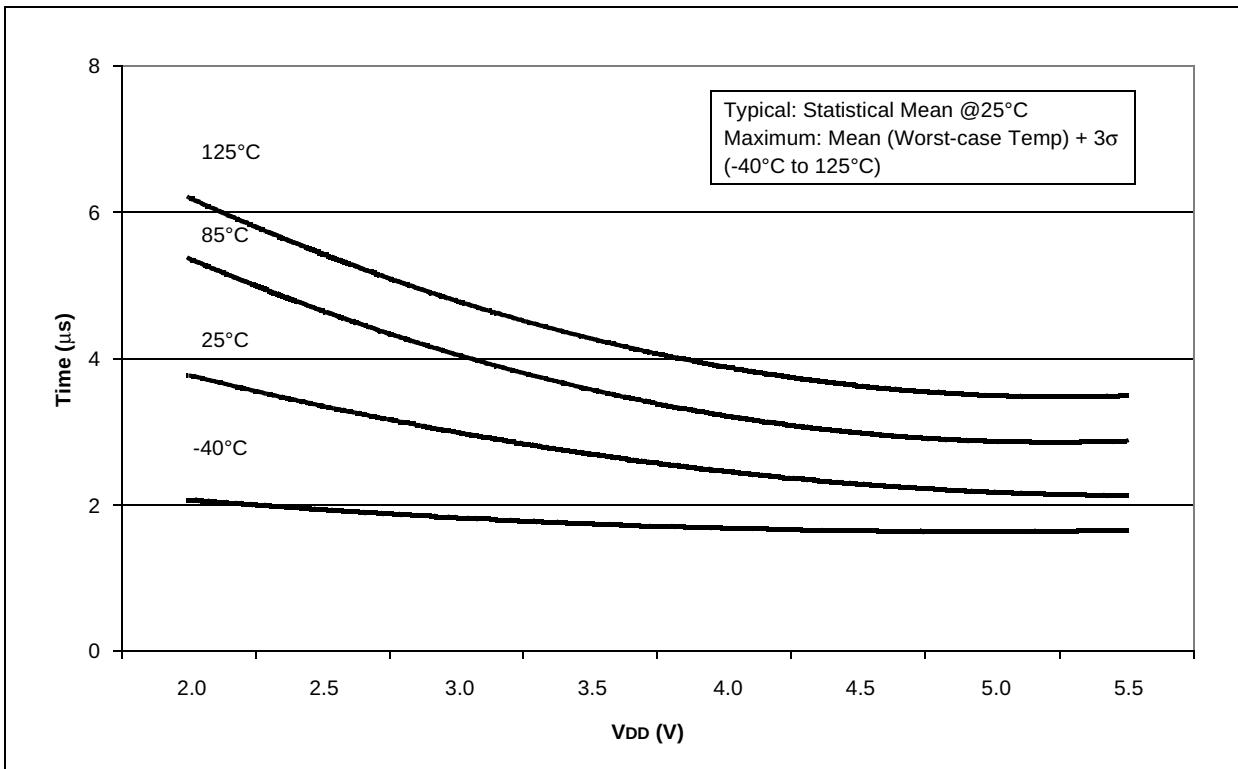


FIGURE 16-33: ADC CLOCK PERIOD vs. VDD OVER TEMPERATURE



PIC12F683

FIGURE 16-34: TYPICAL HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

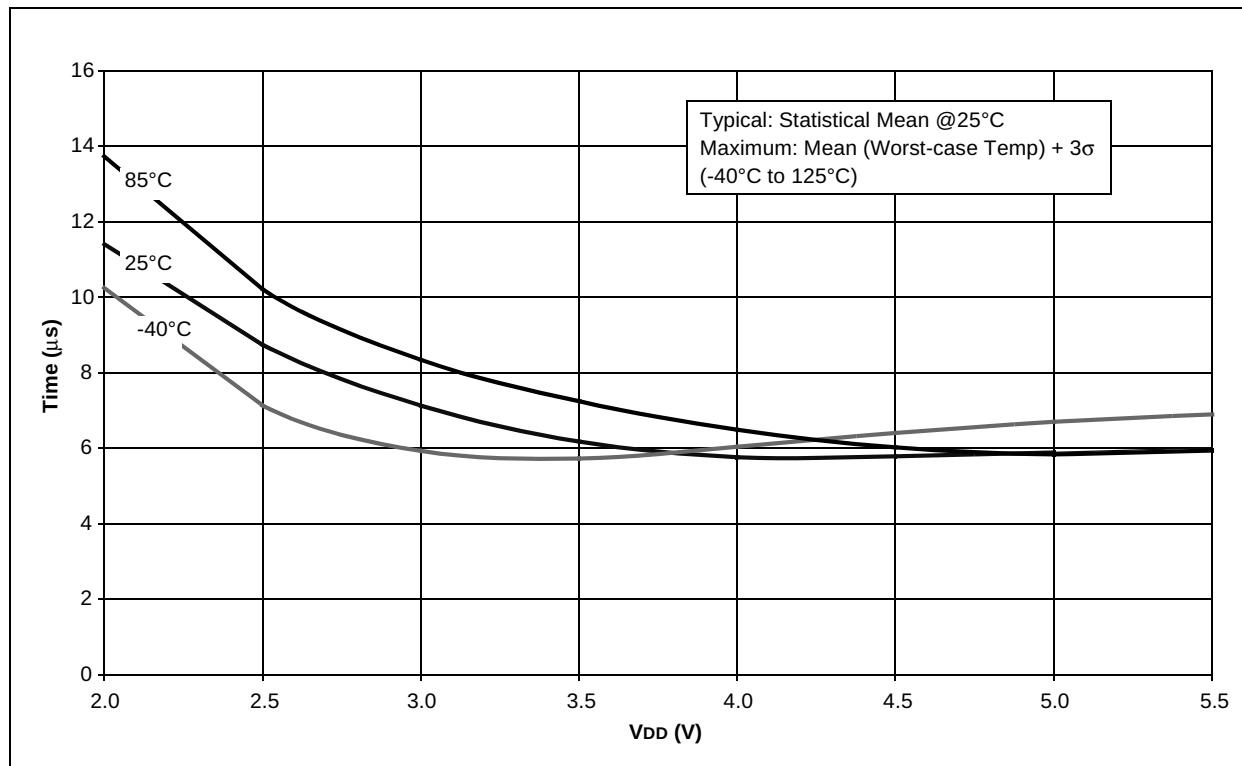


FIGURE 16-35: MAXIMUM HFINTOSC START-UP TIMES vs. VDD OVER TEMPERATURE

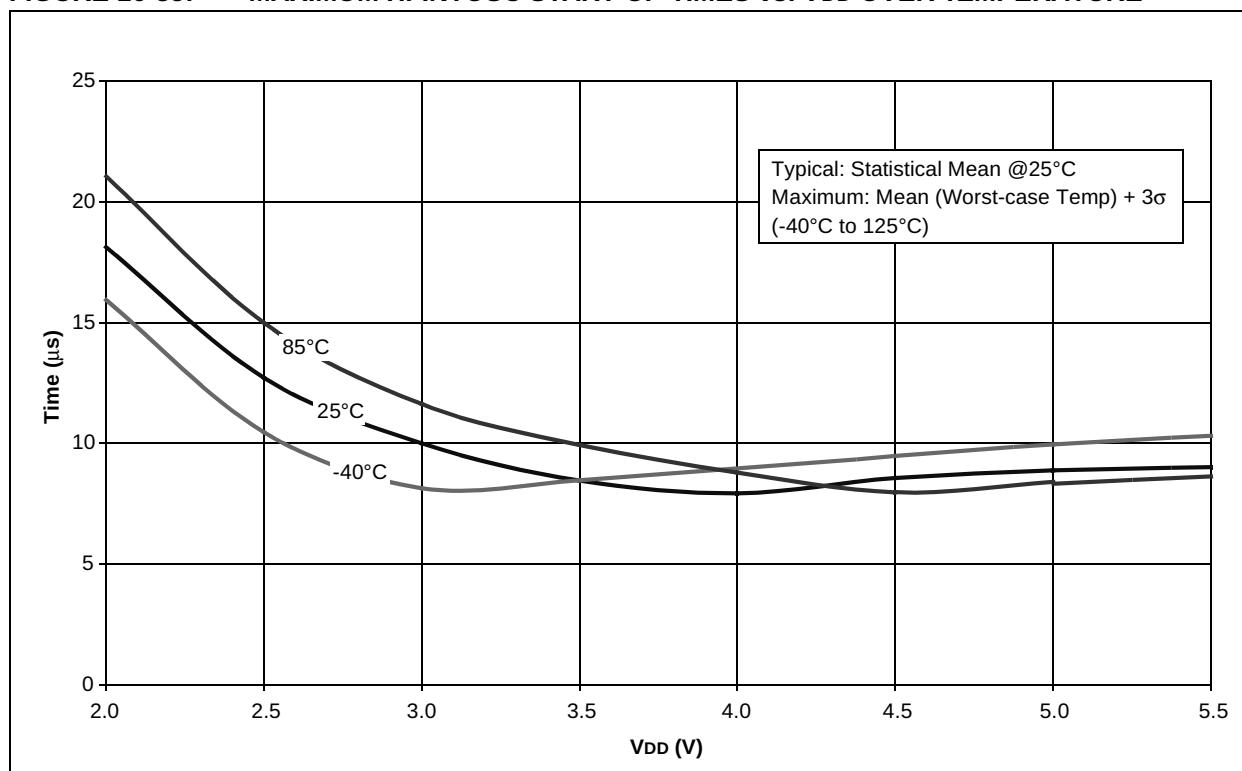
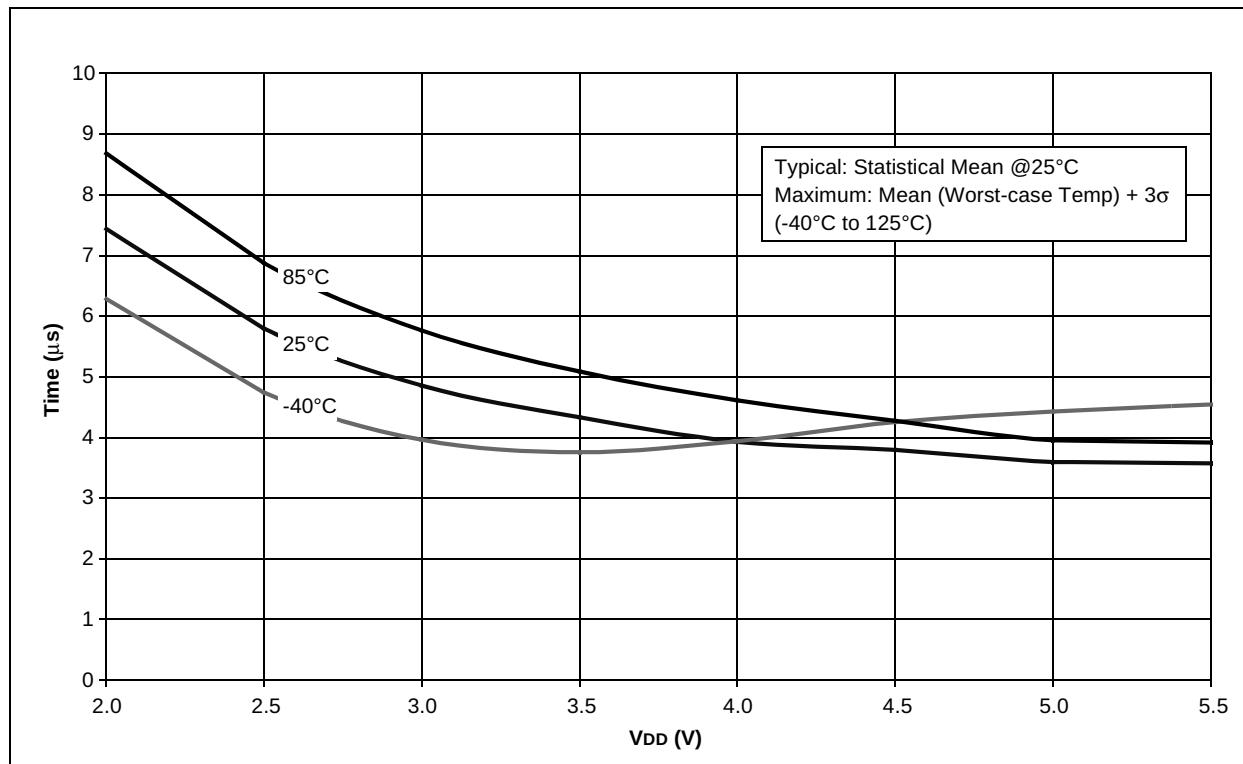
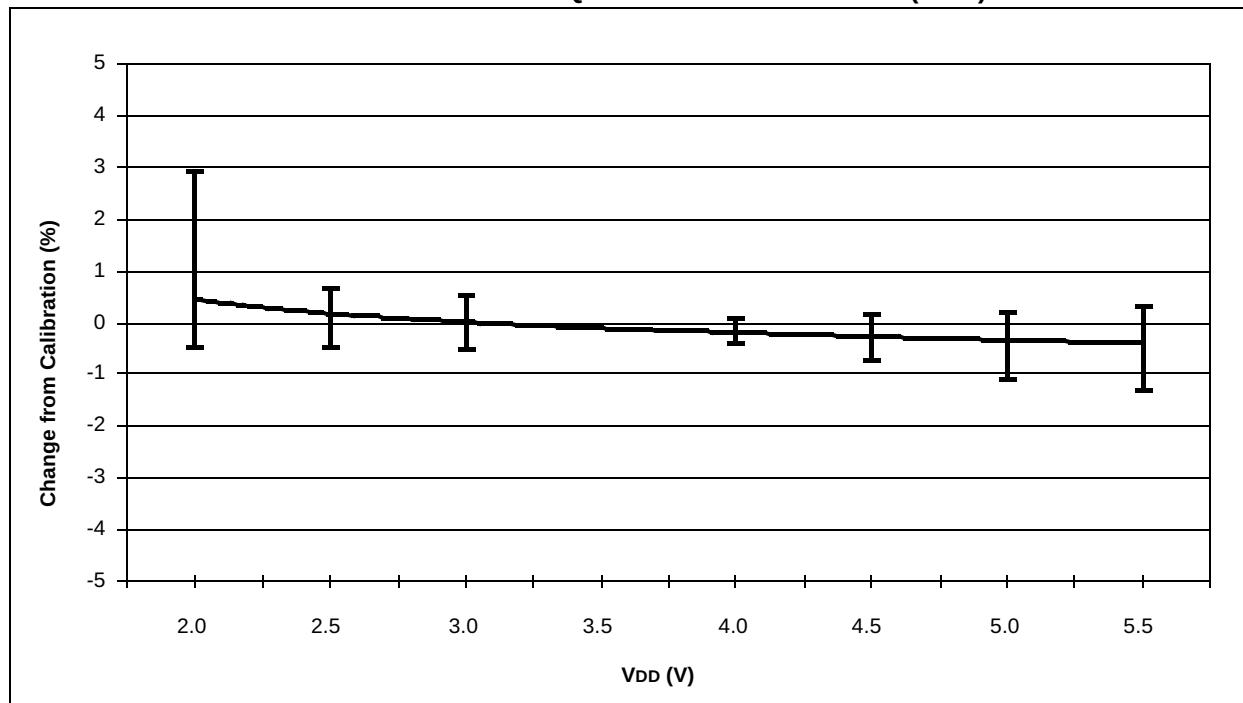


FIGURE 16-36: MINIMUM HFINTOSC START-UP TIMES vs. V_{DD} OVER TEMPERATURE**FIGURE 16-37: TYPICAL HFINTOSC FREQUENCY CHANGE vs. V_{DD} (25°C)**

PIC12F683

FIGURE 16-38: TYPICAL HFINTOSC FREQUENCY CHANGE OVER DEVICE V_{DD} (85°C)

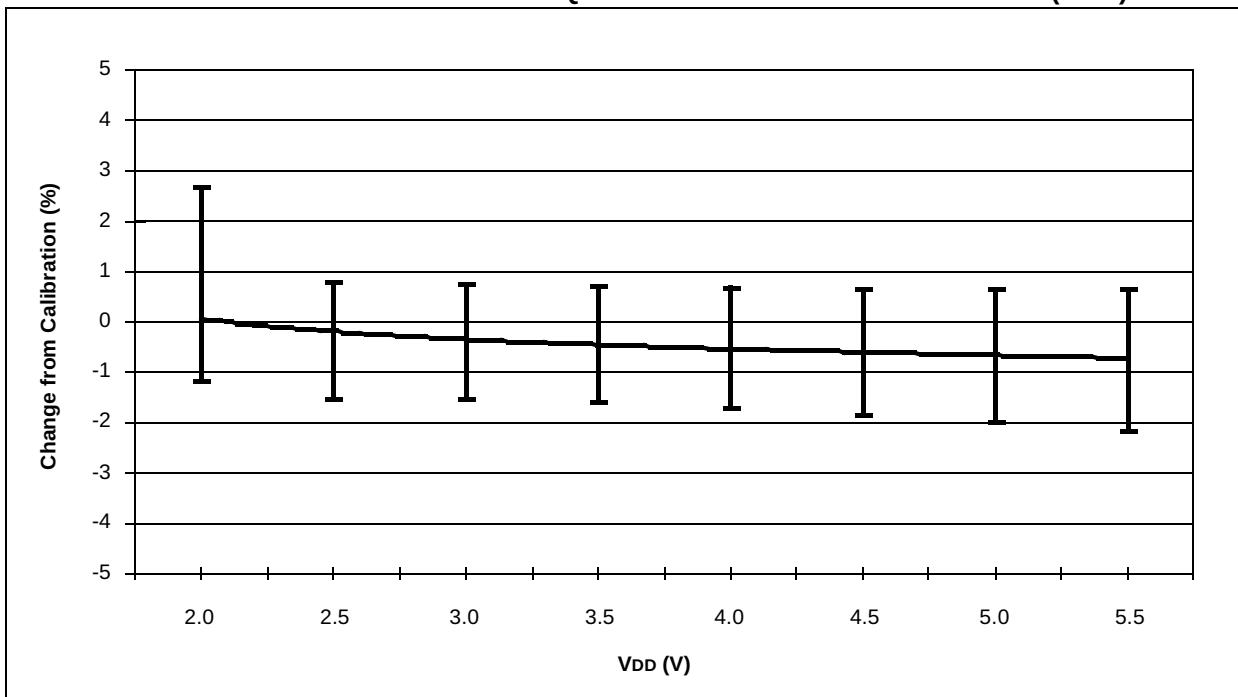


FIGURE 16-39: TYPICAL HFINTOSC FREQUENCY CHANGE vs. V_{DD} (125°C)

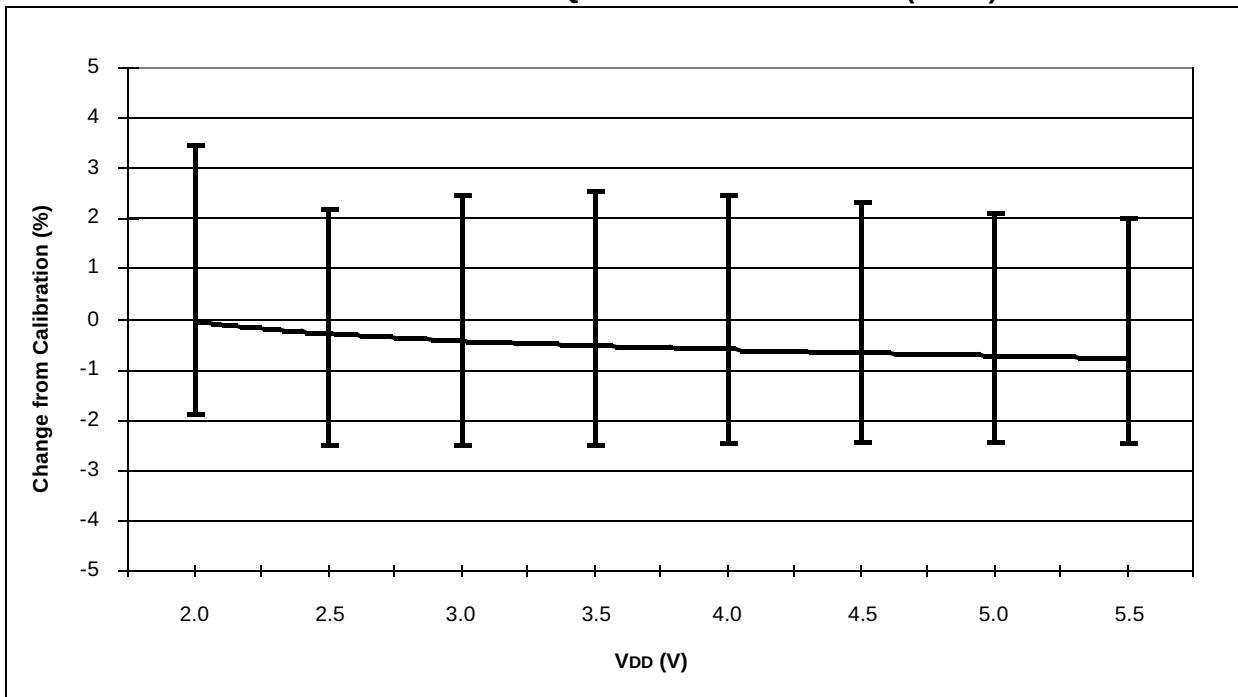
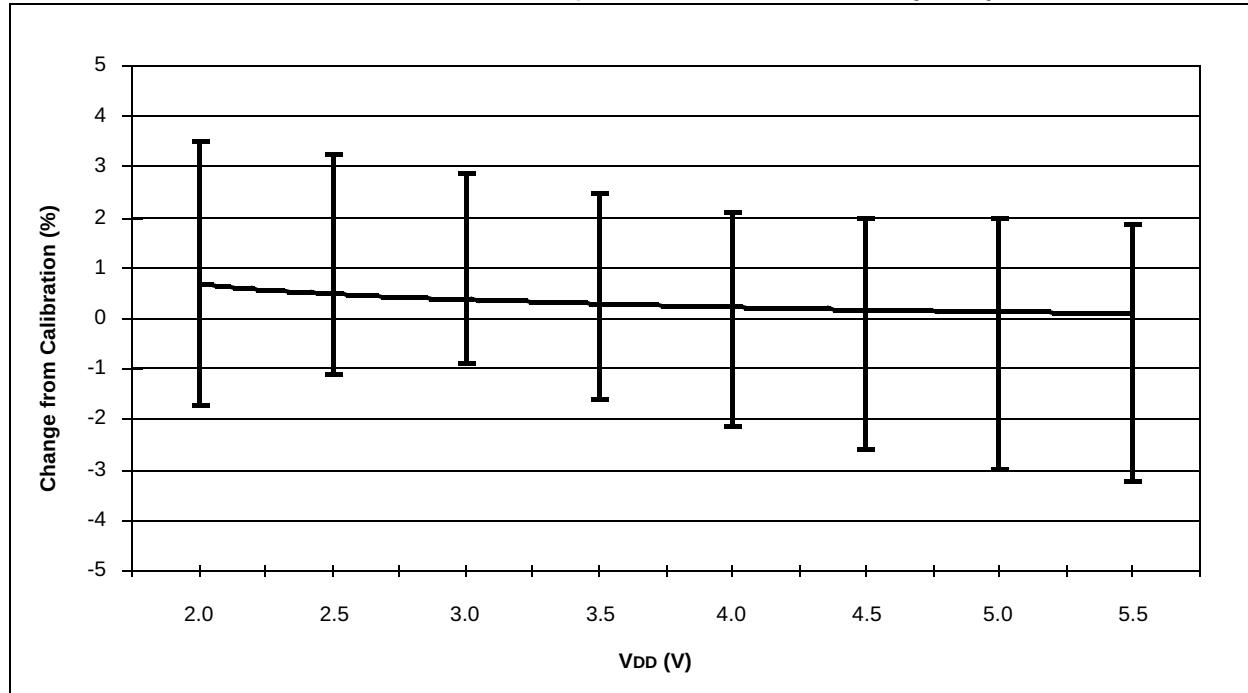


FIGURE 16-40: TYPICAL HFINTOSC FREQUENCY CHANGE vs. VDD (-40°C)

PIC12F683

NOTES:

17.0 PACKAGING INFORMATION

17.1 Package Marking Information

8-Lead PDIP



Example



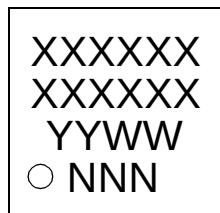
8-Lead SOIC (3.90 mm)



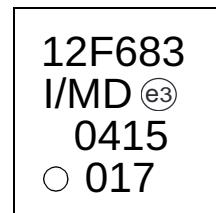
Example



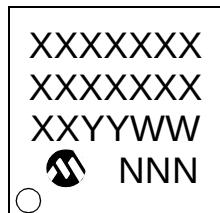
8-Lead DFN (4x4x0.9 mm)



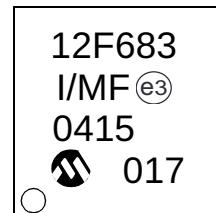
Example



8-Lead DFN-S (6x5 mm)



Example



Legend: XX...X Customer-specific information

Y Year code (last digit of calendar year)

YY Year code (last 2 digits of calendar year)

WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

(e3) Pb-free JEDEC designator for Matte Tin (Sn)

* This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

- * Standard PIC® device marking consists of Microchip part number, year code, week code and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

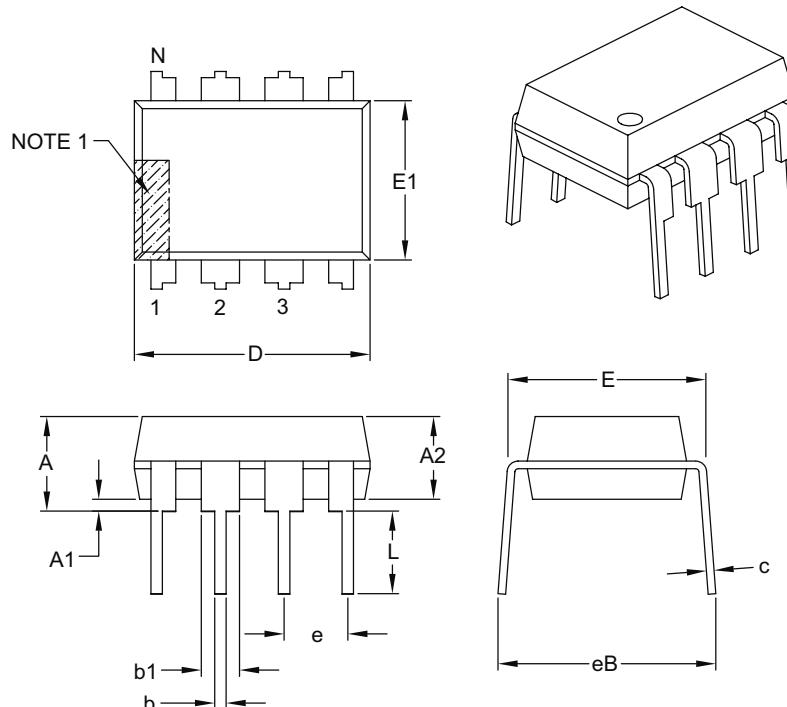
PIC12F683

17.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-Line (P or PA) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

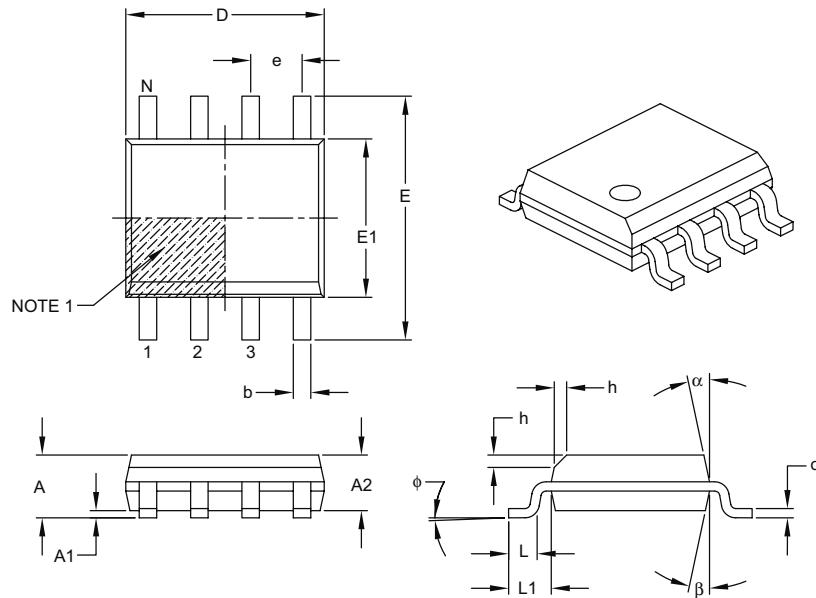
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN or OA) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	—	—	1.75
Molded Package Thickness	A2	1.25	—	—
Standoff §	A1	0.10	—	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	—	0.50
Foot Length	L	0.40	—	1.27
Footprint	L1	1.04 REF		
Foot Angle	phi	0°	—	8°
Lead Thickness	c	0.17	—	0.25
Lead Width	b	0.31	—	0.51
Mold Draft Angle Top	alpha	5°	—	15°
Mold Draft Angle Bottom	beta	5°	—	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

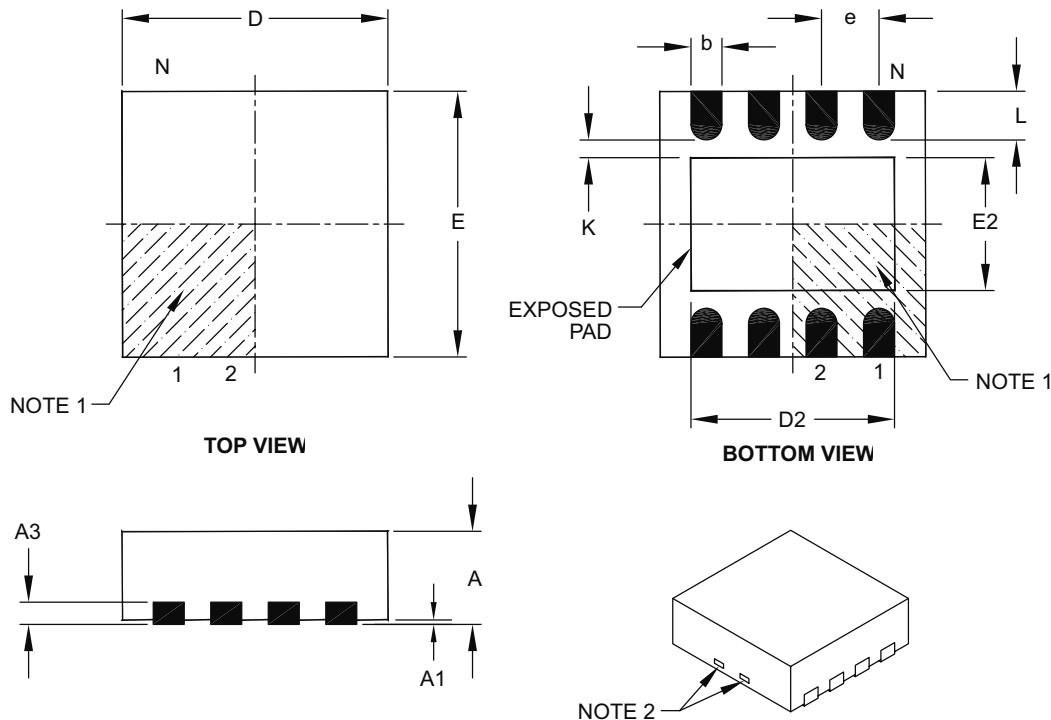
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

PIC12F683

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N			8	
Pitch	e			0.80 BSC	
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Length	D		4.00 BSC		
Exposed Pad Width	E2		0.00	2.20	2.80
Overall Width	E		4.00 BSC		
Exposed Pad Length	D2		0.00	3.00	3.60
Contact Width	b		0.25	0.30	0.35
Contact Length	L		0.30	0.55	0.65
Contact-to-Exposed Pad	K		0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package may have one or more exposed tie bars at ends.

3. Package is saw singulated.

4. Dimensioning and tolerancing per ASME Y14.5M.

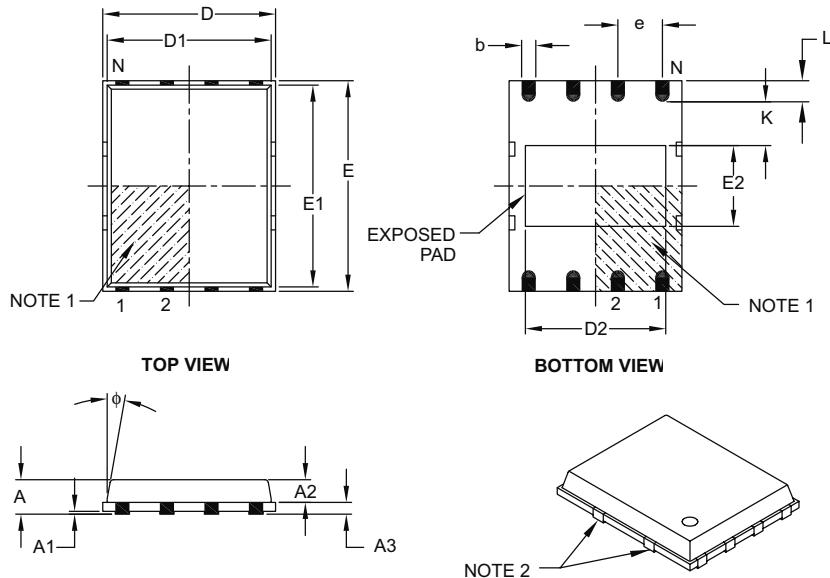
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131C

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	—	0.85	1.00
Molded Package Thickness	A2	—	0.65	0.80
Standoff	A1	0.00	0.01	0.05
Base Thickness	A3		0.20 REF	
Overall Length	D		4.92 BSC	
Molded Package Length	D1		4.67 BSC	
Exposed Pad Length	D2	3.85	4.00	4.15
Overall Width	E		5.99 BSC	
Molded Package Width	E1		5.74 BSC	
Exposed Pad Width	E2	2.16	2.31	2.46
Contact Width	b	0.35	0.40	0.47
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	—	—
Model Draft Angle Top	φ	—	—	12°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

PIC12F683

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Rewrites of the Oscillator and Special Features of the CPU sections. General corrections to Figures and formatting.

Revision C

Revisions throughout document. Incorporated Golden Chapters.

Revision D

Replaced Package Drawings; Revised Product ID Section (SN package to 3.90 mm); Replaced PICmicro with PIC; Replaced Dev Tool Section.

APPENDIX B: MIGRATING FROM OTHER PIC® DEVICES

This discusses some of the issues in migrating from other PIC devices to the PIC12F683 device.

B.1 PIC16F676 to PIC12F683

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC12F683
Max Operating Speed	20 MHz	20 MHz
Max Program Memory (Words)	1024	2048
SRAM (bytes)	64	128
A/D Resolution	10-bit	10-bit
Data EEPROM (Bytes)	128	256
Timers (8/16-bit)	1/1	2/1
Oscillator Modes	8	8
Brown-out Reset	Y	Y
Internal Pull-ups	RA0/1/2/4/5	GP0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	GP0/1/2/3/4/5
Comparator	1	1
ECCP	N	N
Ultra Low-Power Wake-Up	N	Y
Extended WDT	N	Y
Software Control Option of WDT/BOR	N	Y
INTOSC Frequencies	4 MHz	32 kHz- 8 MHz
Clock Switching	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

PIC12F683

NOTES:

INDEX

A

A/D

Specifications.....	133, 134
Absolute Maximum Ratings	115
AC Characteristics	
Industrial and Extended	125
Load Conditions	124
ADC	61
Acquisition Requirements	67
Associated registers.....	69
Block Diagram.....	61
Calculating Acquisition Time	67
Channel Selection	61
Configuration.....	61
Configuring Interrupt	64
Conversion Clock.....	62
Conversion Procedure	64
GPIO Configuration.....	61
Internal Sampling Switch (Rss) IMPEDANCE	67
Interrupts.....	63
Operation	63
Operation During Sleep	64
Reference Voltage (VREF).....	62
Result Formatting.....	63
Source Impedance.....	67
Special Event Trigger.....	64
Starting an A/D Conversion	63
ADCON0 Register.....	65
ADRESH Register (ADFM = 0).....	66
ADRESH Register (ADFM = 1).....	66
ADRESL Register (ADFM = 0).....	66
ADRESL Register (ADFM = 1).....	66
Analog Input Connection Considerations.....	52
Analog-to-Digital Converter. See ADC	
ANSEL Register	33
Assembler	
MPASM Assembler.....	112

B

Block Diagrams

(CCP) Capture Mode Operation	76
ADC	61
ADC Transfer Function	68
Analog Input Model.....	52, 68
CCP PWM.....	78
Clock Source.....	19
Comparator	51
Compare	77
Crystal Operation	22
External RC Mode.....	23
Fail-Safe Clock Monitor (FSCM)	29
GP1 Pin.....	37
GP2 Pin.....	37
GP3 Pin.....	38
GP4 Pin.....	38
GP5 Pin.....	39
In-Circuit Serial Programming Connections.....	100
Interrupt Logic	93
MCLR Circuit.....	86
On-Chip Reset Circuit	85
PIC12F683.....	5
Resonator Operation.....	22
Timer1.....	44

Timer2	49
TMR0/WDT Prescaler	41
Watchdog Timer (WDT).....	96
Brown-out Reset (BOR).....	87
Associated	88
Calibration	87
Specifications	129
Timing and Characteristics	128

C

C Compilers

MPLAB C18.....	112
MPLAB C30.....	112
Calibration Bits.....	85
Capture Module. See Capture/Compare/PWM (CCP)	
Capture/Compare/PWM (CCP)	75
Associated registers w/ Capture, Compare and Timer1	81
Associated registers w/ PWM and Timer2.....	81
Capture Mode	76
CCPx Pin Configuration.....	76
Compare Mode.....	77
CCPx Pin Configuration.....	77
Software Interrupt Mode.....	76, 77
Special Event Trigger	77
Timer1 Mode Selection.....	76, 77

Prescaler	76
PWM Mode	78
Duty Cycle	79
Effects of Reset	80
Example PWM Frequencies and Resolutions, 20 MHZ.....	79
Example PWM Frequencies and Resolutions, 8 MHz	79
Operation in Sleep Mode	80
Setup for Operation	80
System Clock Frequency Changes	80
PWM Period	79
Setup for PWM Operation	80
Timer Resources	75

CCP. See Capture/Compare/PWM (CCP)

CCP1CON Register	75
------------------------	----

Clock Sources

External Modes.....	21
EC	21
HS	22
LP	22
OST	21
RC	23
XT	22
Internal Modes	23
Frequency Selection	25
HFINTOSC	23
INTOSC	23
INTOSCIO	23
LFINTOSC	25

Clock Switching	27
Code Examples	
A/D Conversion	64
Assigning Prescaler to Timer0.....	42
Assigning Prescaler to WDT	42
Changing Between Capture Prescalers	76
Data EEPROM Read	73
Data EEPROM Write	73

PIC12F683

Indirect Addressing	18
Initializing GPIO	31
Saving STATUS and W Registers in RAM	95
Ultra Low-Power Wake-up Initialization	35
Write Verify	73
Code Protection	99
Comparator	51
C2OUT as T1 Gate	57
Configurations	53
I/O Operating Modes	53
Interrupts	55
Operation	51, 54
Operation During Sleep	56
Response Time	54
Synchronizing COUT w/Timer1	57
Comparator Module	59
Associated registers	59
Comparator Voltage Reference (CVREF)	54
Comparator Voltage Reference (CVREF)	58
Effects of a Reset	56
Specifications	132
Comparators	45
C2OUT as T1 Gate	45
Effects of a Reset	56
Specifications	132
Compare Module. See Capture/Compare/PWM (CCP)	84
CONFIG Register	84
Configuration Bits	83
CPU Features	83
Customer Change Notification Service	171
Customer Notification Service	171
Customer Support	171
D	
Data EEPROM Memory	74
Associated Registers	74
Code Protection	71, 74
Data Memory Organization	7
Map of the PIC12F683	8
DC and AC Characteristics	137
Graphs and Tables	137
DC Characteristics	121
Extended and Industrial	121
Industrial and Extended	117
Development Support	111
Device Overview	5
E	
EEADR Register	71
EECON1 Register	72
EECON2 Register	72
EEDAT Register	71
EEPROM Data Memory	74
Avoiding Spurious Write	74
Reading	73
Write Verify	73
Writing	73
Effects of Reset	80
Electrical Specifications	115
Enhanced Capture/Compare/PWM (ECCP)	131
Errata	3
F	
Fail-Safe Clock Monitor	29
Fail-Safe Condition Clearing	29
Fail-Safe Detection	29
Fail-Safe Operation	29
Reset or Wake-up from Sleep	29
Firmware Instructions	101
Fuses. See Configuration Bits	
G	
General Purpose Register File	8
GPIO	31
Additional Pin Functions	32
ANSEL Register	32
Interrupt-on-Change	32
Ultra Low-Power Wake-up	32, 35
Weak Pull-up	32
Associated Registers	39
GP0	36
GP1	37
GP2	37
GP3	38
GP4	38
GP5	39
Pin Descriptions and Diagrams	36
Specifications	127
GPIO Register	31
I	
ID Locations	99
In-Circuit Debugger	100
In-Circuit Serial Programming (ICSP)	100
Indirect Addressing, INDF and FSR Registers	18
Instruction Format	101
Instruction Set	101
ADDLW	103
ADDWF	103
ANDLW	103
ANDWF	103
BCF	103
BSF	103
BTFSZ	103
BTFSZ	104
CALL	104
CLRF	104
CLRW	104
CLRWD	104
COMF	104
DEC	104
DECFSZ	105
GOTO	105
INCF	105
INCFSZ	105
IORLW	105
IORWF	105
MOV	106
MOVLF	106
MOVWF	106
NOP	106
RETFIE	107
RETLW	107
RETURN	107
RLF	108
RRF	108
SLEEP	108

SUBLW	108
SUBWF	109
SWAPF	109
XORLW	109
XORWF	109
INTCON Register	14
Internal Oscillator Block	
INTOSC	
Specifications	126, 127
Internal Sampling Switch (Rss) IMPEDANCE	67
Internet Address	171
Interrupts	92
ADC	64
Associated Registers	94
Comparator	55
Context Saving	95
Data EEPROM Memory Write	72
GP2/INT	92
GPIO Interrupt-on-change	93
Interrupt-on-Change	32
Timer0	93
TMR1	46
INTOSC Specifications	126, 127
IOC Register	34
L	
Load Conditions	124
M	
MCLR	86
Internal	86
Memory Organization	
Data EEPROM Memory	71
Microchip Internet Web Site	171
Migrating from other PIC Devices	165
MPLAB ASM30 Assembler, Linker, Librarian	112
MPLAB ICD 2 In-Circuit Debugger	113
MPLAB ICE 2000 High-Performance Universal	
In-Circuit Emulator	113
MPLAB ICE 4000 High-Performance Universal	
In-Circuit Emulator	113
MPLAB Integrated Development Environment Software ..	111
MPLAB PM3 Device Programmer	113
MPLINK Object Linker/MPLIB Object Librarian	112
O	
OPCODE Field Descriptions	101
OPTION Register	13, 43
OSCCON Register	20
Oscillator	
Associated registers	30, 48
Oscillator Module	19
EC	19
HFINTOSC	19
HS	19
INTOSC	19
INTOSCIO	19
LFINTOSC	19
LP	19
RC	19
RCIO	19
XT	19
Oscillator Parameters	126
Oscillator Specifications	125
Oscillator Start-up Timer (OST)	
Specifications	129
Oscillator Switching	
Fail-Safe Clock Monitor	29
Two-Speed Clock Start-up	27
OSCTUNE Register	24
P	
Packaging	159
Details	160
Marking	159
PCL and PCLATH	18
Computed GOTO	18
Stack	18
PCON Register	17, 88
PICSTART Plus Development Programmer	114
PIE1 Register	15
Pin Diagram	2
Pinout Descriptions	
PIC12F683	6
PIR1 Register	16
Power-Down Mode (Sleep)	98
Power-On Reset (POR)	86
Power-up Timer (PWRT)	86
Specifications	129
Precision Internal Oscillator Parameters	127
Prescaler	
Shared WDT/Timer0	42
Switching Prescaler Assignment	42
Program Memory Organization	7
Map and Stack for the PIC12F683	7
Programming, Device Instructions	101
R	
Reader Response	172
Read-Modify-Write Operations	101
Registers	
ADCON0 (ADC Control 0)	65
ADRESH (ADC Result High) with ADFM = 0	66
ADRESH (ADC Result High) with ADFM = 1	66
ADRESL (ADC Result Low) with ADFM = 0	66
ADRESL (ADC Result Low) with ADFM = 1	66
ANSEL (Analog Select)	33
CCP1CON (CCP1 Control)	75
CMCON0 (Comparator Control) Register	56
CMCON1 (Comparator Control) Register	57
CONFIG (Configuration Word)	84
EEADR (EEPROM Address)	71
EECON1 (EEPROM Control 1)	72
EECON2 (EEPROM Control 2)	72
EEDAT (EEPROM Data)	71
GPIO	31
INTCON (Interrupt Control)	14
IOC (Interrupt-on-Change GPIO)	34
OPTION_REG (OPTION)	13, 43
OSCCON (Oscillator Control)	20
OSCTUNE (Oscillator Tuning)	24
PCON (Power Control Register)	17
PCON (Power Control)	88
PIE1 (Peripheral Interrupt Enable 1)	15
PIR1 (Peripheral Interrupt Register 1)	16
Reset Values	90
Reset Values (Special Registers)	91
STATUS	12
T1CON	47
T2CON	50
TRISIO (Tri-State GPIO)	32
VRCON (Voltage Reference Control)	58

PIC12F683

WDTCON (Watchdog Timer Control).....	97
WPU (Weak Pull-Up GPIO)	34
Resets	85
Brown-out Reset (BOR)	85
MCLR Reset, Normal Operation	85
MCLR Reset, Sleep	85
Power-on Reset (POR)	85
WDT Reset, Normal Operation	85
WDT Reset, Sleep	85
Revision History	165
S	
Sleep	
Power-Down Mode	98
Wake-up.....	98
Wake-up Using Interrupts	98
Software Simulator (MPLAB SIM).....	112
Special Event Trigger.....	64
Special Function Registers	8
STATUS Register.....	12
T	
T1CON Register.....	47
T2CON Register.....	50
Thermal Considerations	123
Time-out Sequence.....	88
Timer0	41
Associated Registers	43
External Clock.....	42
Interrupt.....	13, 43
Operation	41, 44
Specifications.....	130
T0CKI	42
Timer1	44
Associated registers.....	48
Asynchronous Counter Mode	45
Reading and Writing	45
Interrupt.....	46
Modes of Operation	44
Operation During Sleep	46
Oscillator	45
Prescaler.....	45
Specifications.....	130
Timer1 Gate	
Inverting Gate	45
Selecting Source.....	45, 57
Synchronizing COUT w/Timer1	57
TMR1H Register	44
TMR1L Register	44
Timer2	
Associated registers.....	50
Timers	
Timer1	
T1CON	47
Timer2	
T2CON	50
Timing Diagrams	
A/D Conversion	135
A/D Conversion (Sleep Mode)	135
Brown-out Reset (BOR)	128
Brown-out Reset Situations	87
CLKOUT and I/O	127
Clock Timing	125
Comparator Output	51
Enhanced Capture/Compare/PWM (ECCP)	131
Fail-Safe Clock Monitor (FSCM)	30
INT Pin Interrupt	94
Internal Oscillator Switch Timing	26
Reset, WDT, OST and Power-up Timer	128
Time-out Sequence on Power-up (<u>Delayed MCLR</u>)	89
Time-out Sequence on Power-up (MCLR with VDD)	89
Timer0 and Timer1 External Clock	130
Timer1 Incrementing Edge	46
Two Speed Start-up.....	28
Wake-up from Sleep Through Interrupt	99
Timing Parameter Symbology	124
TRISIO Register	32
Two-Speed Clock Start-up Mode.....	27
U	
Ultra Low-Power Wake-up.....	32, 35
V	
Voltage Reference. See Comparator Voltage Reference (CVREF)	
Voltage References	
Associated registers	59
VREF. SEE ADC Reference Voltage	
W	
Wake-up Using Interrupts	98
Watchdog Timer (WDT)	96
Associated Registers	97
Clock Source	96
Modes.....	96
Period	96
Specifications	129
WDTCON Register	97
WPU Register	34
WWW Address	171
WWW, On-Line Support	3

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PIC12F683

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<u>PART NO.</u>	X	XX	XXX	
Device	Temperature Range	Package	Pattern	
Device: PIC12F683 ⁽¹⁾ , PIC12F683T ⁽²⁾ VDD range 2.0V to 5.5V				
Temperature Range:	I = -40°C to +85°C(Industrial) E = -40°C to +125°C (Extended)			
Package:	P = Plastic DIP MD = Dual-Flat, No Leads (DFN-S, 4x4x0.9 mm) MF = Dual-Flat, No Leads (DFN-S, 6x5 mm) SN = 8-lead Small Outline (3.90 mm)			
Pattern:	3-digit Pattern Code for QTP (blank otherwise)			
Examples: a) PIC12F683-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301 b) PIC12F683-I/SN = Industrial Temp., SOIC package, 20 MHz				
Note 1: F = Standard Voltage Range LF = Wide Voltage Range 2: T = in tape and reel PLCC, and TQFP packages only.				



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**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

**'46A, '47A, 'LS47
feature**

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

**'48, 'LS48
feature**

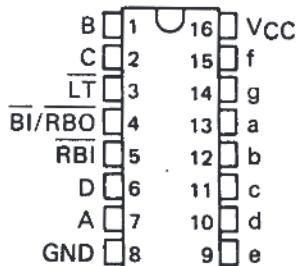
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

**'LS49
feature**

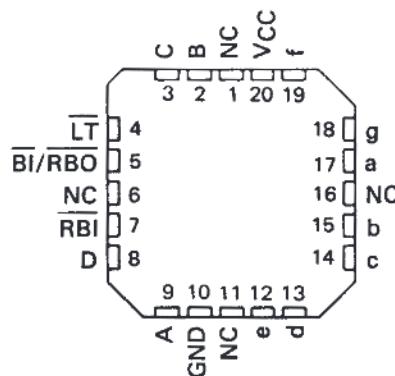
- Open-Collector Outputs
- Blanking Input

SN5446A, SN5447A, SN54LS47, SN5448,
SN54LS48 . . . J PACKAGE
SN7446A, SN7447A,
SN7448 . . . N PACKAGE
SN74LS47, SN74LS48 . . . D OR N PACKAGE

(TOP VIEW)

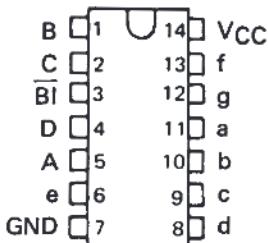


SN54LS47, SN54LS48 . . . FK PACKAGE
(TOP VIEW)

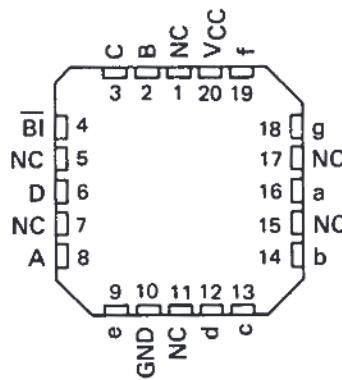


SN54LS49 . . . J OR W PACKAGE
SN74LS49 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS49 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

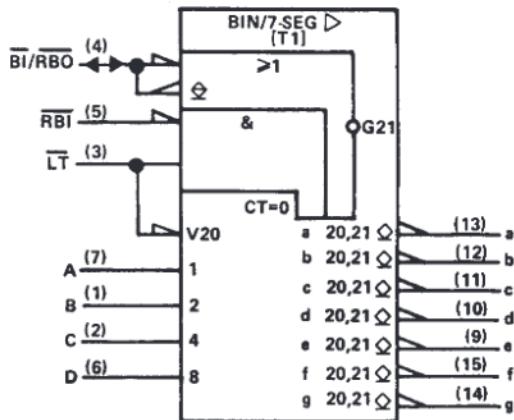
SDLS111 – MARCH 1974 – REVISED MARCH 1988

- All Circuit Types Feature Lamp Intensity Modulation Capability

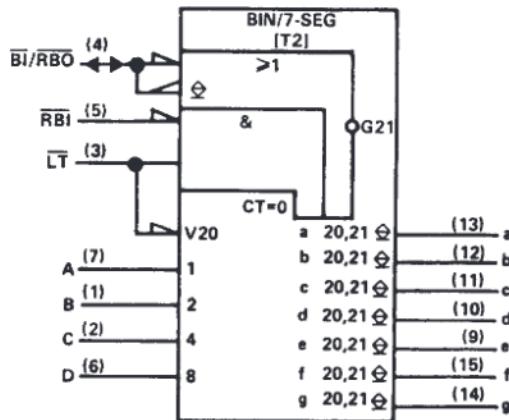
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J,W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

logic symbols†

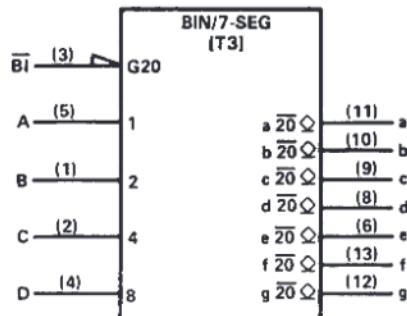
'46A, '47A, 'LS47



'48, 'LS48



'LS49



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

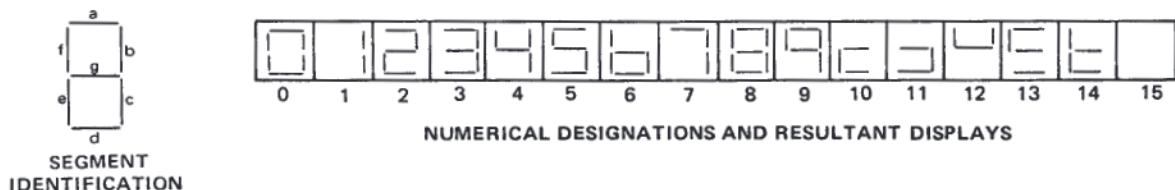
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description

The '46A, '47A, and 'LS47 feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. The '48, 'LS48, and 'LS49 feature active-high outputs for driving lamp buffers or common-cathode LEDs. All of the circuits except 'LS49 have full ripple-blanking input/output controls and a lamp test input. The 'LS49 circuit incorporates a direct blanking input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (\overline{BI} and \overline{RBO}). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input (BI), which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL logic outputs.

The SN54246/SN74246 and '247 and the SN54LS247/SN74LS247 and 'LS248 compose the \square and the \square with tails and were designed to offer the designer a choice between two indicator fonts.



'46A, '47A, 'LS47 FUNCTION TABLE (T1)

DECIMAL OR FUNCTION	INPUTS					$\overline{BI}/\overline{RBO}^{\dagger}$	OUTPUTS							NOTE
	LT	RBI	D	C	B	A	a	b	c	d	e	f		
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON						
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF						
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

- NOTES:
1. The blanking input (\overline{BI}) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (\overline{RBI}) must be open or high if blanking of a decimal zero is not desired.
 2. When a low logic level is applied directly to the blanking input (\overline{BI}), all segment outputs are off regardless of the level of any other input.
 3. When ripple-blanking input (\overline{RBI}) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (\overline{RBO}) goes to a low level (response condition).
 4. When the blanking input/ripple blanking output ($\overline{BI}/\overline{RBO}$) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

[†] $\overline{BI}/\overline{RBO}$ is wire AND logic serving as blanking input (\overline{BI}) and/or ripple-blanking output (\overline{RBO}).

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

'48, 'LS48
FUNCTION TABLE (T2)

DECIMAL OR FUNCTION	INPUTS					\overline{BI}/RBO^t	OUTPUTS							NOTE
	LT	RBI	D	C	B	A	a	b	c	d	e	f		
0	H	H	L	L	L	L	H	H	H	H	H	H	L	
1	H	X	L	L	L	H	H	L	H	H	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	
3	H	X	L	L	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	
BI	X	X	X	X	X		L	L	L	L	L	L	L	2
RBI	H	L	L	L	L		L	L	L	L	L	L	L	3
LT	L	X	X	X	X		H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (\overline{BI}) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
 2. When a low logic level is applied directly to the blanking input (\overline{BI}), all segment outputs are low regardless of the level of any other input.
 3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (\overline{RBO}) goes to a low level (response condition).
 4. When the blanking input/ripple-blanking output (\overline{BI}/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

\overline{BI}/RBO is wire-AND logic serving as blanking input (\overline{BI}) and/or ripple-blanking output (\overline{RBO}).

'LS49
FUNCTION TABLE (T3)

DECIMAL OR FUNCTION	INPUTS					\overline{BI}	OUTPUTS							NOTE
	D	C	B	A			a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	H	L	
1	L	L	L	H	H	L	H	H	L	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	H	
3	L	L	H	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	H	
12	H	H	L	L	H	L	H	L	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	L	
BI	X	X	X	X		L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

- NOTES: 1. The blanking input (\overline{BI}) must be open or held at a high logic level when output functions 0 through 15 are desired.
 2. When a low logic level is applied directly to the blanking input (\overline{BI}), all segment outputs are low regardless of the level of any other input.

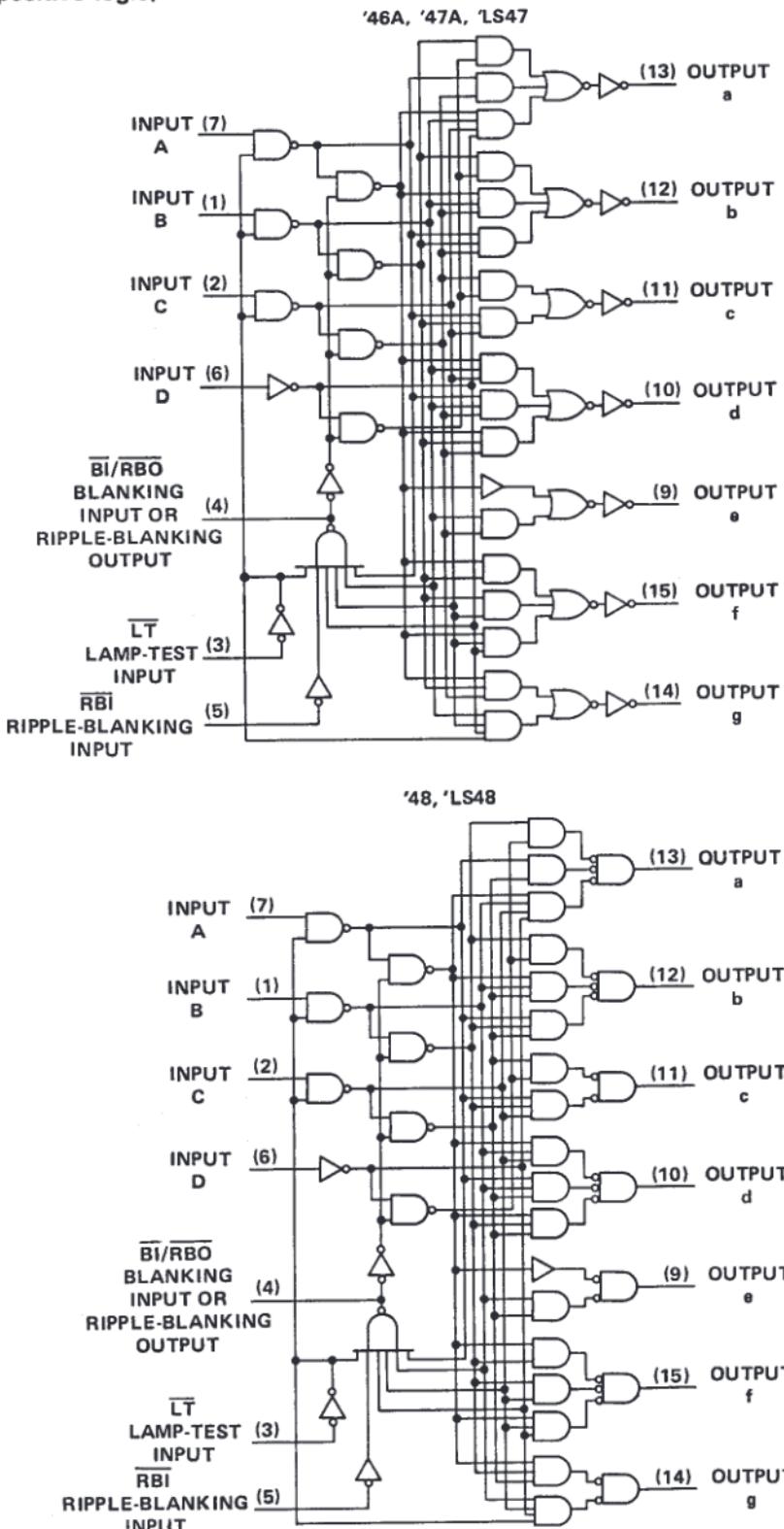


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

logic diagrams (positive logic)

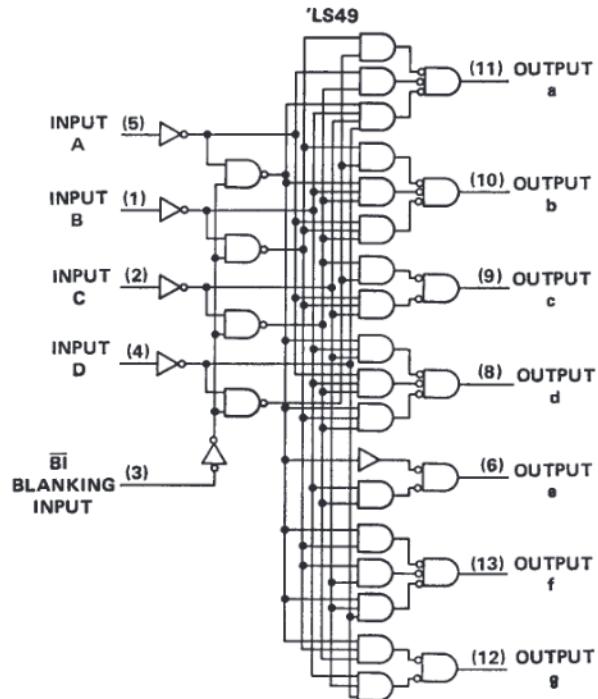


Pin numbers shown are for D, J, N, and W packages.

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

logic diagrams (continued)



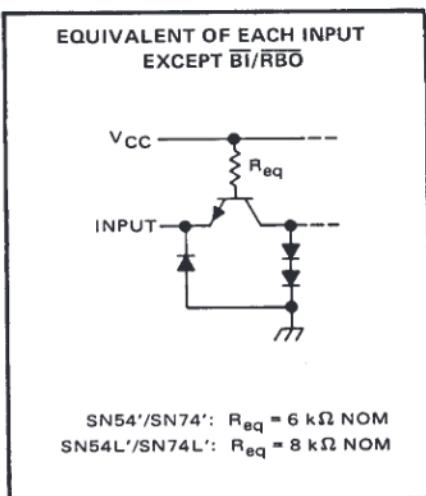
Pin numbers shown are for D, J, N, and W packages.

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

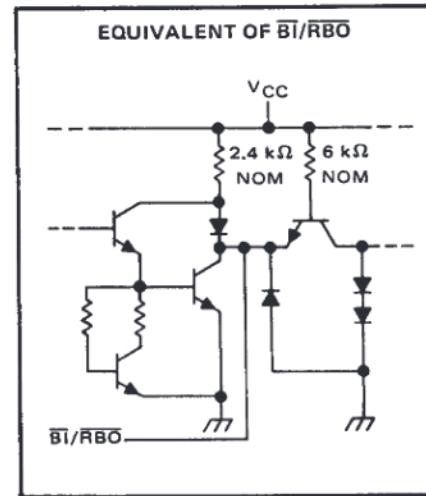
SDLS111 – MARCH 1974 – REVISED MARCH 1988

schematics of inputs and outputs

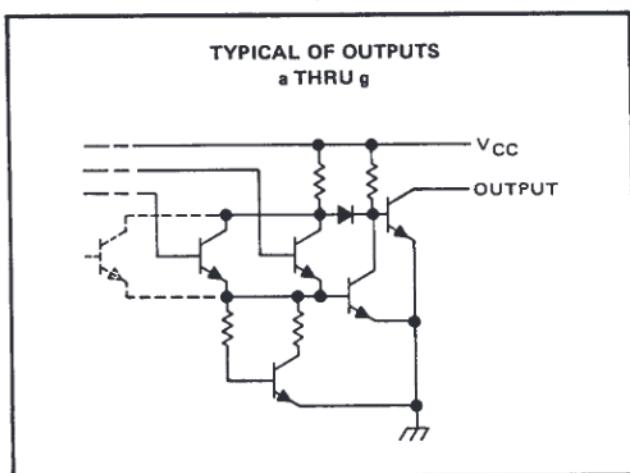
'46A, '47A, '48



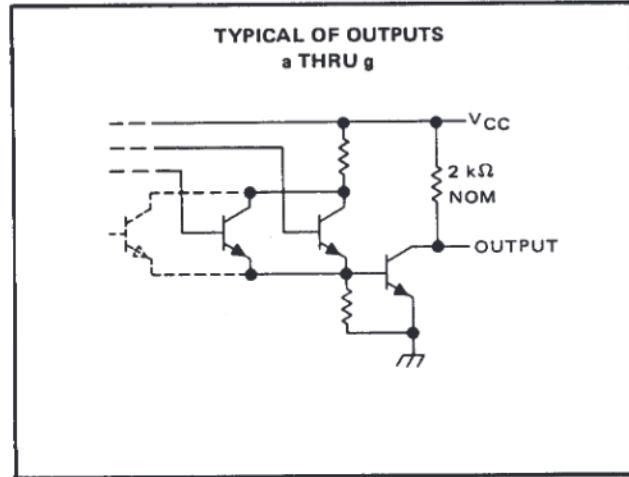
'46A, '47A, '48



'46A, '47A



'48



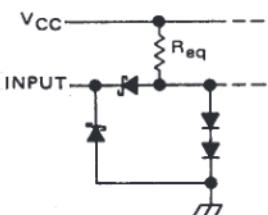
**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

schematics of inputs and outputs

'LS47, 'LS48, 'LS49

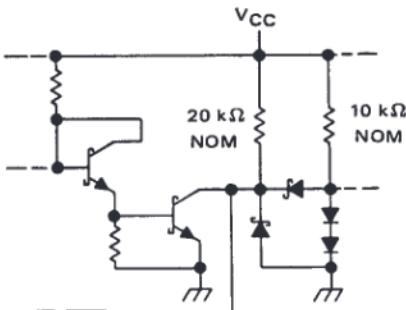
EQUIVALENT OF EACH INPUT
 EXCEPT $\overline{BI}/\overline{RBO}$



\overline{LT} and \overline{RB} ('LS47, 'LS48): $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$
 \overline{BI} ('LS49): $R_{eq} = 20 \text{ k}\Omega \text{ NOM}$
 A, B, C, and D: $R_{eq} = 25 \text{ k}\Omega \text{ NOM}$

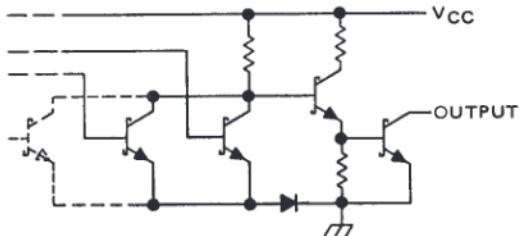
'LS47, 'LS48, 'LS49

EQUIVALENT OF $\overline{BI}/\overline{RBO}$



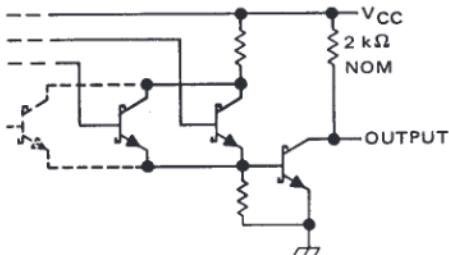
'LS47

TYPICAL OF OUTPUTS
 a THRU g



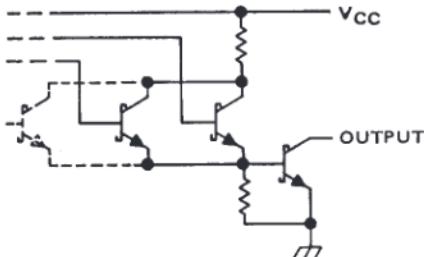
'LS48

TYPICAL OF OUTPUTS
 a THRU g



'LS49

TYPICAL OF OUTPUTS
 a THRU g



**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**
SDS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN5446A, SN5447A	-55°C to 125°C
SN7446A, SN7447A	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5446A			SN5447A			SN7446A			SN7447A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_O(\text{off})$	a thru g	30			15		30			15			V
On-state output current, $I_O(\text{on})$	a thru g	40			40		40			40			mA
High-level output current, I_{OH}	\overline{BI}/RBO	-200			-200		-200			-200			μA
Low-level output current, I_{OL}	\overline{BI}/RBO	8			8		8			8			mA
Operating free-air temperature, T_A	-55	125	-55	125	0	70	0	70		0	70		$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT	
V _{IH} High-level input voltage				2		V	
V _{IL} Low-level input voltage				0.8		V	
V _{IK} Input clamp voltage		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V	
V _{OH} High-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -200 \mu A$	2.4	3.7		V	
V _{OL} Low-level output voltage		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 8 \text{ mA}$		0.27	0.4	V	
I _{O(off)} Off-state output current		a thru g	V _{CC} = MAX, $V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_O(\text{off}) = \text{MAX}$		250	μA	
V _{O(on)} On-state output voltage		a thru g	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_O(\text{on}) = 40 \text{ mA}$	0.3	0.4	V	
I _I Input current at maximum input voltage		Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1	mA	
I _{IH} High-level input current		Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40	μA	
I _{IL} Low-level input current		Any input except \overline{BI}/RBO	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6	mA	
		\overline{BI}/RBO			-4		
I _{OS} Short-circuit output current		\overline{BI}/RBO	$V_{CC} = \text{MAX}$		-4	mA	
I _{CC} Supply current			$V_{CC} = \text{MAX}, \text{See Note 2}$	SN54'	64	85	mA
				SN74'	64	103	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	$C_L = 15 \text{ pF}, R_L = 120 \Omega,$ See Note 3		100		ns
t_{on}	Turn-on time from A input			100		
t_{off}	Turn-off time from \overline{BI} input			100		ns
t_{on}	Turn-on time from \overline{BI} input			100		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5448	-55°C to 125°C
SN7448	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5448			SN7448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	a thru g	-400		-400			μA
	BI/RBO	-200		-200			
Low-level output current, I _{OL}	a thru g	6.4		6.4			mA
	BI/RBO	8		8			
Operating free-air temperature, T _A	-55	125	0	70			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
V _{IH} High-level input voltage			2			V
V _{IL} Low-level input voltage				0.8		V
V _{IK} Input clamp voltage		V _{CC} = MIN, I _I = -12 mA		-1.5		V
V _{OH} High-level output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V,	2.4	4.2		V
	BI/RBO	V _{IL} = 0.8 V, I _{OH} = MAX	2.4	3.7		
I _O Output current	a thru g	V _{CC} = MIN, V _O = 0.85 V, Input conditions as for V _{OH}	-1.3	-2		mA
V _{OL} Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX		0.27	0.4	V
I _I Input current at maximum input voltage	Any input except BI/RBO	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH} High-level input current	Any input except BI/RBO	V _{CC} = MAX, V _I = 2.4 V		40		μA
I _{IL} Low-level input current	Any input except BI/RBO	V _{CC} = MAX, V _I = 0.4 V		-1.6		mA
	BI/RBO			-4		
I _{OS} Short-circuit output current	BI/RBO	V _{CC} = MAX		-4		mA
I _{CC} Supply current		V _{CC} = MAX, SN5448	53	76		mA
		See Note 2, SN7448	53	90		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL} Propagation delay time, high-to-low-level output from A input	C _L = 15 pF, R _L = 1 kΩ See Note 3		100		ns
t _{TPLH} Propagation delay time, low-to-high-level output from A input			100		
t _{PHL} Propagation delay time, high-to-low-level output from BI input			100		
t _{TPLH} Propagation delay time, low-to-high-level output from BI input			100		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$)	200 mA
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS47 SN74LS47	-55°C to 125°C 0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_O(\text{off})$	a thru g			15			15	V
On-state output current, $I_O(\text{on})$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			-50			-50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		-55	125	0	0	70	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS47			SN74LS47			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2		2	2		2	V
V_{IL}	Low-level input voltage			0.7		0.7		0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18$ mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	BI/RBO	$V_{CC} = \text{MIN}$, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max, $I_{OH} = -50$ μA	2.4	4.2	2.4	4.2	2.4	V
V_{OL}	Low-level output voltage	BI/RBO	$V_{CC} = \text{MIN}$, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max	0.25	0.4	0.25	0.4	0.25	V
$I_{O(\text{off})}$	Off-state output current	a thru g	$V_{CC} = \text{MAX}$, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max, $V_O(\text{off}) = 15$ V		250		250	250	
$V_{O(\text{on})}$	On-state output voltage	a thru g	$V_{CC} = \text{MIN}$, $V_{IH} = 2$ V, $V_{IL} = V_{IL}$ max	0.25	0.4	0.25	0.4	0.25	V
I_I	Input current at maximum input voltage		$I_{O(\text{on})} = 12$ mA		0.1		0.1	0.1	
I_{IH}	High-level input current		$I_{O(\text{on})} = 24$ mA				0.35	0.5	μA
I_{IL}	Low-level input current	Any input except BI/RBO	$V_{CC} = \text{MAX}$, $V_I = 0.4$ V		-0.4		-0.4	-0.4	mA
		BI/RBO			-1.2		-1.2	-1.2	
I_{OS}	Short-circuit output current	BI/RBO	$V_{CC} = \text{MAX}$	-0.3	-2	-0.3	-2	-2	mA
I_{CC}	Supply current		$V_{CC} = \text{MAX}$, See Note 2	7	13	7	13	7	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	$C_L = 15$ pF, $R_L = 665$ Ω, See Note 3	100			ns
t_{on}		100			
t_{off}		100			
t_{on}		100			

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 – MARCH 1974 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS48	-55°C to 125°C
SN74LS48	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS48			SN74LS48			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	a thru g	-100		-100		-50	-50	μA
	BI/RBO	-50		-50				
Low-level output current, I _{OL}	a thru g	2		6		1.6	3.2	mA
	BI/RBO	1.6		3.2				
Operating free-air temperature, T _A		-55	125	0	70	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN54LS48			SN74LS48			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage			0.7			0.8		V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	High-level output voltage	a thru g and BI/RBO	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, I _{OH} = MAX	2.4	4.2	2.4	4.2		V
I _O	Output current	a thru g	V _{CC} = MIN, V _O = 0.85 V, Input conditions as for V _{OH}	-1.3	-2	-1.3	-2		mA
V _{OL}	Low-level output voltage	a thru g	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 2 mA	0.25	0.4	0.25	0.4	V
				I _{OL} = 6 mA			0.35	0.5	
V _{OL}		BI/RBO	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 1.6 mA	0.25	0.4	0.25	0.4	V
				I _{OL} = 3.2 mA			0.35	0.5	
I _I	Input current at maximum input voltage	Any input except BI/RBO	V _{CC} = MAX, V _I = 7 V		0.1			0.1	mA
I _{IH}	High-level input current	Any input except BI/RBO	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
I _{IL}	Low-level input current	Any input except BI/RBO	V _{CC} = MAX, V _I = 0.4 V		-0.4		-0.4		mA
					-1.2		-1.2		
I _{OS}	Short-circuit output current	BI/RBO	V _{CC} = MAX	-0.3	-2	-0.3	-2		mA
I _{CC}	Supply current		V _{CC} = MAX, See Note 2		25	38	25	38	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL}	Propagation delay time, high-to-low-level output from A input	C _L = 15 pF, R _L = 4 kΩ,			ns
			See Note 3		
t _{PLH}	Propagation delay time, low-to-high-level output from A input	C _L = 15 pF, R _L = 6 kΩ,			ns
			See Note 3		

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN5446A, '47A, '48, SN54LS47, 'LS48, 'LS49
 SN7446A, '47A, '48, SN74LS47, 'LS48, 'LS49
 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS**

SDLS111 - MARCH 1974 - REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Current forced into any output in the off state	1 mA
Operating free-air temperature range: SN54LS49	-55°C to 125°C
SN74LS49	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5		5.5	V
Low-level output current, I_{OL}				1		8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS49			SN74LS49			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage			0.7			0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$, $V_{OH} = 5.5 \text{ V}$			250			250	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL} \text{ max}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4		V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$			0.1			0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		8	15	8	15		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A input	$C_L = 15 \text{ pF}$, $R_L = 4 \text{ k}\Omega$, See Note 3			100	ns
t_{PLH} Propagation delay time, low-to-high-level output from A input				100	
t_{PHL} Propagation delay time, high-to-low-level output (a-f only) from $\overline{\text{RBI}}$ input	$C_L = 15 \text{ pF}$, $R_L = 6 \text{ k}\Omega$, See Note 3			100	ns
t_{PLH} Propagation delay time, low-to-high-level output (a-f only) from $\overline{\text{RBI}}$ input				100	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9856401QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9856401QE A SNJ5447AJ
5962-9856401QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9856401QF A SNJ5447AW
7604501EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7604501EA SNJ54LS47J
SN5447AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN5447AJ
SN54LS47J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS47J
SN54LS49J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS49J
SN7447AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7447AN
SN7447ANE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN7447AN
SN74LS47D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS47
SN74LS47DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	LS47	Samples
SN74LS47N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS47N
SN74LS47NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS47N
SN74LS47NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS47
SNJ5447AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9856401QE A SNJ5447AJ
SNJ5447AW	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9856401QF A SNJ5447AW
SNJ54LS47FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS 47FK

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (³)	Op Temp (°C)	Device Marking (^{4/5})	Samples
SNJ54LS47J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125 7604501EA SNJ54LS47J	Samples
SNJ54LS49J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125 SNJ54LS49J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS-T09B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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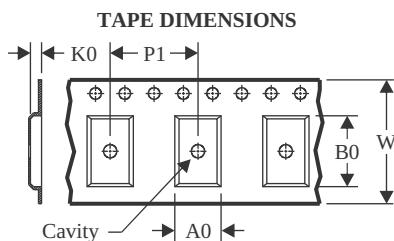
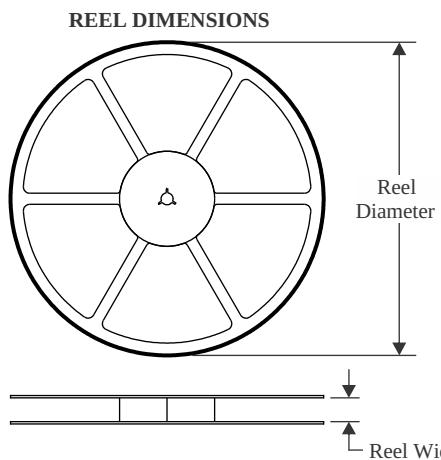
OTHER QUALIFIED VERSIONS OF SN5447A, SN54LS47, SN7447A, SN74LS47 :

- Catalog : [SN7447A](#), [SN74LS47](#)

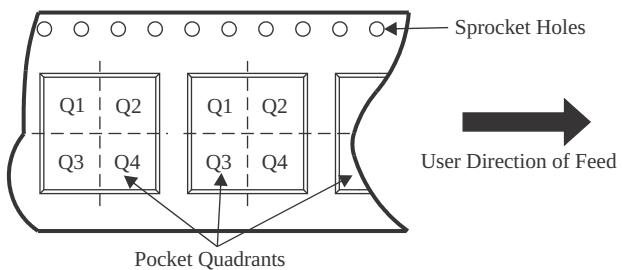
- Military : [SN5447A](#), [SN54LS47](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

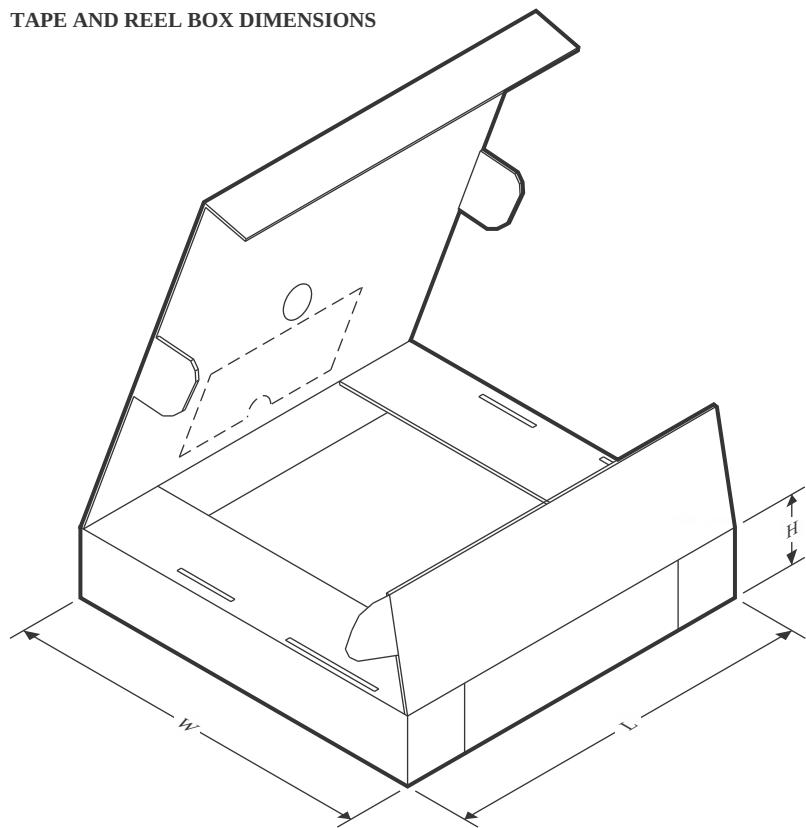
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


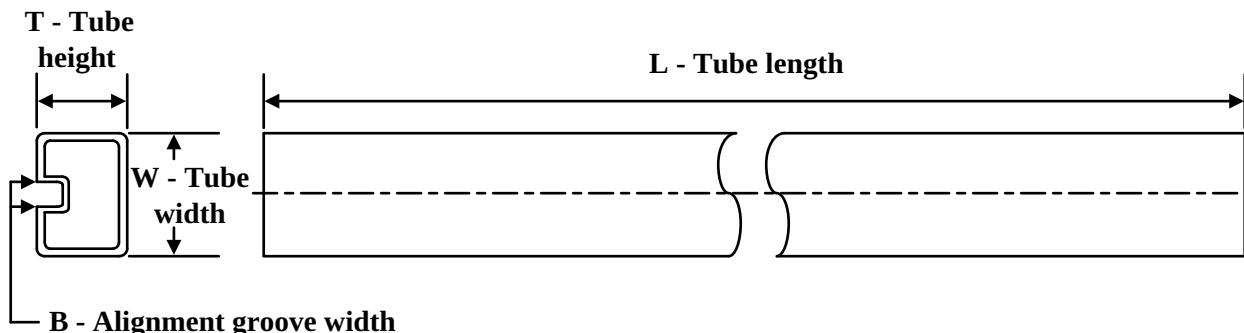
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS47DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS47NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS47DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS47NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-9856401QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN7447AN	N	PDIP	16	25	506	13.97	11230	4.32
SN7447AN	N	PDIP	16	25	506	13.97	11230	4.32
SN7447ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN7447ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47D	D	SOIC	16	40	507	8	3940	4.32
SN74LS47N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS47NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ5447AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS47FK	FK	LCCC	20	55	506.98	12.06	2030	NA

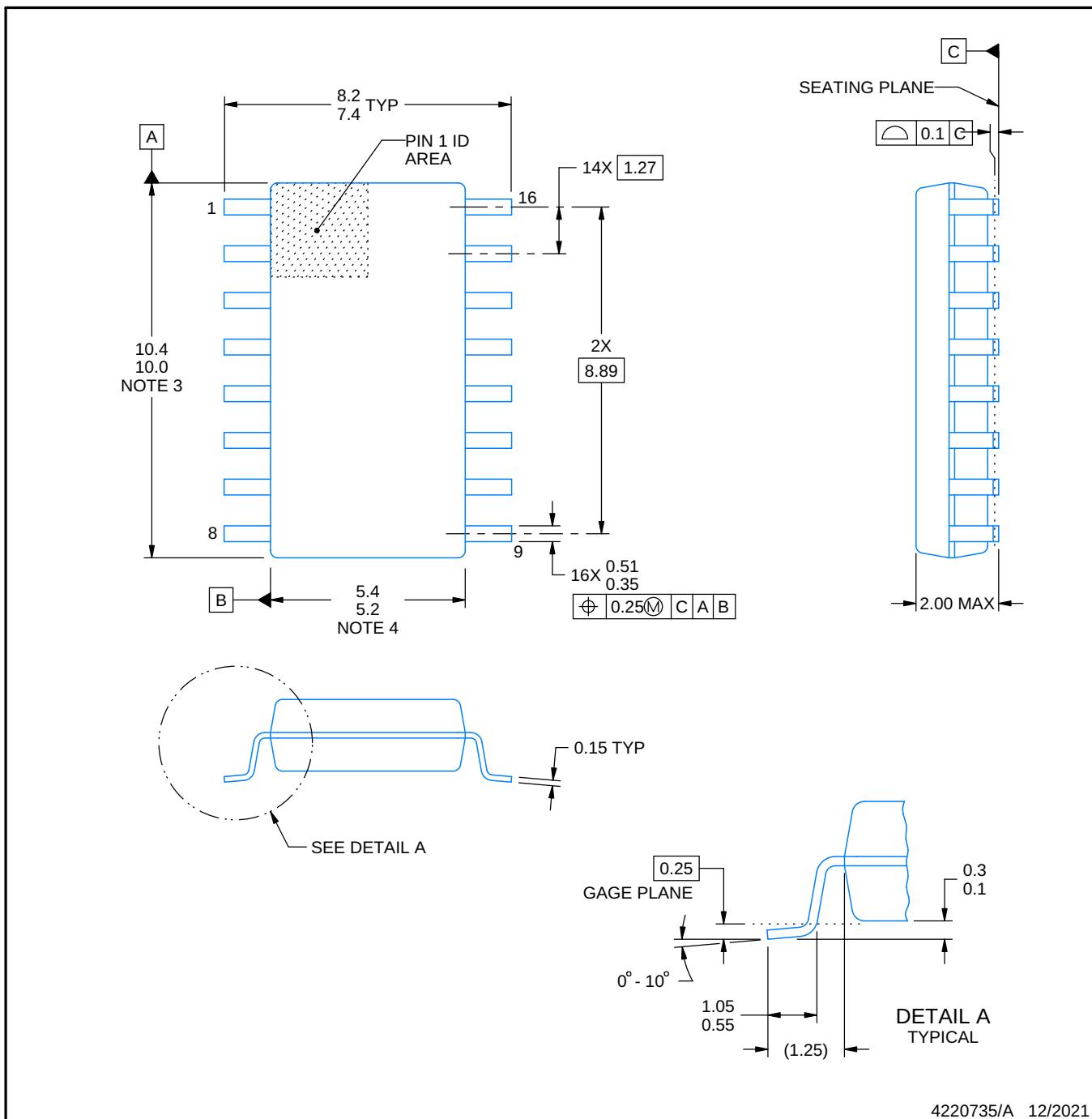
NS0016A



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

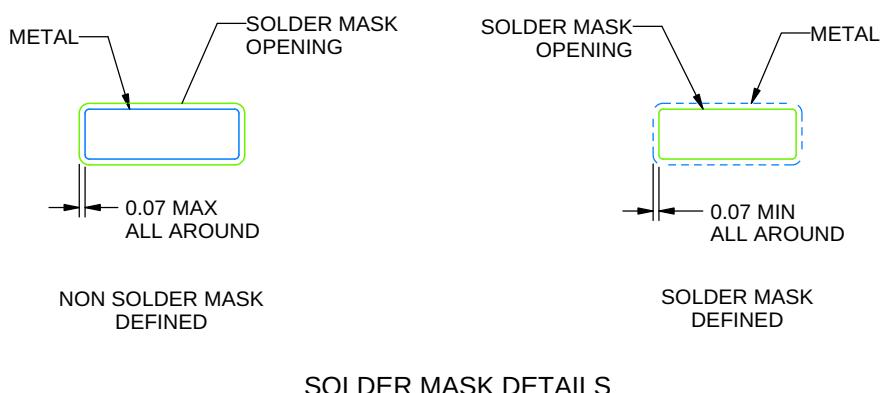
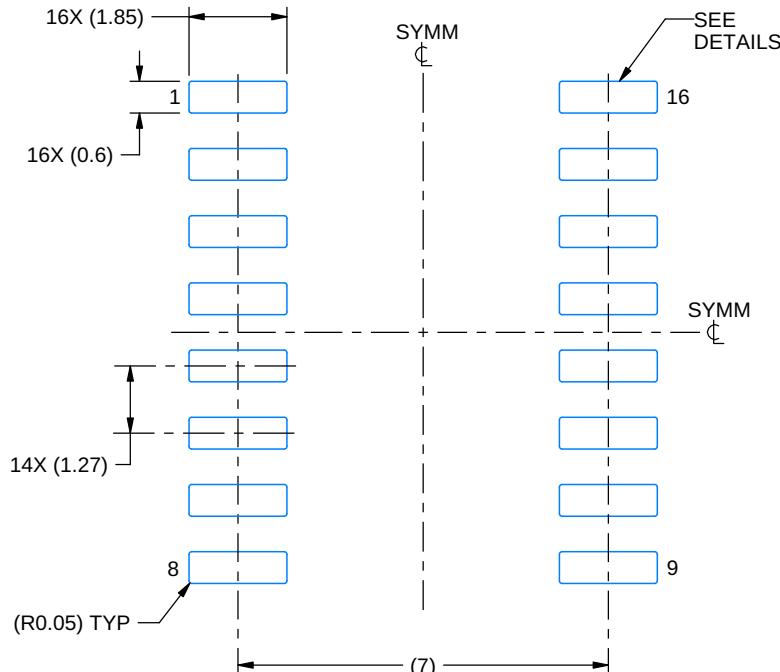
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

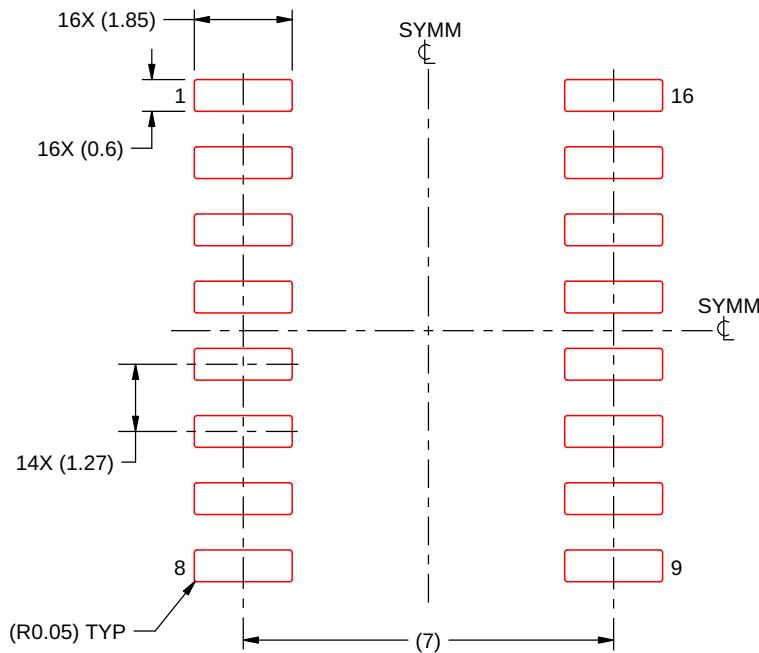
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

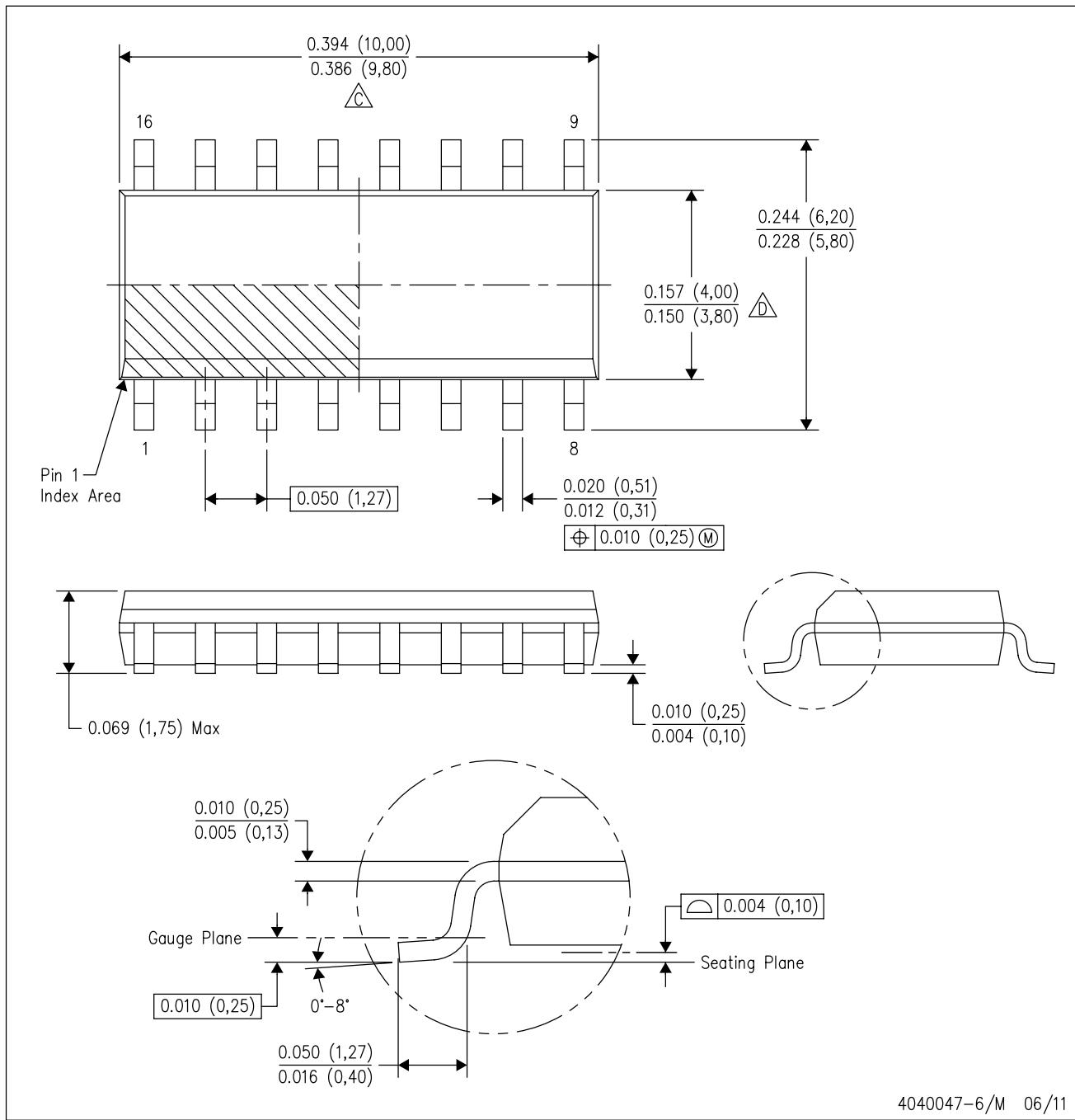
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

$\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

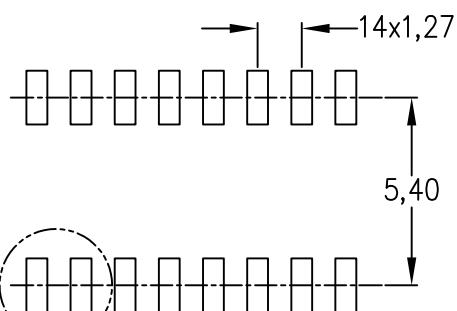
$\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

LAND PATTERN DATA

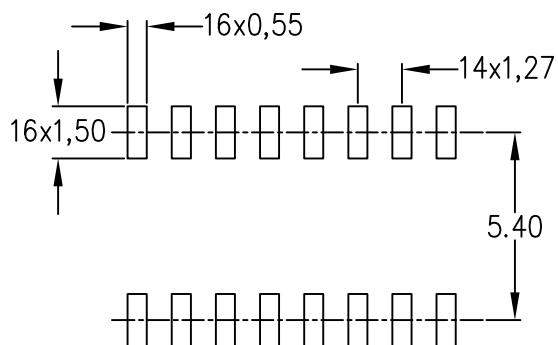
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

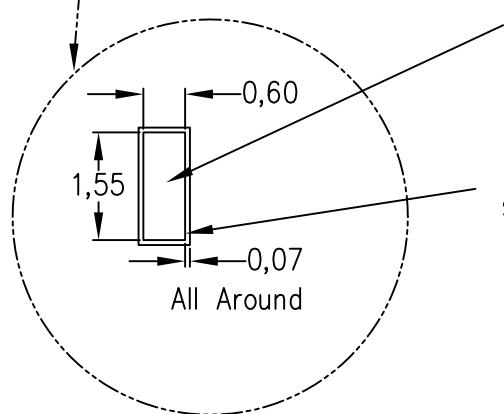
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

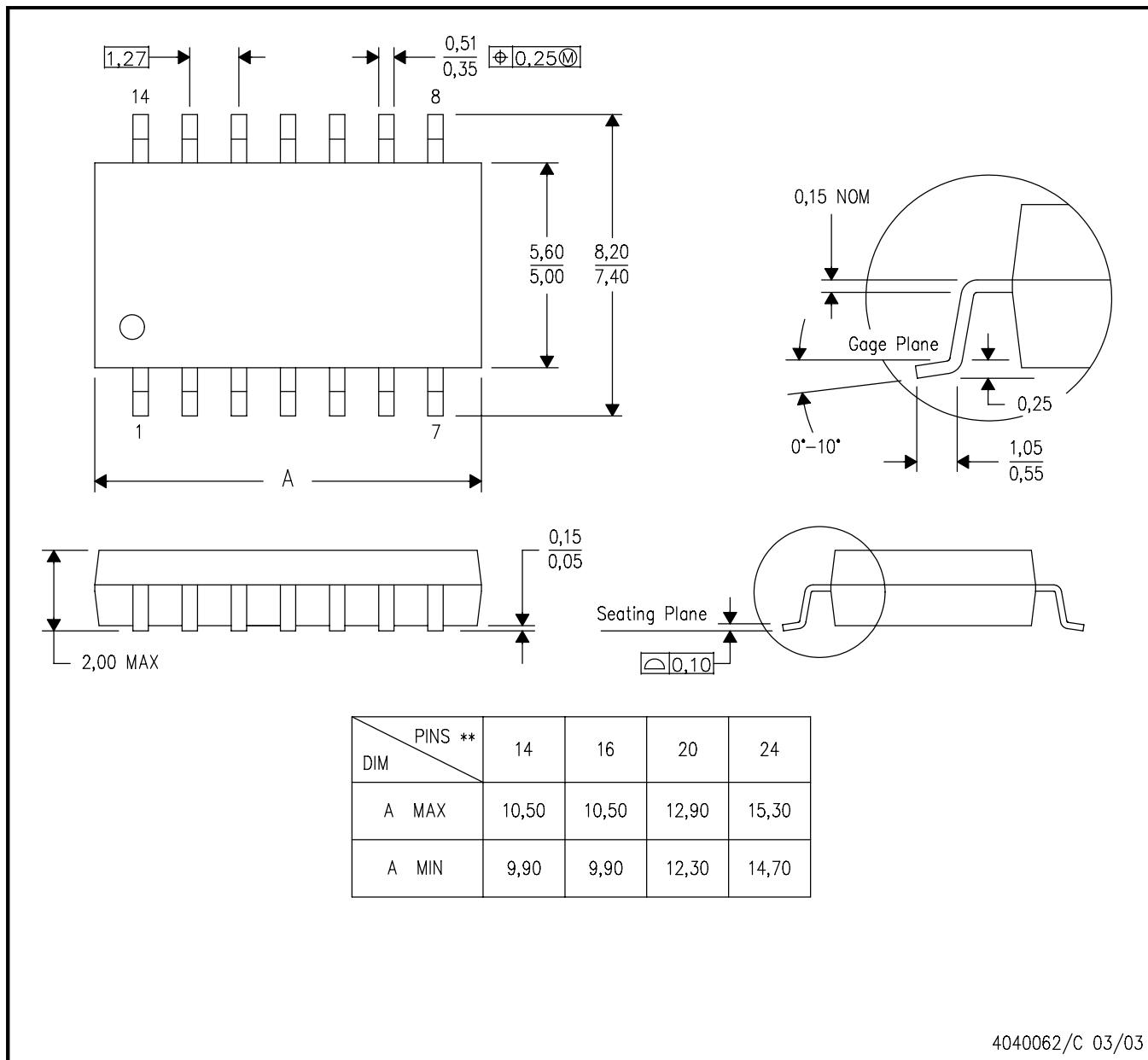
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



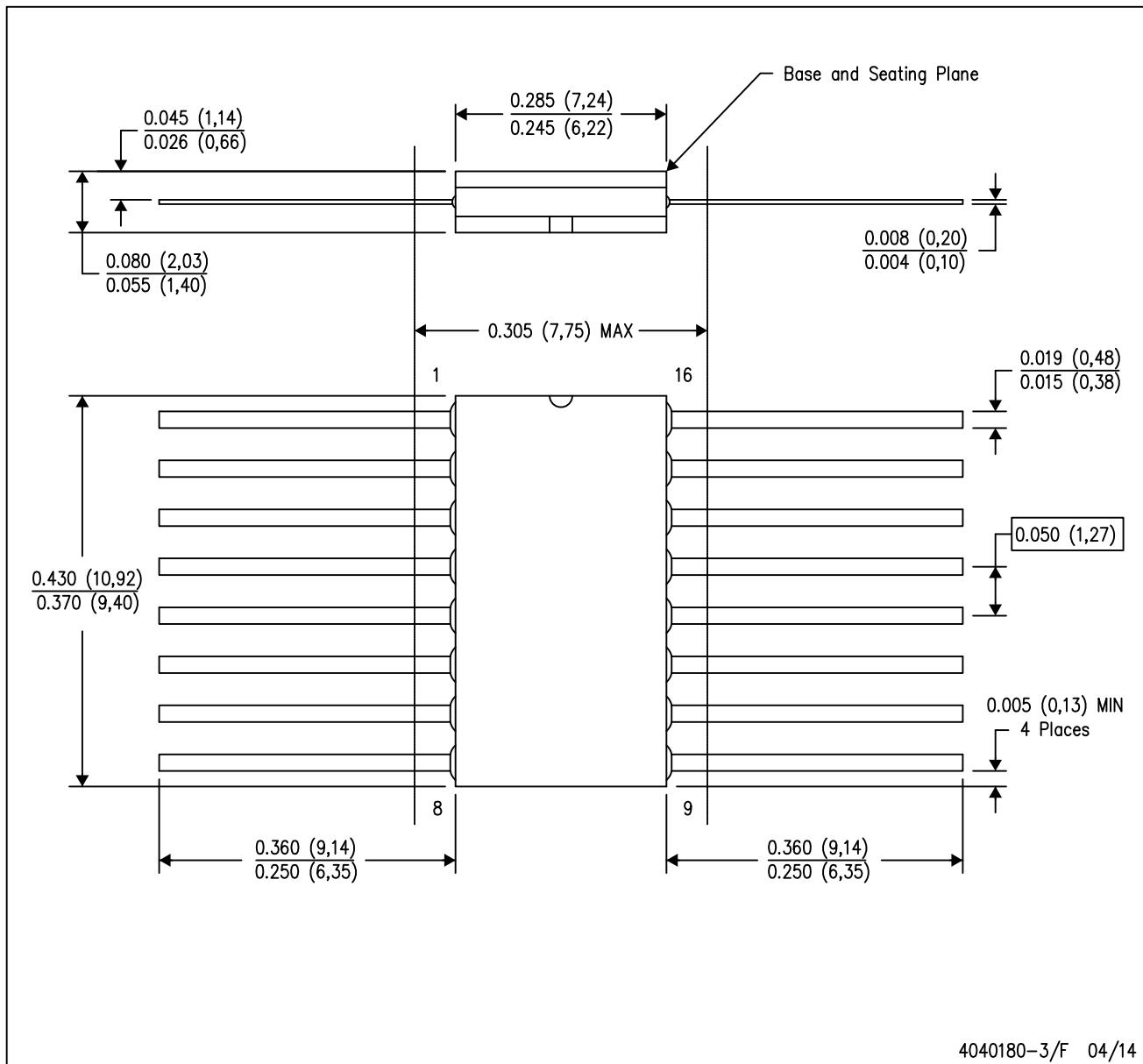
4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

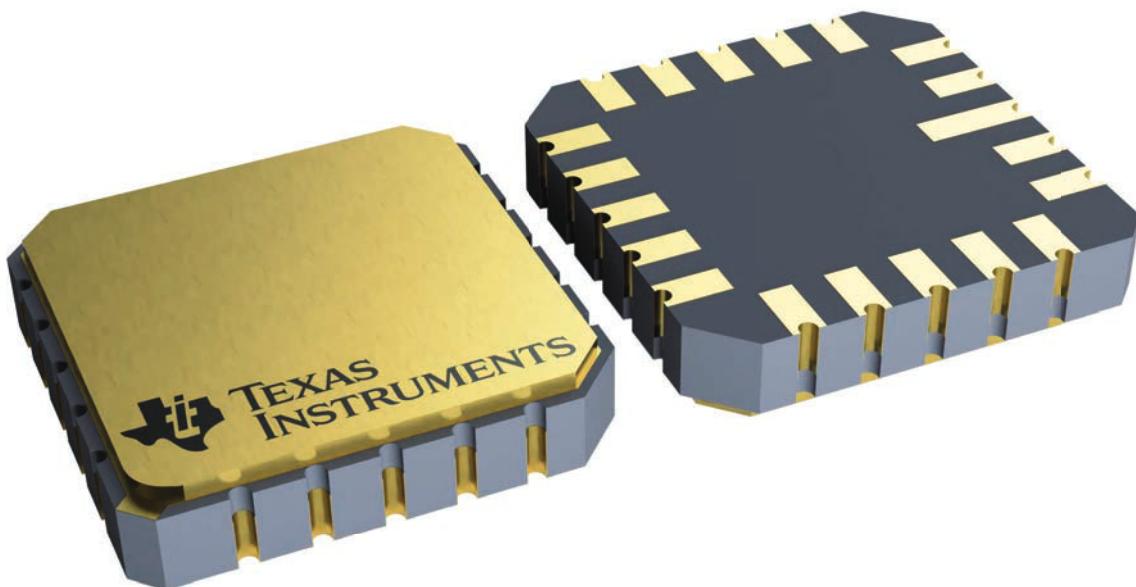
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

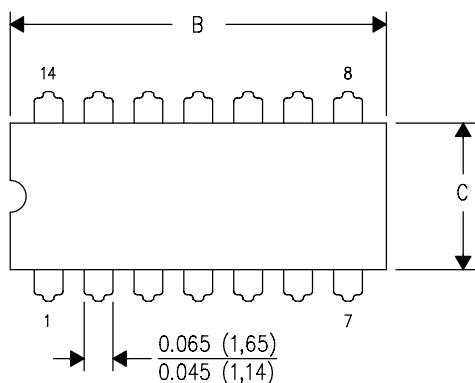


4229370VA\

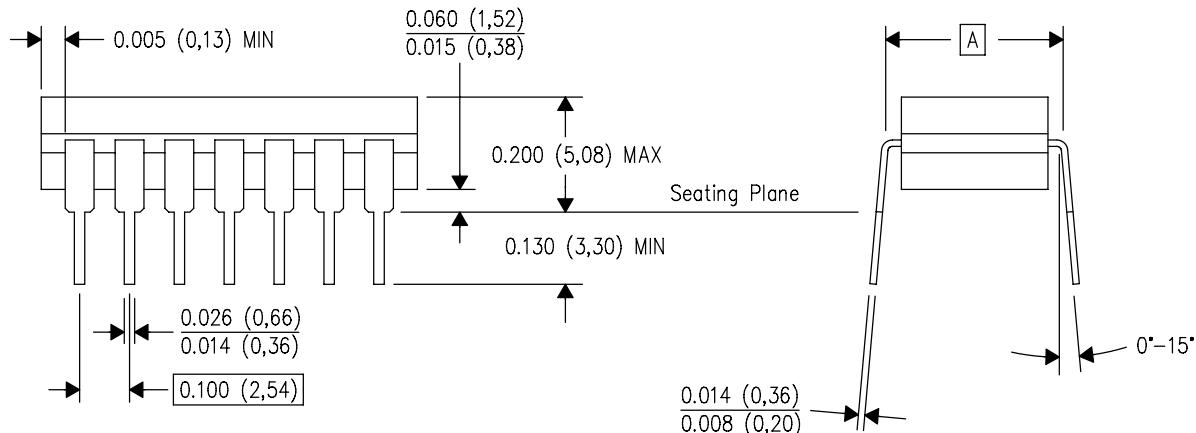
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS **\nDIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

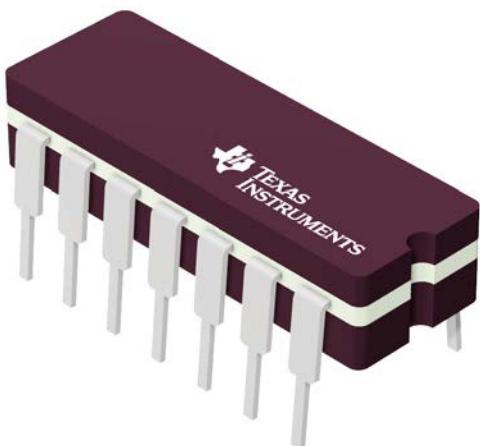
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

J 14

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

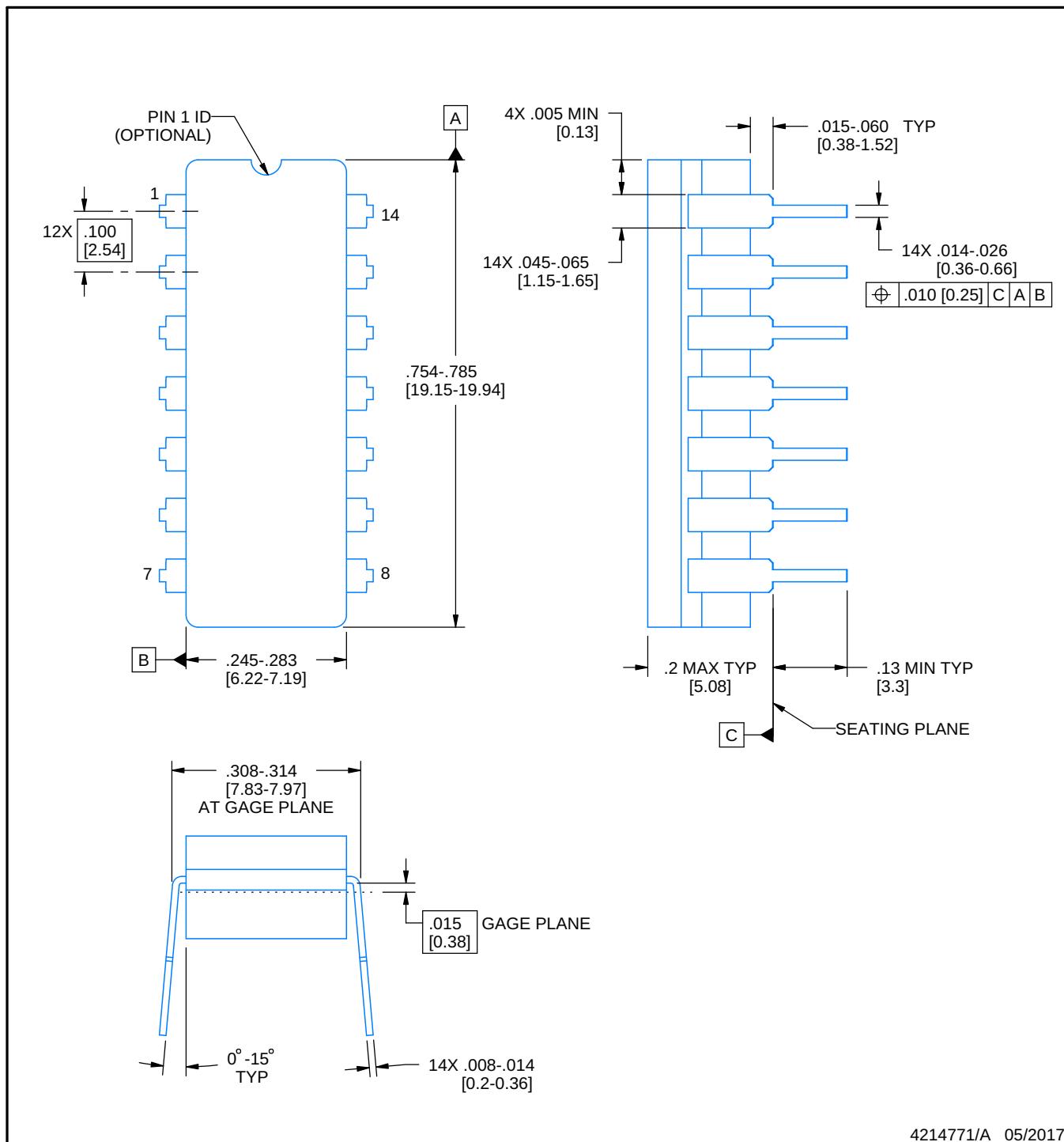
J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

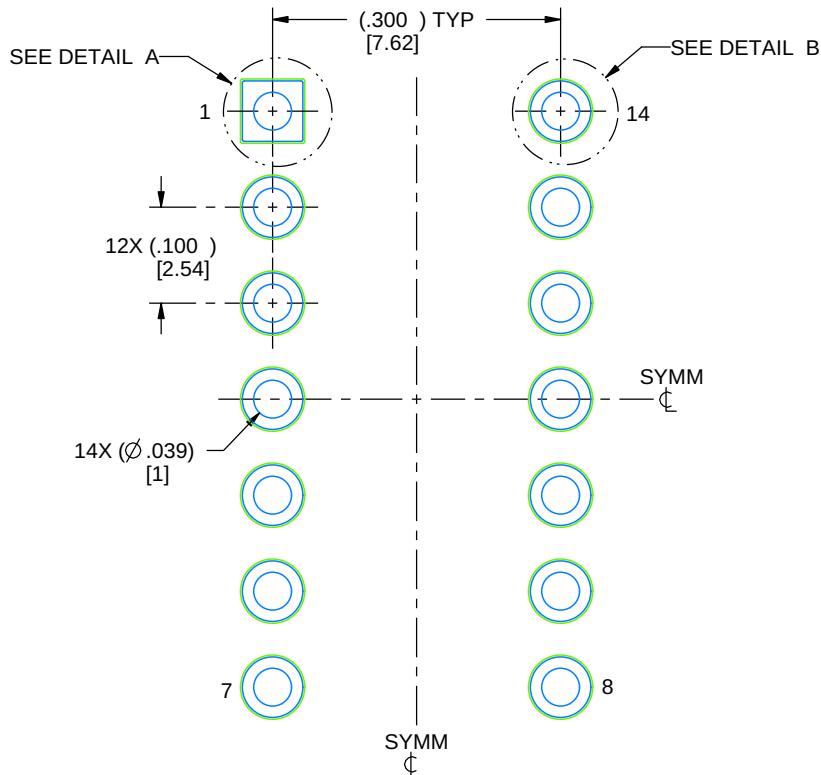
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

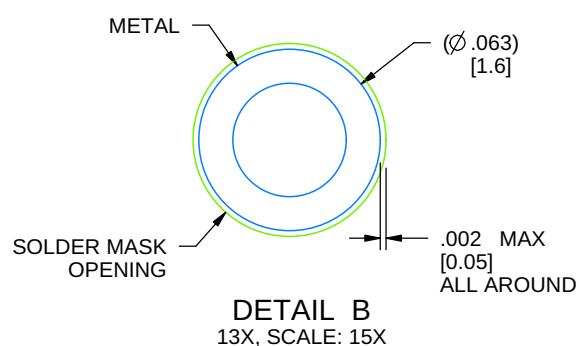
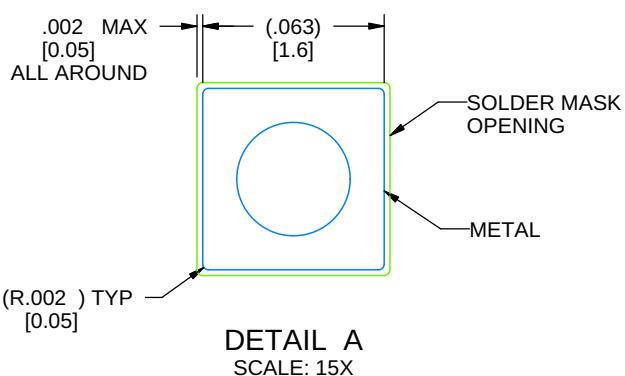
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

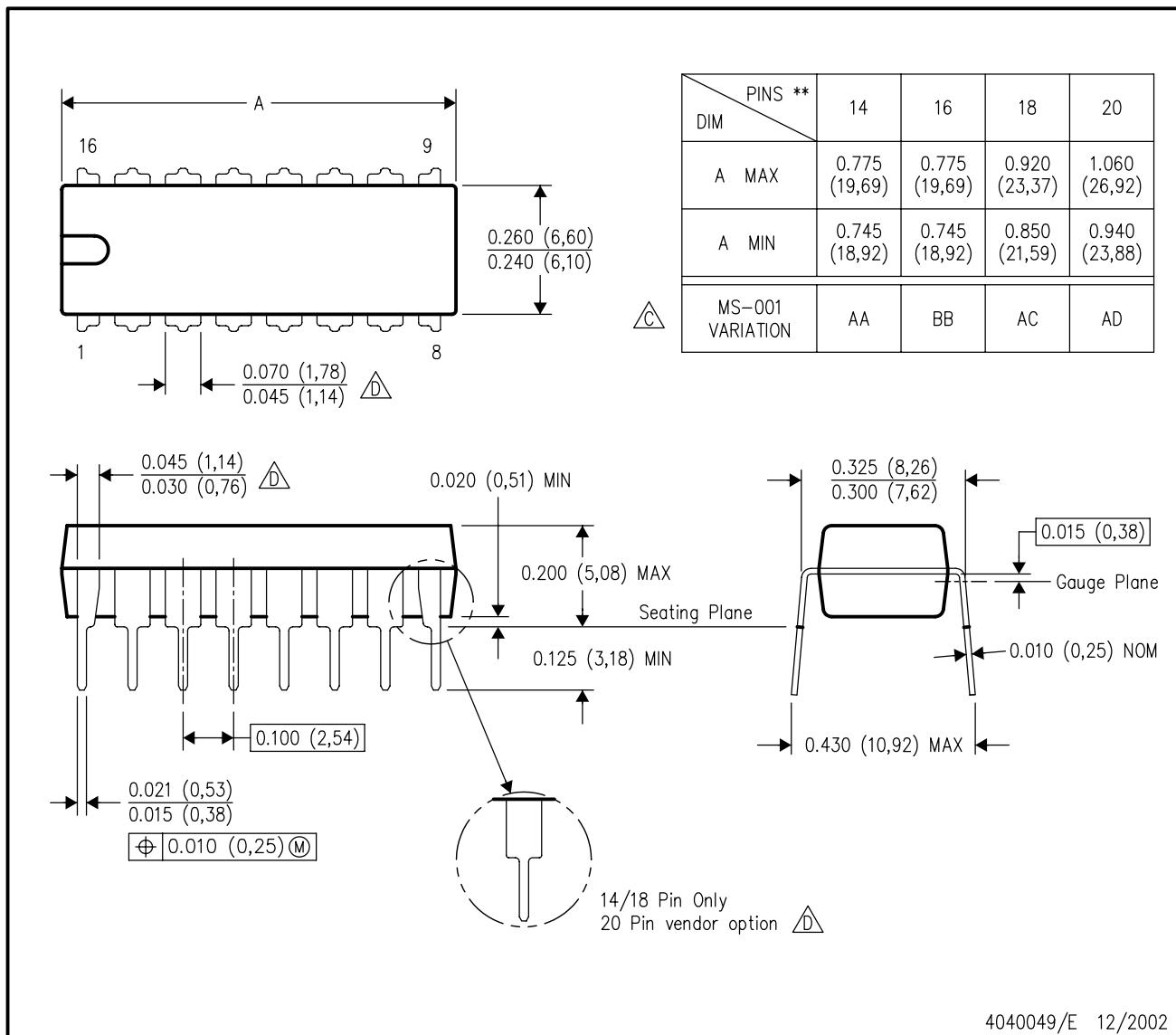


4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

Symbol C: Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

Symbol D: The 20 pin end lead shoulder width is a vendor option, either half or full width.

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ZXT6717MC
COMPLEMENTARY 15V NPN & 12V PNP LOW SATURATION TRANSISTOR
Features
NPN Transistor

- $BV_{CEO} > 15V$
- $I_c = 4.5A$ Continuous Collector Current
- Low Saturation Voltage (100mV max @ 1A)
- $R_{SAT} = 45m\Omega$ for a low equivalent On-Resistance

PNP Transistor

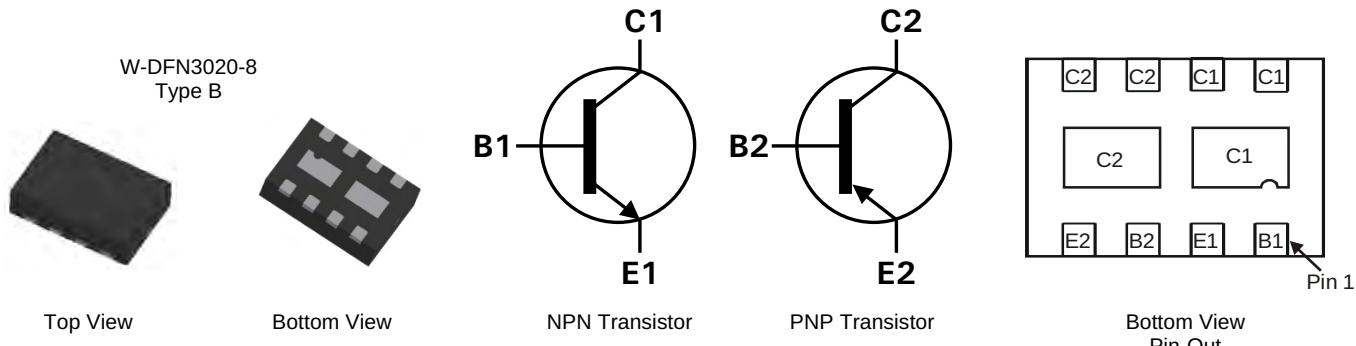
- $BV_{CEO} > -12V$
- $I_c = -4A$ Continuous Collector Current
- Low Saturation Voltage (-140mV max @ -1A)
- $R_{SAT} = 60m\Omega$ for a low equivalent On-Resistance
- h_{FE} characterized up to 12A for high current gain hold up
- Low profile 0.8mm high package for thin applications
- R_{EJA} efficient, 40% lower than SOT26
- 6mm² footprint, 50% smaller than TSOP6 and SOT26
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- PPAP capable (Note 4)

Mechanical Data

- Case: W-DFN3020-8 Type B
- Nominal package height: 0.8mm
- Case material: molded plastic. "Green" molding compound.
- UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - NiPdAu, Solderable per MIL-STD-202, Method 208 (e4)
- Weight: 0.013 grams (approximate)

Applications

- DC – DC Converters
- Charging circuits
- Power switches
- Motor control
- LED Backlighting circuits
- Portable applications


Ordering Information (Note 4 & 5)

Product	Compliance	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXT6717MCTA	AEC-Q101	DA1	7	8	3,000
ZXT6717MCQTA	Automotive	DA1	7	8	3,000

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive, AEC-Q101 and standard products are electrically and thermally the same, except where specified.
 5. For packaging details, go to our website at <http://www.diodes.com>

Marking Information

DA1 = Product type Marking Code
Dot denotes Pin 1

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

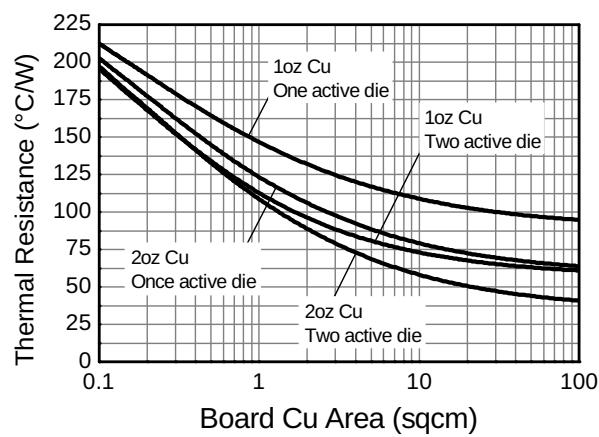
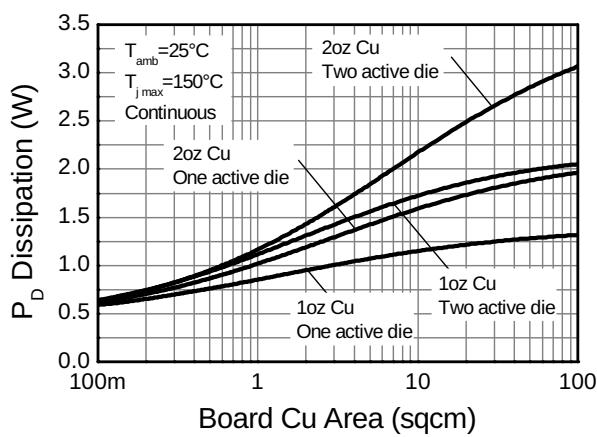
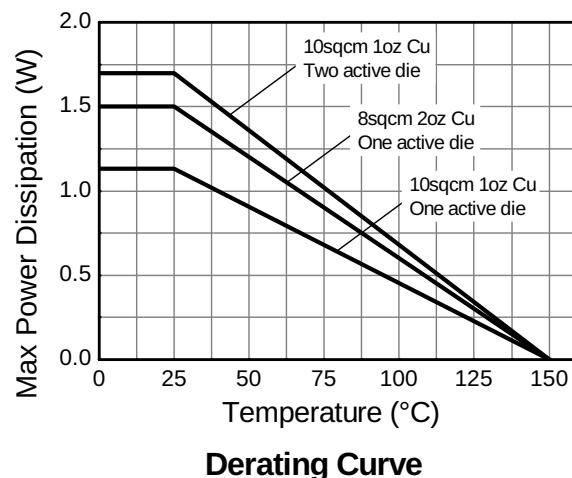
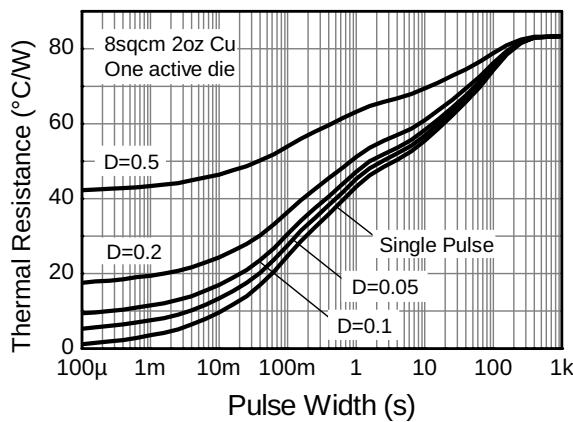
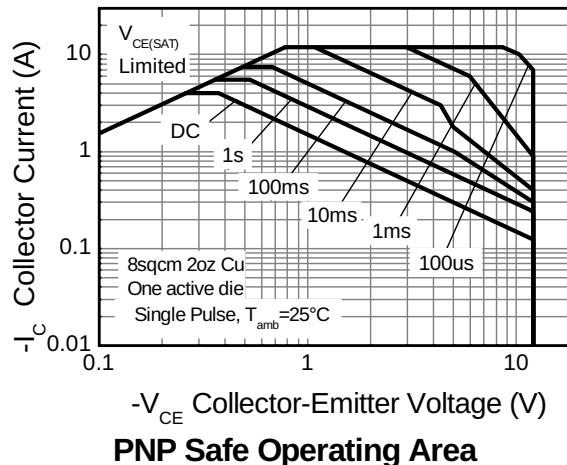
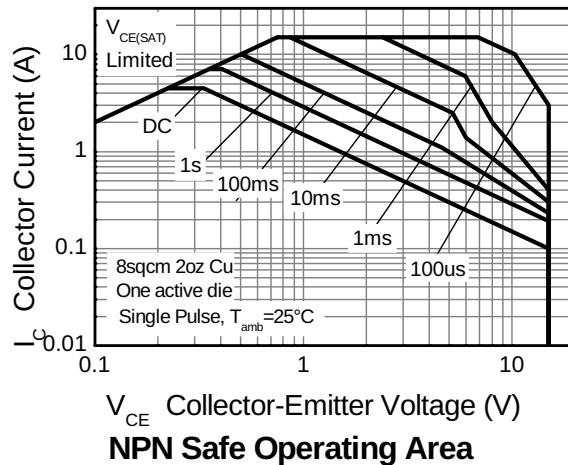
Characteristic		Symbol	NPN	PNP	Unit
Collector-Base Voltage		V_{CBO}	40	-20	V
Collector-Emitter Voltage		V_{CEO}	15	-12	V
Emitter-Base Voltage		V_{EBO}	7	-7	V
Peak Pulse Current		I_{CM}	15	-12	A
Continuous Collector Current	(Notes 6 & 9)	I_C	4.5	-4	A
	(Notes 7 & 9)		5	-4.45	
Base Current		I_B	1		A

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	NPN	PNP	Unit
Power Dissipation Linear Derating Factor	P_D	1.5		W mW/ $^\circ\text{C}$
		12		
		2.45		
		19.6		
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	1.13		$^\circ\text{C}/\text{W}$
		8		
		1.7		
		13.6		
Thermal Resistance, Junction to Lead	$R_{\theta JL}$	83.3		$^\circ\text{C}/\text{W}$
		51.0		
		111		
		73.5		
Operating and Storage Temperature Range	T_J, T_{STG}	17.1	-55 to +150	$^\circ\text{C}$

- Notes:
- 6. For a dual device surface mounted on 28mm x 28mm (8cm^2) FR4 PCB with high coverage of single sided 2 oz copper, in still air conditions; the device is measured when operating in a steady-state condition. The heatsink is split in half with the exposed collector pads connected to each half.
 - 7. Same as note (6), except the device is measured at $t < 5$ sec.
 - 8. Same as note (6), except the device is surface mounted on 31mm x 31mm (10cm^2) FR4 PCB with high coverage of single sided 1oz copper.
 - 9. For a dual device with one active die.
 - 10. For dual device with 2 active die running at equal power.
 - 11. Thermal resistance from junction to solder-point (on the exposed collector pads).

Thermal Characteristics and Derating Information

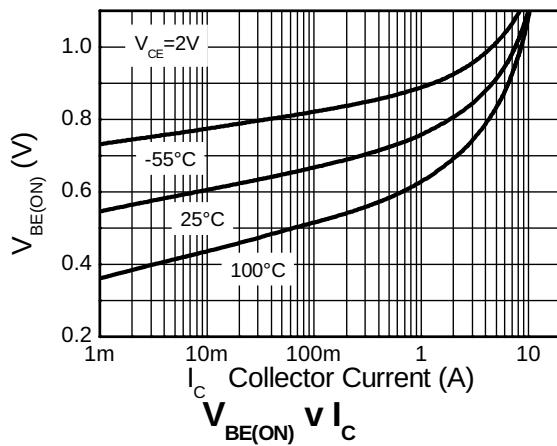
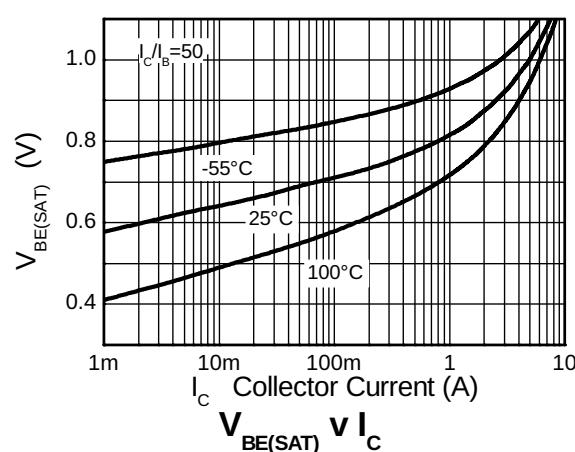
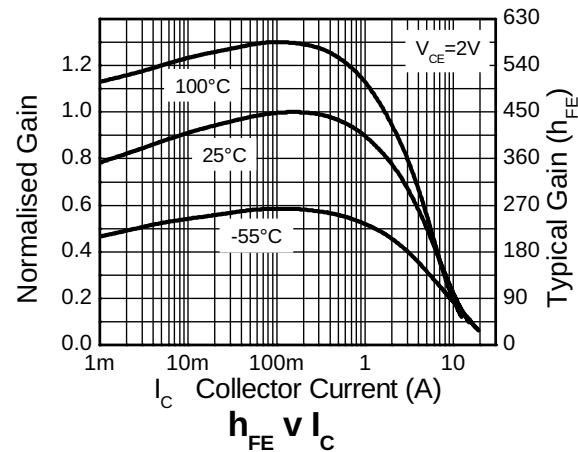
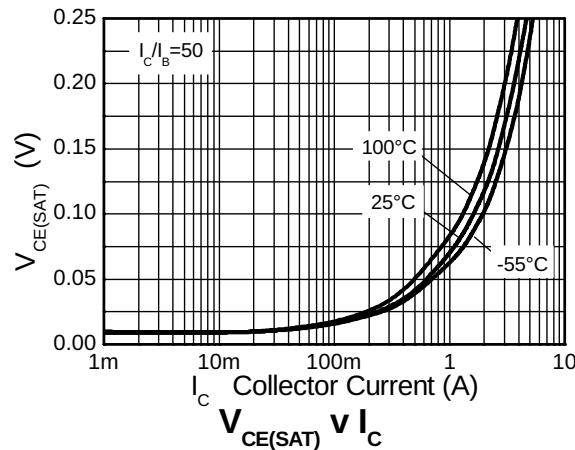
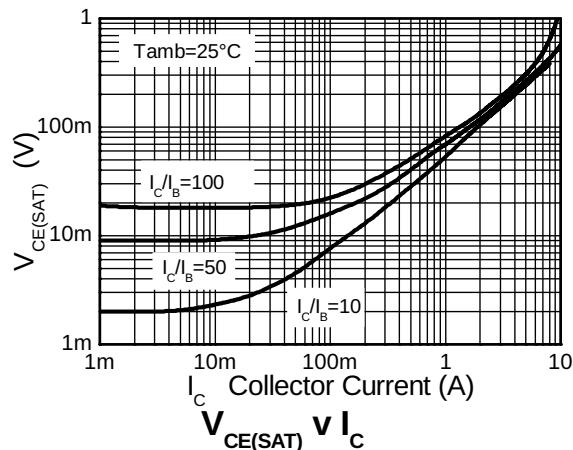


NPN - Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV _{CBO}	40	70	-	V	I _C = 100µA
Collector-Emitter Breakdown Voltage (Note 12)	BV _{CEO}	15	18	-	V	I _C = 10mA
Emitter-Base Breakdown Voltage	BV _{EBO}	7	8.2	-	V	I _E = 100µA
Collector Cutoff Current	I _{CBO}	-	-	100	nA	V _{CB} = 30V
Emitter Cutoff Current	I _{EBO}	-	-	100	nA	V _{EB} = 6V
Collector Emitter Cutoff Current	I _{CES}	-	-	100	nA	V _{CE} = 12V
Static Forward Current Transfer Ratio (Note 12)	h _{FE}	200	415	-		I _C = 10mA, V _{CE} = 2V
		300	450	-		I _C = 200mA, V _{CE} = 2V
		200	320	-		I _C = 3A, V _{CE} = 2V
		150	240	-		I _C = 5A, V _{CE} = 2V
		-	80	-		I _C = 12A, V _{CE} = 2V
Collector-Emitter Saturation Voltage (Note 12)	V _{CE(sat)}	-	8	14		I _C = 0.1A, I _B = 10mA
		-	70	100		I _C = 1A, I _B = 10mA
		-	165	200	mV	I _C = 3A, I _B = 50mA
		-	240	310		I _C = 4.5A, I _B = 50mA
		-	200	-		I _C = 4.5A, I _B = 100mA
Base-Emitter Turn-On Voltage (Note 12)	V _{BE(on)}	-	0.88	0.96	V	I _C = 4.5A, V _{CE} = 2V
Base-Emitter Saturation Voltage (Note 12)	V _{BE(sat)}	-	0.94	1.05	V	I _C = 4.5A, I _B = 50mA
Output Capacitance	C _{obo}	-	30	40	pF	V _{CB} = 10V, f = 1MHz
Transition Frequency	f _T	80	120	-	MHz	V _{CE} = 10V, I _C = 50mA, f = 100MHz
Turn-on Time	t _{on}	-	120	-	ns	V _{CC} = 10V, I _C = 1A
Turn-off Time	t _{off}	-	160	-	ns	I _{B1} = I _{B2} = 10mA

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300µs. Duty cycle ≤ 2%.

NPN – Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



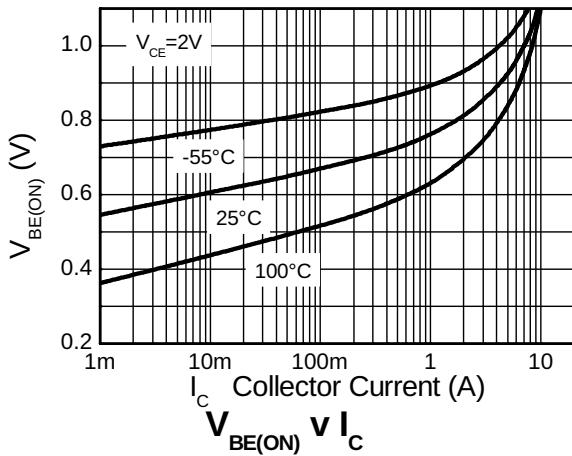
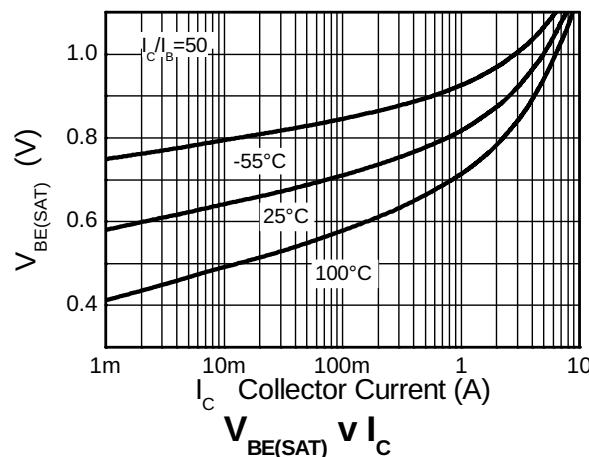
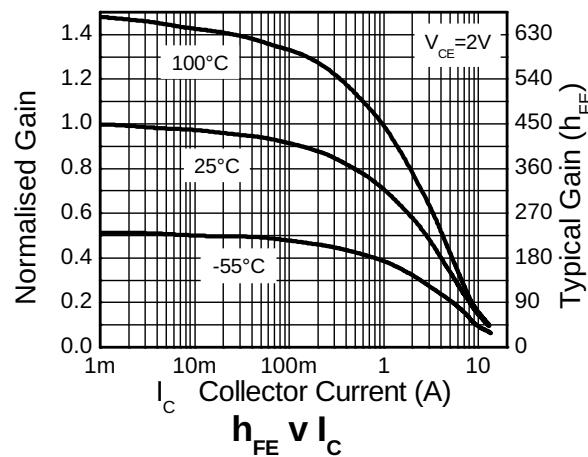
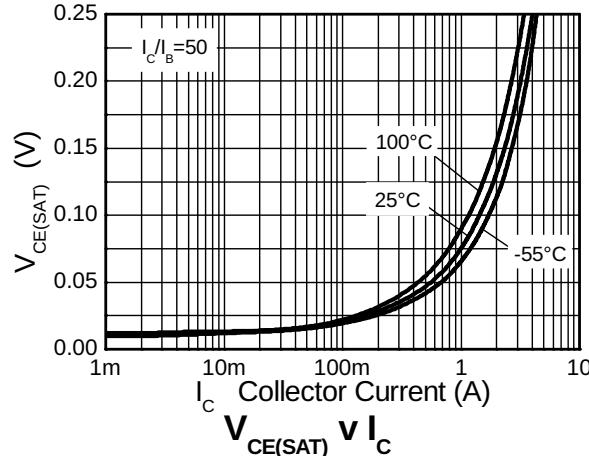
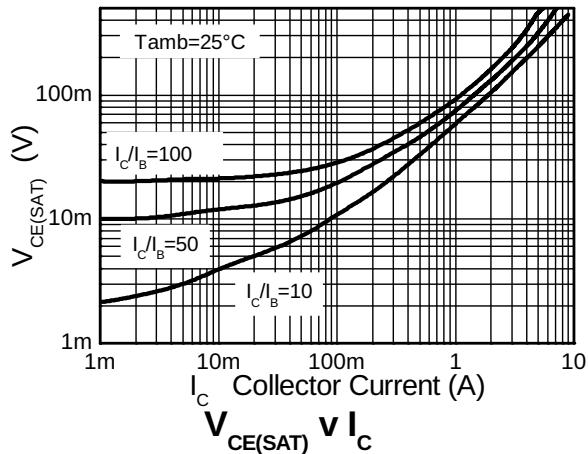
ZXT_C6717MC

PNP - Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV _{CBO}	-20	-35	-	V	I _C = -100µA
Collector-Emitter Breakdown Voltage (Note 12)	BV _{CEO}	-12	-25	-	V	I _C = -10mA
Emitter-Base Breakdown Voltage	BV _{EBO}	-7	-8.5	-	V	I _E = -100µA
Collector Cutoff Current	I _{CBO}	-	-	-100	nA	V _{CB} = -16V
Emitter Cutoff Current	I _{EBO}	-	-	-100	nA	V _{EB} = -6V
Collector Emitter Cutoff Current	I _{CES}	-	-	-100	nA	V _{CES} = -10V
Static Forward Current Transfer Ratio (Note 12)	h _{FE}	300	475	-		I _C = -10mA, V _{CE} = -2V
		300	450	-		I _C = -100mA, V _{CE} = -2V
		180	275	-		I _C = -2.5A, V _{CE} = -2V
		60	100	-		I _C = -8A, V _{CE} = -2V
		45	70	-		I _C = -10A, V _{CE} = -2V
Collector-Emitter Saturation Voltage (Note 12)	V _{CE(sat)}	-	-10	-17		I _C = -0.1A, I _B = -10mA
		-	-100	-140		I _C = -1A, I _B = -10mA
		-	-100	-150	mV	I _C = -1.5A, I _B = -50mA
		-	-195	-300		I _C = -3A, I _B = -50mA
		-	-240	-310		I _C = -4A, I _B = -150mA
Base-Emitter Turn-On Voltage (Note 12)	V _{BE(on)}	-	-0.87	-0.96	V	I _C = -4A, V _{CE} = -2V
Base-Emitter Saturation Voltage (Note 12)	V _{BE(sat)}	-	-0.97	-1.07	V	I _C = -4A, I _B = -150mA
Output Capacitance	C _{obo}	-	21	30	pF	V _{CB} = -10V, f = 1MHz
Transition Frequency	f _T	100	110	-	MHz	V _{CE} = -10V, I _C = -50mA, f = 100MHz
Turn-on Time	t _{on}	-	70	-	ns	V _{CC} = -6V, I _C = -2A
Turn-off Time	t _{off}	-	130	-	ns	I _{B1} = I _{B2} = -50mA

Notes: 12. Measured under pulsed conditions. Pulse width ≤ 300µs. Duty cycle ≤ 2%.

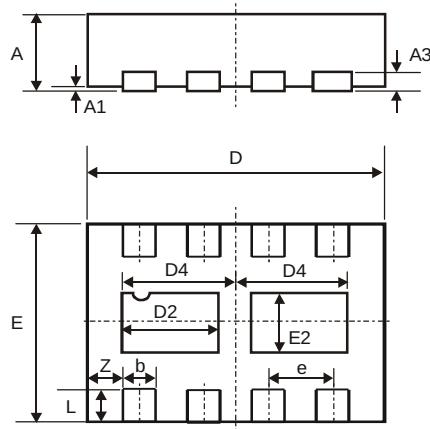
PNP – Typical Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)



ZXT_C6717MC

Package Outline Dimensions

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

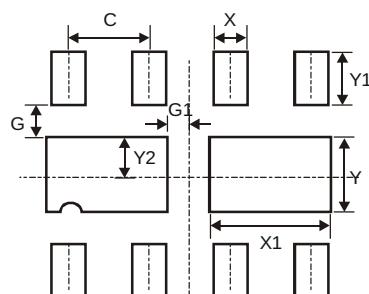


W-DFN3020-8 Type B			
Dim	Min	Max	Typ
A	0.77	0.83	0.80
A1	0	0.05	0.02
A3	-	-	0.15
b	0.25	0.35	0.30
D	2.95	3.075	3.00
D2	0.82	1.02	0.92
D4	1.01	1.21	1.11
e	-	-	0.65
E	1.95	2.075	2.00
E2	0.43	0.63	0.53
L	0.25	0.35	0.30
Z	-	-	0.375

All Dimensions in mm

Suggested Pad Layout

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
C	0.650
G	0.285
G1	0.090
X	0.400
X1	1.120
Y	0.730
Y1	0.500
Y2	0.365

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1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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General Purpose Capacitors

GPR Series



Features

- Wide CV value range for general purpose
- Safely vent construction products, GPR series are guaranteed 2,000 hours at 85°C

Specifications

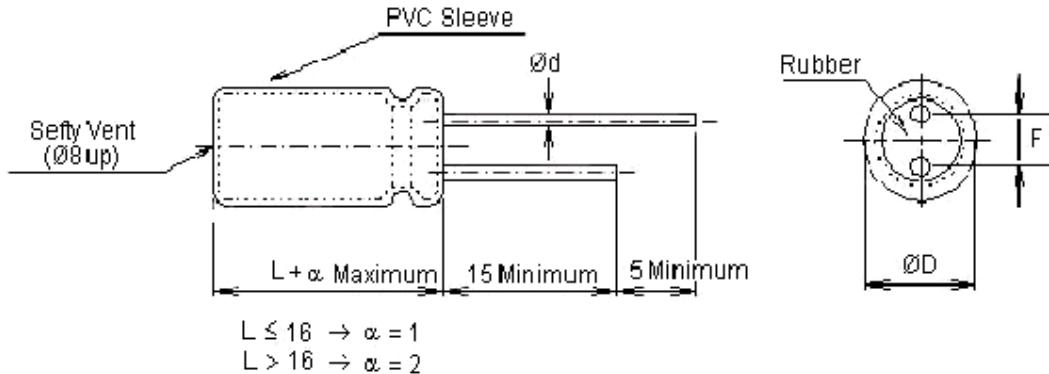
Item	Performance																															
Operating Temperature Range	-40°C to +85°C																															
Rated Working Voltage Range	10 to 100V DC																															
Nominal Capacitance Range	0.1 to 22,000μF																															
Capacitance Tolerance	± 20% (at +20°C, 120 Hz)																															
Leakage Current	$I = 0.01CV$ or $3 (\mu\text{A})$ Max. I : Leakage Current(μA) Which ever is greater after 3 mins. C : Rated Capacitance(μF) V : Working Voltage(v)																															
Dissipation Factor ($\tan \delta$) (120Hz \ +20°C)	<table border="1"><tr><th>Working voltage (V)</th><td>10</td><td>16</td><td>25</td><td>35</td><td>50</td><td>63</td><td>100</td></tr><tr><th>$\tan \delta$ Max.</th><td>0.2</td><td>0.17</td><td>0.15</td><td>0.12</td><td>0.1</td><td>0.09</td><td>0.08</td></tr></table> Add 0.02 per 1,000 μF for more than 1,000 μF								Working voltage (V)	10	16	25	35	50	63	100	$\tan \delta$ Max.	0.2	0.17	0.15	0.12	0.1	0.09	0.08								
Working voltage (V)	10	16	25	35	50	63	100																									
$\tan \delta$ Max.	0.2	0.17	0.15	0.12	0.1	0.09	0.08																									
Ripple Current	Refer to standard products table (120Hz, +85°C) Correction factor for frequency. <table border="1"><tr><th>Frequency (Hz)</th><td>50 / 60</td><td>120</td><td>1 K</td><td>10 K</td></tr><tr><th>Correction Factor (Multiplier)</th><td>0.7</td><td>1</td><td>1.3</td><td>1.7</td></tr></table>								Frequency (Hz)	50 / 60	120	1 K	10 K	Correction Factor (Multiplier)	0.7	1	1.3	1.7														
Frequency (Hz)	50 / 60	120	1 K	10 K																												
Correction Factor (Multiplier)	0.7	1	1.3	1.7																												
Characteristics at High and Low Temperature (Stability at 120 Hz)	<table border="1"><tr><th>Working voltage (V)</th><td>10</td><td>16</td><td>25</td><td>35</td><td>50</td><td>63</td><td>100</td></tr><tr><th>-25°C / +20°C</th><td>3</td><td>2</td><td>2</td><td>2</td><td>2</td><td>2</td><td>2</td></tr><tr><th>-40°C / +20°C</th><td>6</td><td>4</td><td>4</td><td>3</td><td>3</td><td>3</td><td>3</td></tr></table> For capacitance value > 1,000 μF , Add 0.5 per another 1,000 μF for -25°C / +25°C. Add 1 per another 1,000 μF for -40°C / +20°C.								Working voltage (V)	10	16	25	35	50	63	100	-25°C / +20°C	3	2	2	2	2	2	2	-40°C / +20°C	6	4	4	3	3	3	3
Working voltage (V)	10	16	25	35	50	63	100																									
-25°C / +20°C	3	2	2	2	2	2	2																									
-40°C / +20°C	6	4	4	3	3	3	3																									
High Temperature Loading	After 2,000 hours application of DC rated working voltage at +85°C, The capacitor shall meet the following limits: Post test requirements at +20°C. <table border="1"><tr><td>Leakage current</td><td>≤ the initial specified value</td></tr><tr><td>Capacitance change</td><td>≤ ±20% of initial measured value</td></tr><tr><td>Dissipation factor ($\tan \delta$)</td><td>≤ 150% of initial specified value</td></tr></table>								Leakage current	≤ the initial specified value	Capacitance change	≤ ±20% of initial measured value	Dissipation factor ($\tan \delta$)	≤ 150% of initial specified value																		
Leakage current	≤ the initial specified value																															
Capacitance change	≤ ±20% of initial measured value																															
Dissipation factor ($\tan \delta$)	≤ 150% of initial specified value																															
Shelf Life	After storage for 500 hours at +85°C with no voltage applied. Post test requirements at +20°C same limits as high temperature loading.																															

General Purpose Capacitors

GPR Series

multicomp^m

Diagram of Dimensions



Dimensions : Millimetres

ØD (+0.5 Max.)	5	6.3	8	10	13	16	18	22	25
F (± 0.5)	2	2.5	3.5	5	5	7.5	7.5	10	12
Ød (± 0.02)	0.5	0.5	0.6	0.6	0.6	0.8	0.8	0.8	0.8

Case Size Table

W V (SV) µF	10 (13)	16 (20)	25 (32)	35 (44)	50 (63)	63 (79)	100 (125)				
0.1	-	-	-	→	5 × 11	-	5 × 11				
0.22	-	-	-	→		-					
0.33	-	-	-	→		-					
0.47	-	-	-	→		-					
1	-	-	-	→		-					
2.2	-	-	-	→		-					
3.3	-	-	-	→		-					
4.7	-	-	-	→		-					
10	-	→	5 × 11	5 × 11		5 × 11	6.3 × 11				
22	-	→				6.3 × 11	8 × 11				
33	→	5 × 11				10 × 13	10 × 13				
47	→					8 × 11	10 × 16				
100	5 × 11	6.3 × 11	6.3 × 11	8 × 11	8 × 11	10 × 13	13 × 21				
220	6.3 × 11		8 × 11	10 × 13	10 × 16	10 × 21	16 × 26				
330			10 × 13	10 × 16	10 × 21	13 × 21	16 × 26				
470	8 × 11		10 × 16		13 × 21	13 × 26	16 × 32				
1,000	10 × 13	10 × 16	10 × 21	13 × 21	16 × 26	16 × 32	18 × 42				

General Purpose Capacitors

GPR Series



W V (SV) µF	10 (13)	16 (20)	25 (32)	35 (44)	50 (63)	63 (79)	100 (125)
2,200	10 × 21	13 × 21	13 × 26	16 × 26	16 × 36	18 × 36	25 × 50
3,300	13 × 21	13 × 26	16 × 26	16 × 36	18 × 36	22 × 42	-
4,700	13 × 26	16 × 26	16 × 36	18 × 36	22 × 41	25 × 50	-
6,800	16 × 26	16 × 36	18 × 36	22 × 41	25 × 50	30 × 46	-
8,200	18 × 36	18 × 42	22 × 46	22 × 50	30 × 46	-	-
10,000	18 × 32	18 × 36	22 × 41	25 × 50	-	-	-
15,000	18 × 36	22 × 50	25 × 50	-	-	-	-
22,000	22 × 50	25 × 50	30 × 46	-	-	-	-
8,200	18 × 36	18 × 42	22 × 46	22 × 50	30 × 46	-	-
10,000	18 × 32	18 × 36	22 × 41	25 × 50		-	-
15,000	18 × 36	22 × 50	25 × 50	-	-	-	-
22,000	22 × 50	25 × 50	30 × 46	-	-	-	-

Dimensions : Millimetres

- All blank voltage on sleeve marking is the same voltage as the " → " point to.

Permissible Ripple Current

Maximum Ripple Current : mA (rms) (at 85°C 120 Hz)

W V (SV) µF	10 (13)	16 (20)	25 (32)	35 (44)	50 (63)	63 (79)	100 (125)
0.1-0.47	-	-	-	-	8	-	10
1	-	-	-	-	13	-	16
2.2	-	-	-	-	21	-	27
3.3	-	-	-	-	30	-	40
4.7	-	-	30	35	40	40	45
10	-	45	45	50	60	65	75
22	60	60	70	80	90	110	130
33	75	85	95	105	120	140	170
47	90	100	120	135	150	180	230
100	140	170	180	220	250	280	380
150	220	240	310	350	400	450	550
220	240	280	320	380	430	490	680
330	320	360	420	480	540	680	800
470	400	460	540	620	750	880	1,000
560	500	580	670	770	880	1,050	1,170
680	570	660	760	870	1,000	1,160	1,330
820	640	740	850	970	1,130	1,300	1,500

General Purpose Capacitors

GPR Series



W V (SV) μF	10 (13)	16 (20)	25 (32)	35 (44)	50 (63)	63 (79)	100 (125)
1,000	660	760	900	1,040	1,260	1,400	1,970
2,200	1,050	1,250	1,460	1,700	1,900	2,460	3,390
3,300	1,340	1,620	1,800	2,060	2,180	3,270	-
4,700	1,720	1,960	2,150	2,280	3,380	3,800	-
6,800	2,060	2,250	2,400	3,490	4,110	4,500	-
8,200	2,520	2,870	3,420	3,780	4,150	-	-
10,000	2,640	2,980	3,710	4,170	4,300	-	-
15,000	3,120	3,890	4,270	-	-	-	-
22,000	4,010	4,410	4,500	-	-	-	-

Dimensions : Millimetres

Part Number Table

Description	Part Number	Description	Part Number
CAPACITOR, 100uF, 10V	MCGPR10V107M5X11	CAPACITOR, 47UF, 25V	MCGPR25V476M5X11
CAPACITOR, 220uF, 10V	MCGPR10V227M6.3X11	CAPACITOR, 100UF, 25V	MCGPR25V107M6.3X11
CAPACITOR, 470uF, 10V	MCGPR10V477M8X11	CAPACITOR, 220UF, 25V	MCGPR25V227M8X11
CAPACITOR, 1000uF, 10V	MCGPR10V108M8X14	CAPACITOR, 330UF, 25V	MCGPR25V337M8X14
CAPACITOR, 2200uF, 10V	MCGPR10V228M10X21	CAPACITOR, 470UF, 25V	MCGPR25V477M10X16
CAPACITOR, 4700uF, 10V	MCGPR10V478M13X26	CAPACITOR, 1000UF, 25V	MCGPR25V108M10X21
CAPACITOR, 10UF, 16V	MCGPR16V106M5X11	CAPACITOR, 2200UF, 25V	MCGPR25V228M13X26
CAPACITOR, 22UF, 16V	MCGPR16V226M5X11	CAPACITOR, 3300UF, 25V	MCGPR25V338M16X26
CAPACITOR, 33uF, 16V	MCGPR16V336M5X11	CAPACITOR, 4700UF, 25V	MCGPR25V478M16X32
CAPACITOR, 47UF, 16V	MCGPR16V476M5X11	CAPACITOR, 4.7UF, 35V	MCGPR35V475M5X11
CAPACITOR, 100UF, 16V	MCGPR16V107M6.3X11	CAPACITOR, 10UF, 35V	MCGPR35V106M5X11
CAPACITOR, 220UF, 16V	MCGPR16V227M6.3X11	CAPACITOR, 22UF, 35V	MCGPR35V226M5X11
CAPACITOR, 330UF, 16V	MCGPR16V337M8X11	CAPACITOR, 33UF, 35V	MCGPR35V336M5X11
CAPACITOR, 470UF, 16V	MCGPR16V477M8X11	CAPACITOR, 47UF, 35V	MCGPR35V476M6.3X11
CAPACITOR, 1000UF, 16V	MCGPR16V108M10X16	CAPACITOR, 100UF, 35V	MCGPR35V107M8X11
CAPACITOR, 2200UF, 16V	MCGPR16V228M13X21	CAPACITOR, 220UF, 35V	MCGPR35V227M10X13
CAPACITOR, 3300UF, 16V	MCGPR16V338M13X26	CAPACITOR, 330UF, 35V	MCGPR35V337M10X16
CAPACITOR, 4700UF, 16V	MCGPR16V478M16X26	CAPACITOR, 470UF, 35V	MCGPR35V477M10X21
CAPACITOR, 10UF, 25V	MCGPR25V106M5X11	CAPACITOR, 1000UF, 35V	MCGPR35V108M13X21
CAPACITOR, 22UF, 25V	MCGPR25V226M5X11	CAPACITOR, 2200UF, 35V	MCGPR35V228M16X32
CAPACITOR, 33UF, 25V	MCGPR25V336M5X11	CAPACITOR, 3300UF, 35V	MCGPR35V338M16X32

General Purpose Capacitors

GPR Series



Part Number Table

Description	Part Number
CAPACITOR, 4700UF, 35V	MCGPR35V478M18X36
CAPACITOR, 0.47UF, 50V	MCGPR50V474M5X11
CAPACITOR, 1UF, 50V	MCGPR50V105M5X11
CAPACITOR, 2.2UF, 50V	MCGPR50V225M5X11
CAPACITOR, 3.3UF, 50V	MCGPR50V335M5X11
CAPACITOR, 4.7UF, 50V	MCGPR50V475M5X11
CAPACITOR, 10UF, 50V	MCGPR50V106M5X11
CAPACITOR, 22UF, 50V	MCGPR50V226M5X11
CAPACITOR, 33UF, 50V	MCGPR50V336M6.3X11
CAPACITOR, 47UF, 50V	MCGPR50V476M6.3X11
CAPACITOR, 100UF, 50V	MCGPR50V107M8X11
CAPACITOR, 220UF, 50V	MCGPR50V227M10X16
CAPACITOR, 330UF, 50V	MCGPR50V337M10X21
CAPACITOR, 470UF, 50V	MCGPR50V477M13X21
CAPACITOR, 1000UF, 50V	MCGPR50V108M16X26
CAPACITOR, 2200UF, 50V	MCGPR50V228M16X32
CAPACITOR, 3300UF, 50V	MCGPR50V338M18X33
CAPACITOR, 4700UF, 50V	MCGPR50V478M22X41
CAPACITOR, 1UF, 63V	MCGPR63V105M5X11
CAPACITOR, 2.2UF, 63V	MCGPR63V225M5X11

Description	Part Number
CAPACITOR, 4.7UF, 63V	MCGPR63V475M5X11
CAPACITOR, 10UF, 63V	MCGPR63V106M5X11
CAPACITOR, 22UF, 63V	MCGPR63V226M6.3X11
CAPACITOR, 47UF, 63V	MCGPR63V476M8X11
CAPACITOR, 100UF, 63V	MCGPR63V107M10X13
CAPACITOR, 220UF, 63V	MCGPR63V227M10X21
CAPACITOR, 470UF, 63V	MCGPR63V477M13X26
CAPACITOR, 1000UF, 63V	MCGPR63V108M16X32
CAPACITOR, 2200UF, 63V	MCGPR63V228M18X36
CAPACITOR, 4700UF, 63V	MCGPR63V478M25X42
CAPACITOR, 1UF, 100V	MCGPR100V105M5X11
CAPACITOR, 2.2UF, 100V	MCGPR100V225M5X11
CAPACITOR, 4.7UF, 100V	MCGPR100V475M5X11
CAPACITOR, 10UF, 100V	MCGPR100V106M6.3X11
CAPACITOR, 22UF, 100V	MCGPR100V226M8X11
CAPACITOR, 47UF, 100V	MCGPR100V476M10X16
CAPACITOR, 100UF, 100V	MCGPR100V107M13X21
CAPACITOR, 220UF, 100V	MCGPR100V227M16X26
CAPACITOR, 470UF, 100V	MCGPR100V477M16X32

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SN74LVC1G19 1-of-2 Decoder and Demultiplexer

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10-µA Maximum I_{CC}
- ±24-mA Output Drive at 3.3 V
- V_{OLP} (Output Ground Bounce)
<0.8 V Typical at V_{CC} = 3.3 V, T_A = 25°C
- V_{OHV} (Output V_{OH} Undershoot)
>2 V Typical at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray® Players and Home Theater
- MP3 Players/Recorders
- Personal Digital Assistants (PDAs)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD/Digital and High-Definition (HDTVs)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

This decoder/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G19 device is a 1-of-2 decoder / demultiplexer. When Ē input is high, the decoder will be disabled and both outputs will be high. When Ē input is low, the A input selects which output will be low.

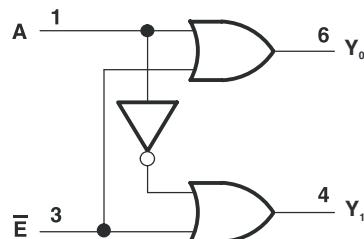
This device is fully specified for partial-power-down applications using I_{off}.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G19DBV	SOT-23 (6)	2.9 mm × 1.6 mm
SN74LVC1G19DCK	SC70 (6)	2.0 mm × 1.25 mm
SN74LVC1G19DRL	SOT (6)	1.6 mm × 1.2 mm
SN74LVC1G19DRY	SON (6)	1.45 mm × 1.0 mm
SN74LVC1G19YZP	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

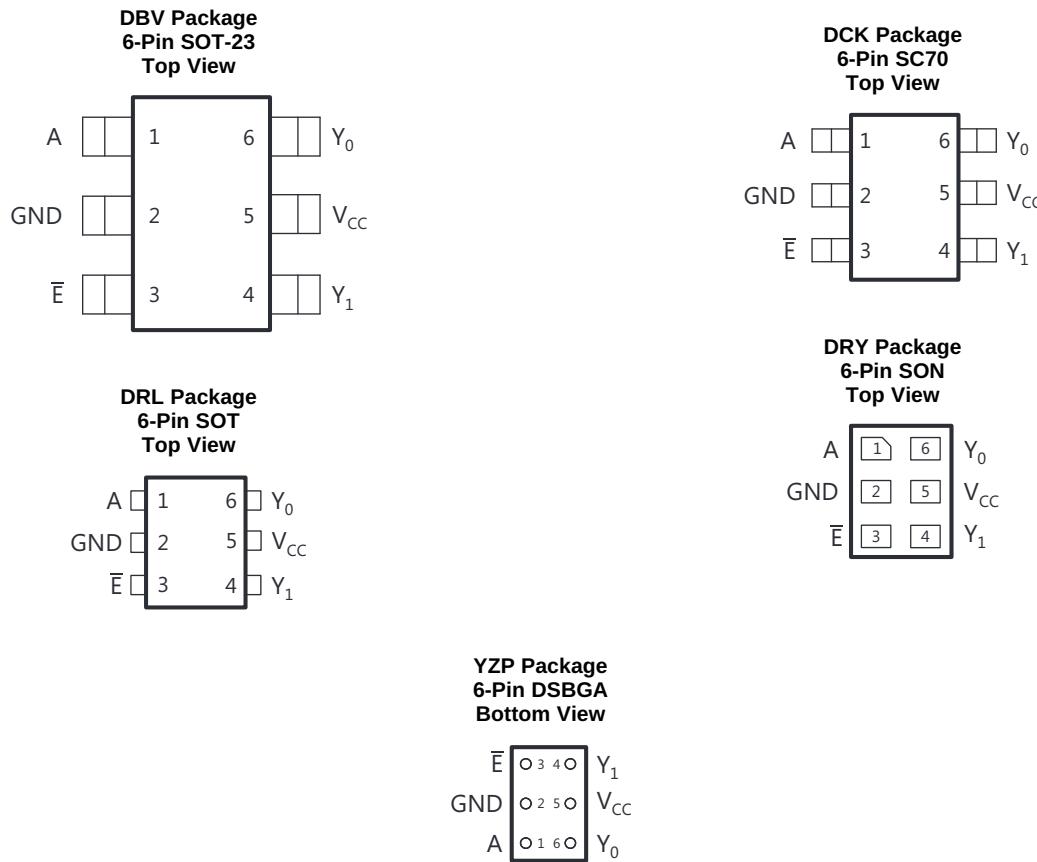
1 Features	1	8.1 Overview	10
2 Applications	1	8.2 Functional Block Diagram	10
3 Description	1	8.3 Feature Description	10
4 Revision History.....	2	8.4 Device Functional Modes.....	10
5 Pin Configuration and Functions	3	9 Application and Implementation	11
6 Specifications.....	4	9.1 Application Information.....	11
6.1 Absolute Maximum Ratings	4	9.2 Typical Application	11
6.2 ESD Ratings.....	4	10 Power Supply Recommendations	12
6.3 Recommended Operating Conditions	5	11 Layout.....	12
6.4 Thermal Information	5	11.1 Layout Guidelines	12
6.5 Electrical Characteristics.....	6	11.2 Layout Example	12
6.6 Switching Characteristics, $C_L = 15 \text{ pF}$	6	12 Device and Documentation Support	13
6.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or 50 pF	6	12.1 Community Resources.....	13
6.8 Operating Characteristics.....	6	12.2 Trademarks	13
6.9 Typical Characteristics	7	12.3 Electrostatic Discharge Caution	13
7 Parameter Measurement Information	8	12.4 Glossary	13
8 Detailed Description	10	13 Mechanical, Packaging, and Orderable Information	13

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2012) to Revision G	Page
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table.	1
• Updated I_{off} in <i>Features</i>	1

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		I/O	DESCRIPTION
NAME	NO.		
A	1	I	Address input, selects which output goes low.
GND	2	—	Ground
\bar{E}	3	I	Enable input, active low
Y ₁	4	O	Output 1, low when selected by A high and \bar{E} low
V _{CC}	5	—	Power pin
Y ₀	6	O	Output 0, low when selected by A low and \bar{E} low

(1) See mechanical drawings for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	6.5	V
V_I	Input voltage ⁽²⁾	-0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V_O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 100	mA
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000	V
	Charged-Device Model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 1000	
	Machine model	± 200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.8		
		V _{CC} = 4.5 V to 5.5 V	0.3 × V _{CC}		
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature		-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G19					UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	YZP (DSBGA)	
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
R _{θJA} Junction-to-ambient thermal resistance	165	259	142	234	123	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	1.65 V to 5.5 V	V _{CC}	-0.1		V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -8 mA	2.3 V		1.9		
	I _{OH} = -16 mA	3 V		2.4		
	I _{OH} = -24 mA			2.3		
	I _{OH} = -32 mA	4.5 V		3.8		
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V		0.1		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 8 mA	2.3 V		0.3		
	I _{OL} = 16 mA	3 V		0.4		
	I _{OL} = 24 mA			0.55		
	I _{OL} = 32 mA	4.5 V		0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1	µA	
I _{off}	V _I or V _O = 5.5 V	0		±10	µA	
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10	µA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500	µA	
C _I	V _I = V _{CC} or GND	3.3 V		3.5	pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics, C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or Ē	Y	2.5	16.1	1.5	5.9	1	4	0.5	2.8	ns

6.7 Switching Characteristics, C_L = 30 pF or 50 pF

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or Ē	Y	3.2	16.1	1.5	6.5	1.1	5.2	0.5	3.9	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V		V _{CC} = 2.5 V		V _{CC} = 3.3 V		V _{CC} = 5 V		UNIT
		TYP		TYP		TYP		TYP		
C _{pd}	Power dissipation capacitance f = 10 MHz	15.5		16		16		18		pF

6.9 Typical Characteristics

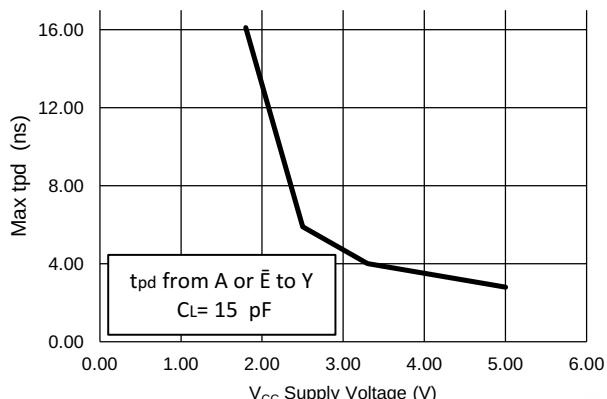


Figure 1. Time Propagation Delay vs V_{CC} , $C_L = 15 \text{ pF}$

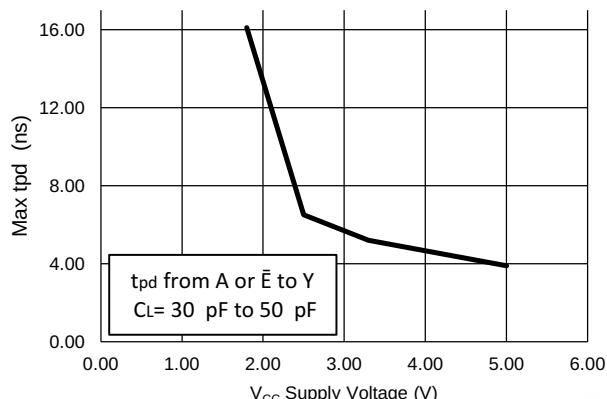
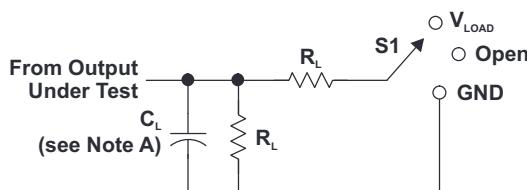


Figure 2. Time Propagation Delay vs V_{CC} , $C_L = 30 \text{ pF}$ or 50 pF

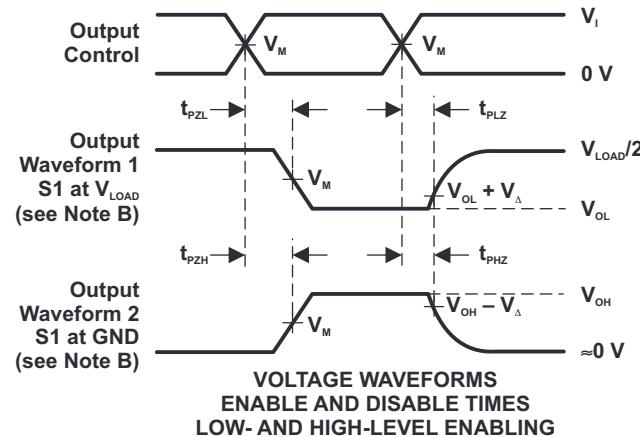
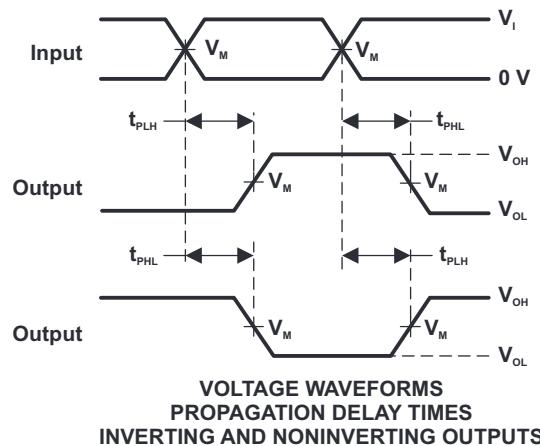
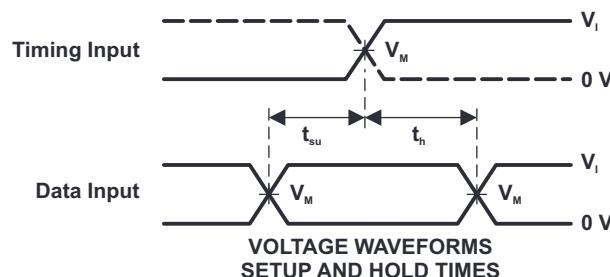
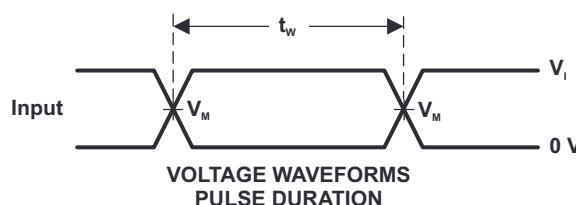
7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

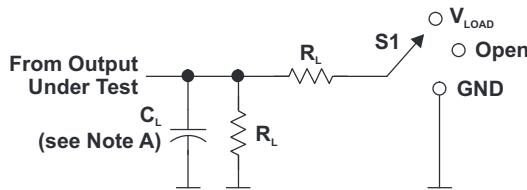
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_I/t_I					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 MΩ	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 MΩ	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

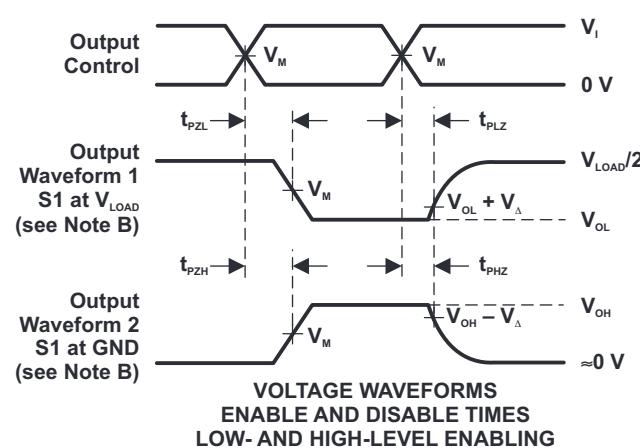
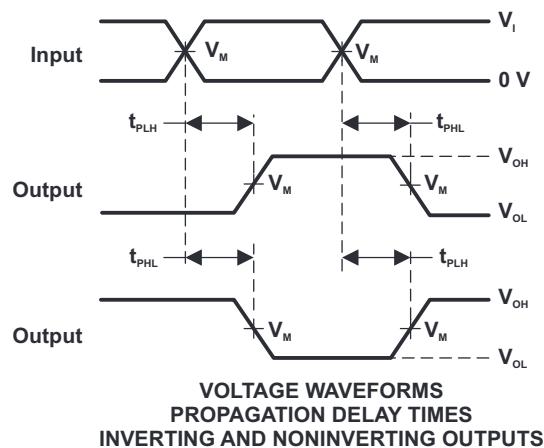
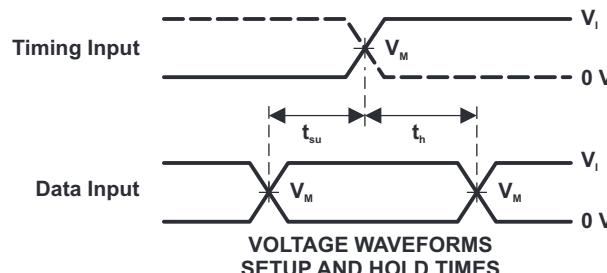
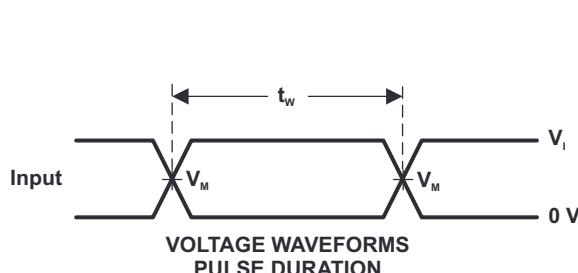
Parameter Measurement Information (continued)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_o = 50\text{ }\Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

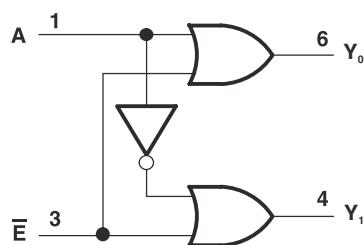
This decoder/demultiplexer is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G19 device is a 1-of-2 decoder/demultiplexer. This device decodes the 1-bit address on input A and places a logic low on the matching address output, Y_0 or Y_1 , when the enable (\bar{E}) input signal is low.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

8.2 Functional Block Diagram



8.3 Feature Description

SN74LVC1G19 is available in NanoFree package. NanoFree is a major breakthrough in IC packaging concepts, it is a bare die package developed for applications that require the smallest possible package. The device supports 5-V V_{CC} Operation. All Inputs accept voltages up to 5.5 V. $\pm 24\text{-mA}$ output drive at 3.3 V. The maximum time propagation delay (t_{pd}) is 5.4 ns at 3.3 V. Low Power Consumption, 10- μA Max I_{CC} . Typical output ground bounce (V_{OLP}) and Output V_{OH} Undershoot (V_{OHV}). This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The SN74LVC1G19 device has isolation during power off. I_{off} supports live insertion, partial-power-down mode and back drive protection.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74LVC1G19.

Table 1. Function Table

INPUTS		OUTPUTS	
\bar{E}	A	Y_0	Y_1
L	L	L	H
L	H	H	L
H	X	H	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G19 device is a 1-of-2 decoder/demultiplexer. This device decodes the 1 bit address on input A and places a logic low on the matching address output, Y_0 or Y_1 , when the enable (\bar{E}) input signal is low. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs.

9.2 Typical Application

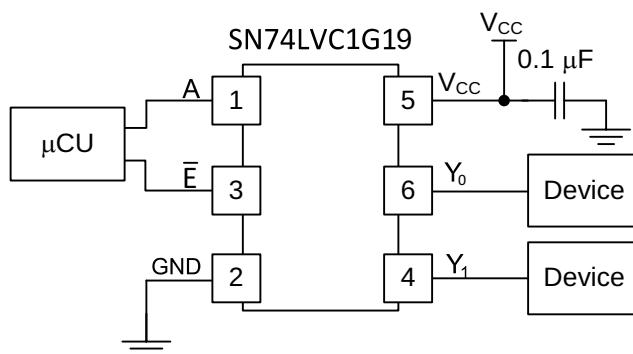


Figure 5. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see $(V_{IH}$ and V_{IL}) in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions:
 - Load currents must not exceed 50 mA per output and 100 mA total for the part.
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Application (continued)

9.2.3 Application Curve

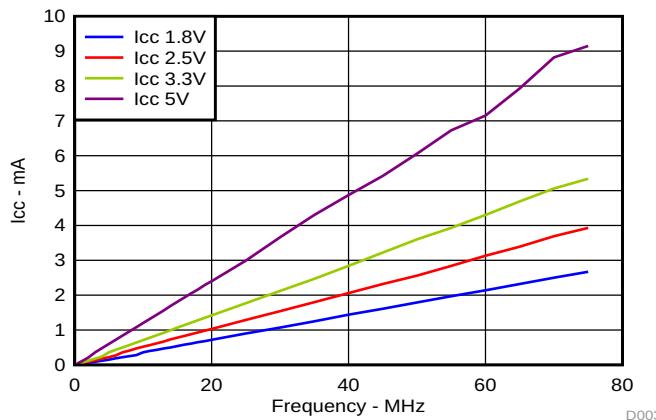


Figure 6. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Absolute Maximum Ratings* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F capacitor is recommended. If there are multiple V_{CC} terminals then 0.01- μ F or 0.022- μ F capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 7 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example



Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.

Blu-ray is a registered trademark of Blu-ray Disc Association.

All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022 — TI Glossary.](#)

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp (³)	Op Temp (°C)	Device Marking (^{4/5})	Samples
SN74LVC1G19BVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVRE4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C195, C19R)
SN74LVC1G19DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(CY5, CYF, CYK, CYR)
SN74LVC1G19DCKRE4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY5
SN74LVC1G19DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY5
SN74LVC1G19DRLLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1JZ, CY7, CYR)
SN74LVC1G19DRLRG4	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1JZ, CY7, CYR)
SN74LVC1G19DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CY
SN74LVC1G19YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CY7, CYN)
										Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JESD09B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

PACKAGE OPTION ADDENDUM

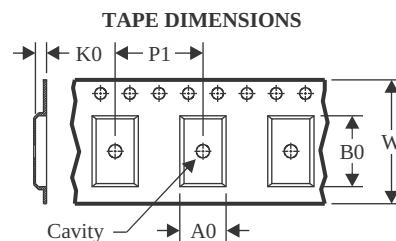
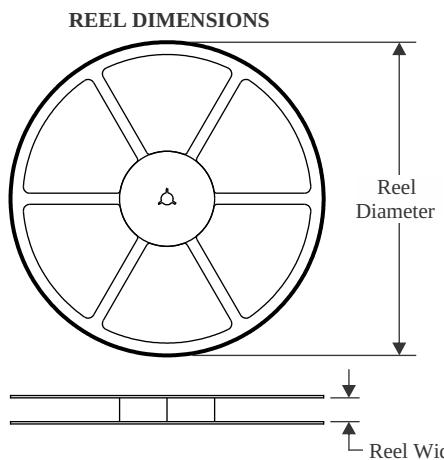
1.1-Apr-2023

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

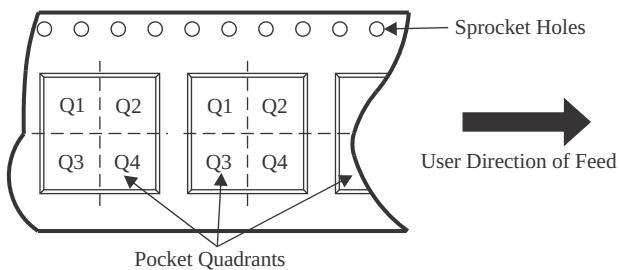
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

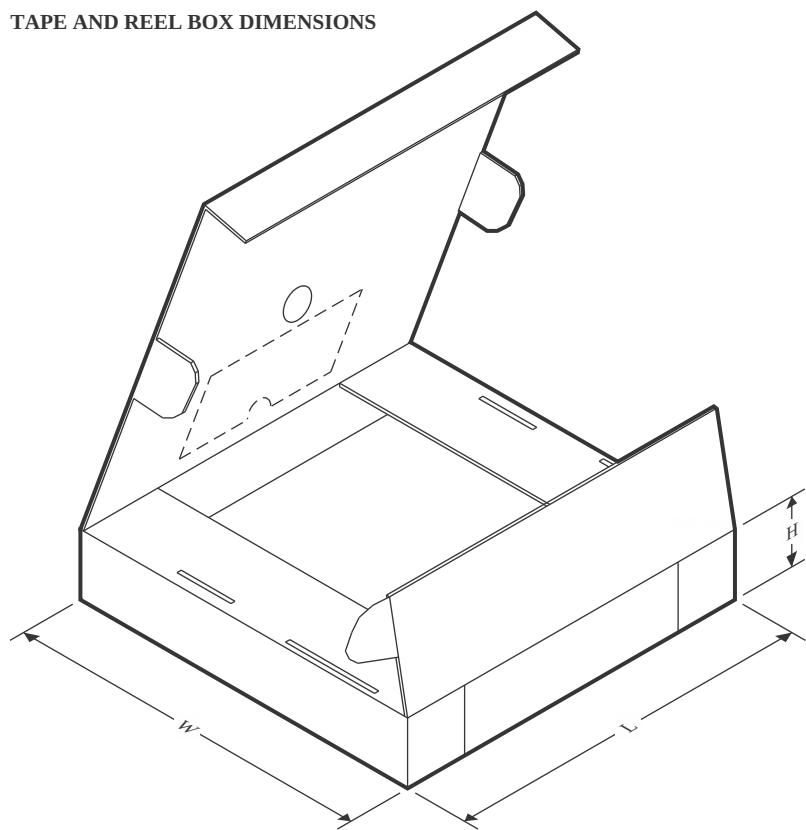
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G19DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G19DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G19DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G19DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


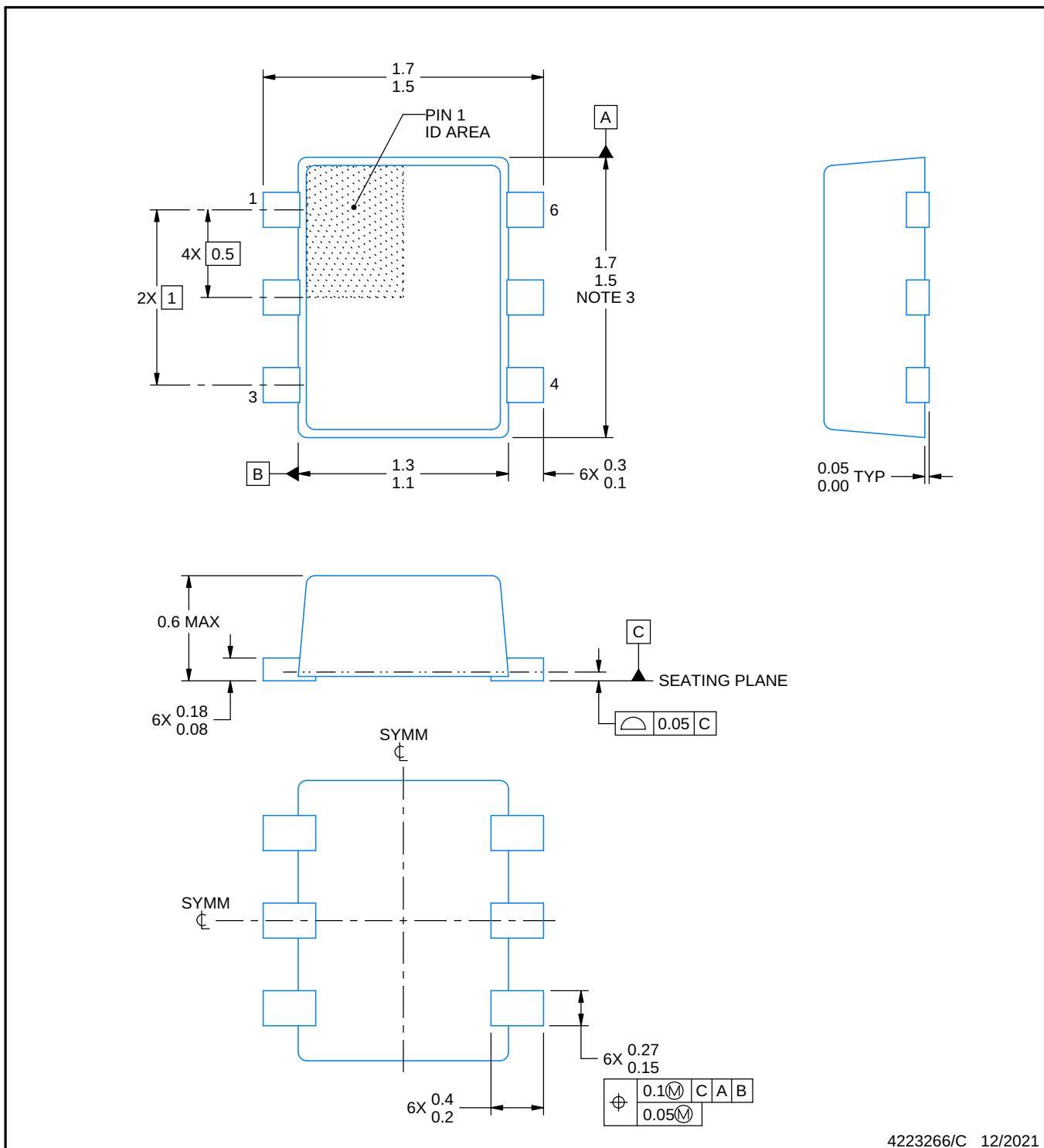
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G19DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G19DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G19DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G19DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G19YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/C 12/2021

NOTES:

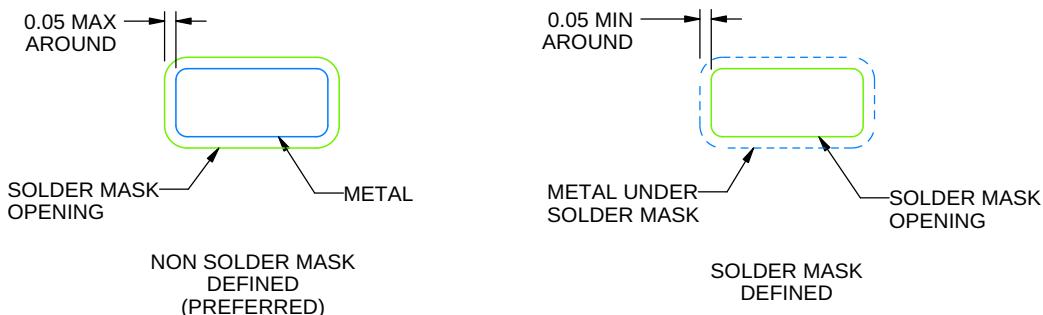
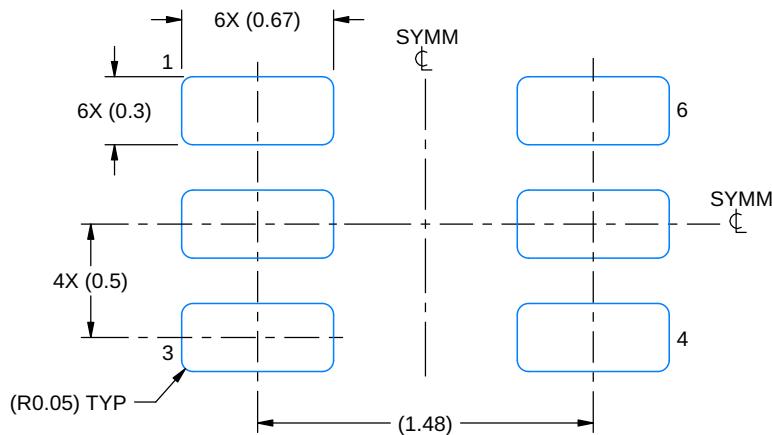
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

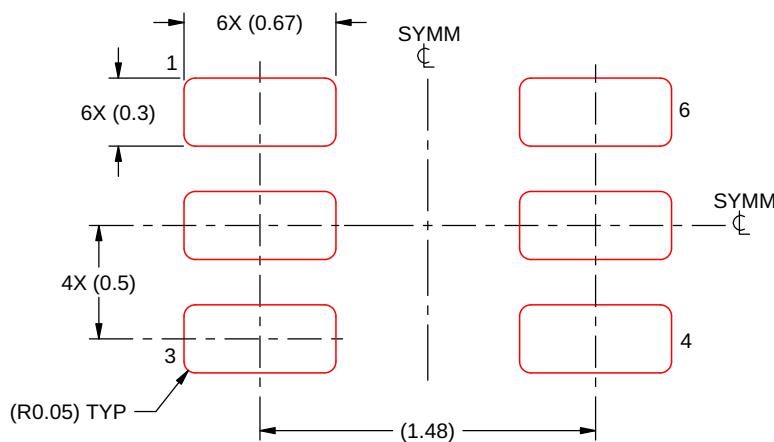
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

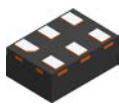
PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

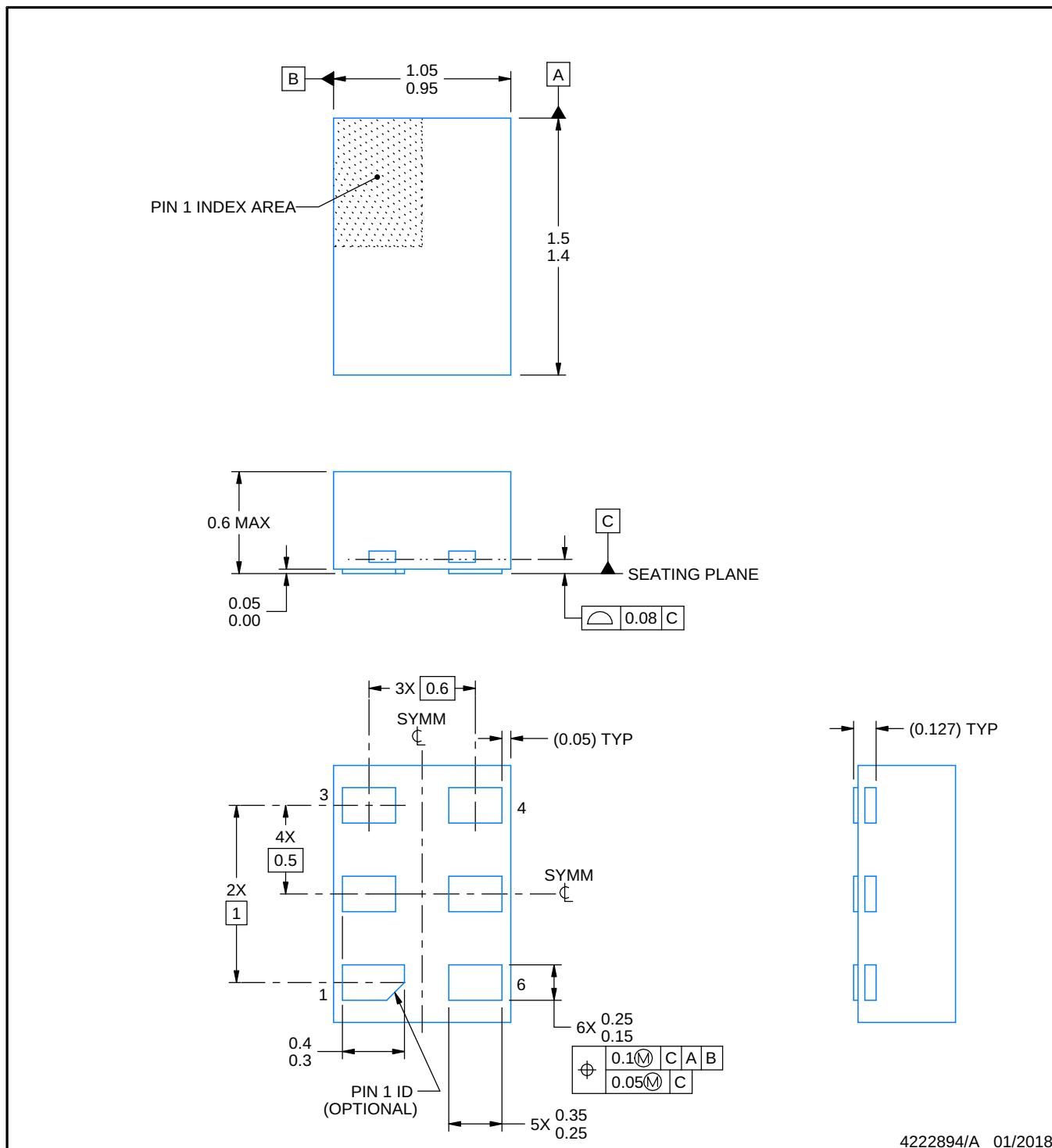
PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

NOTES:

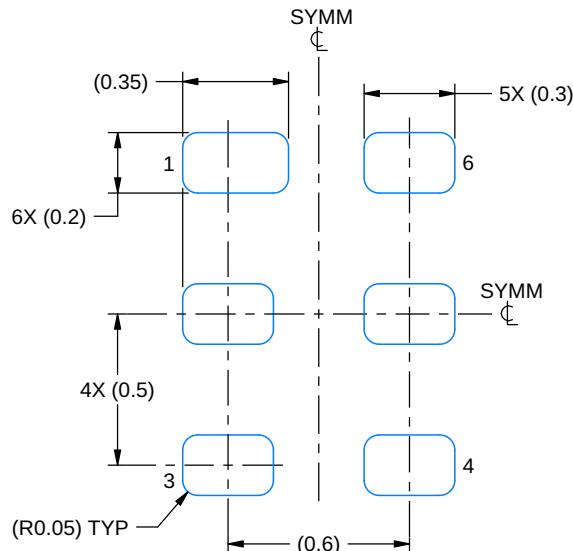
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

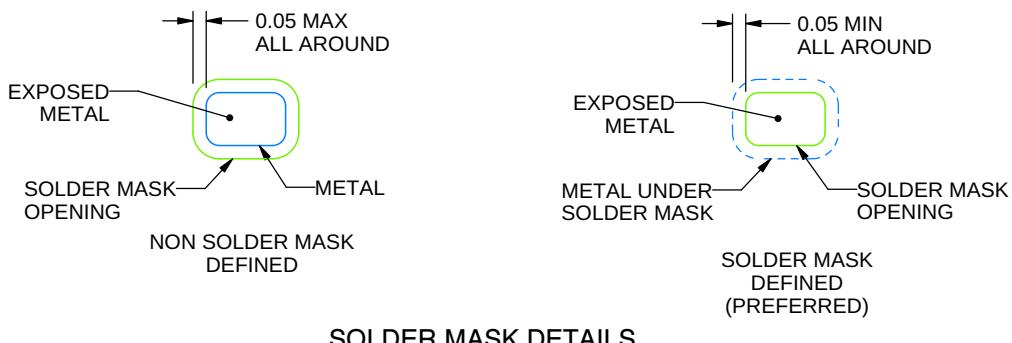
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

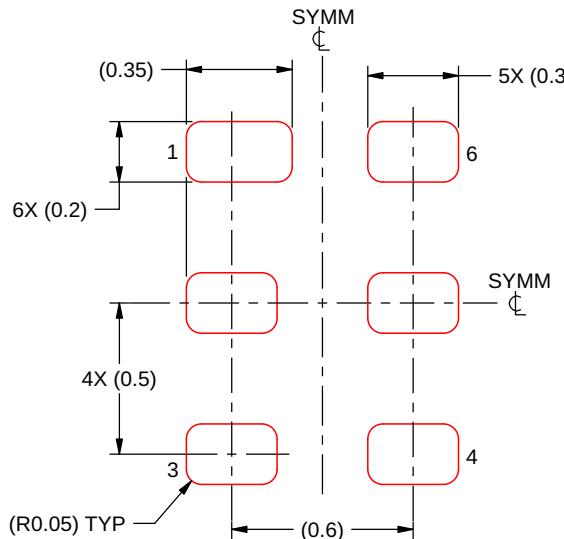
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

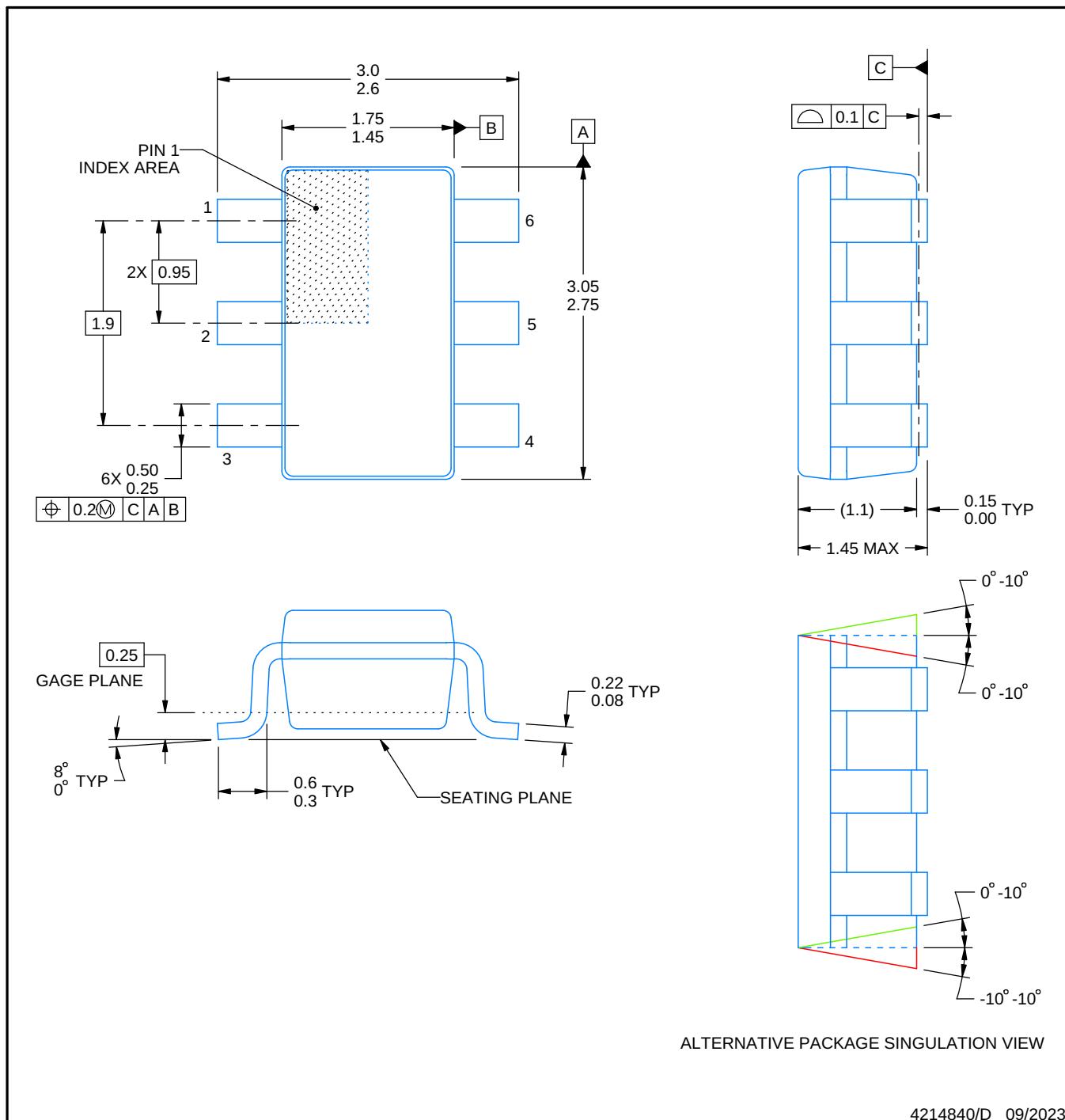
PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

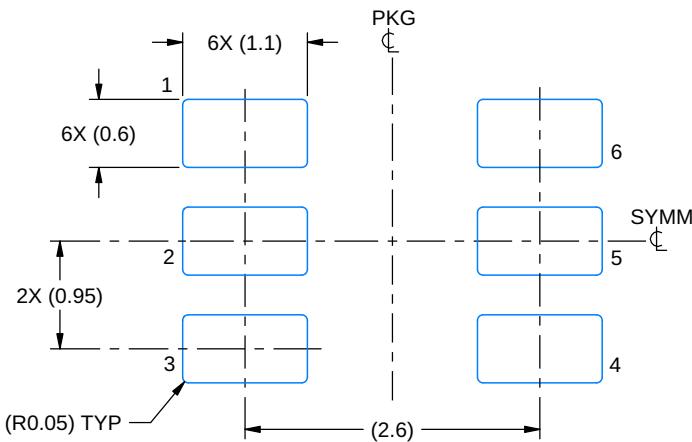
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
- Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

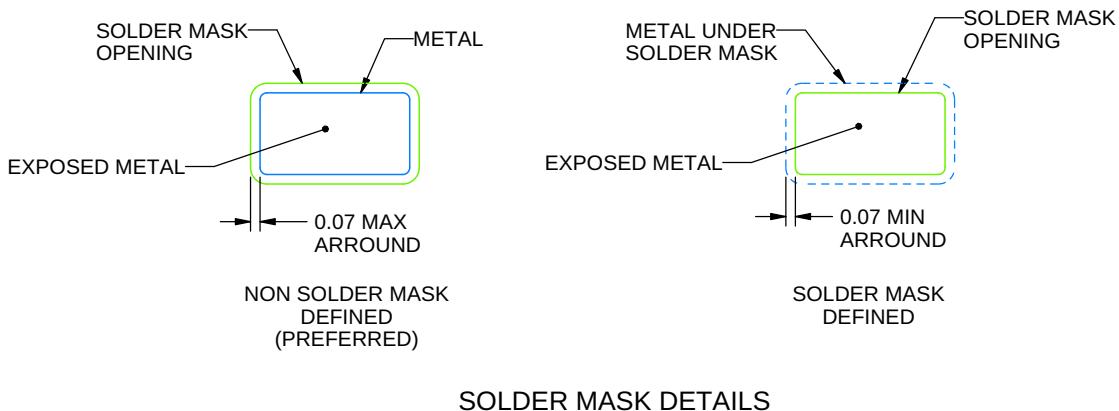
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

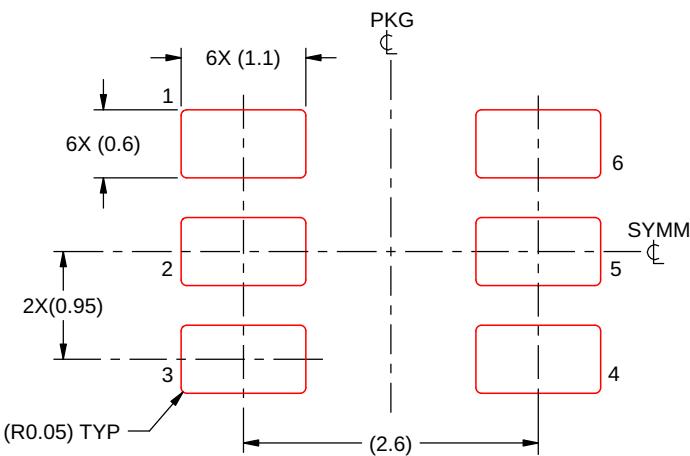
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

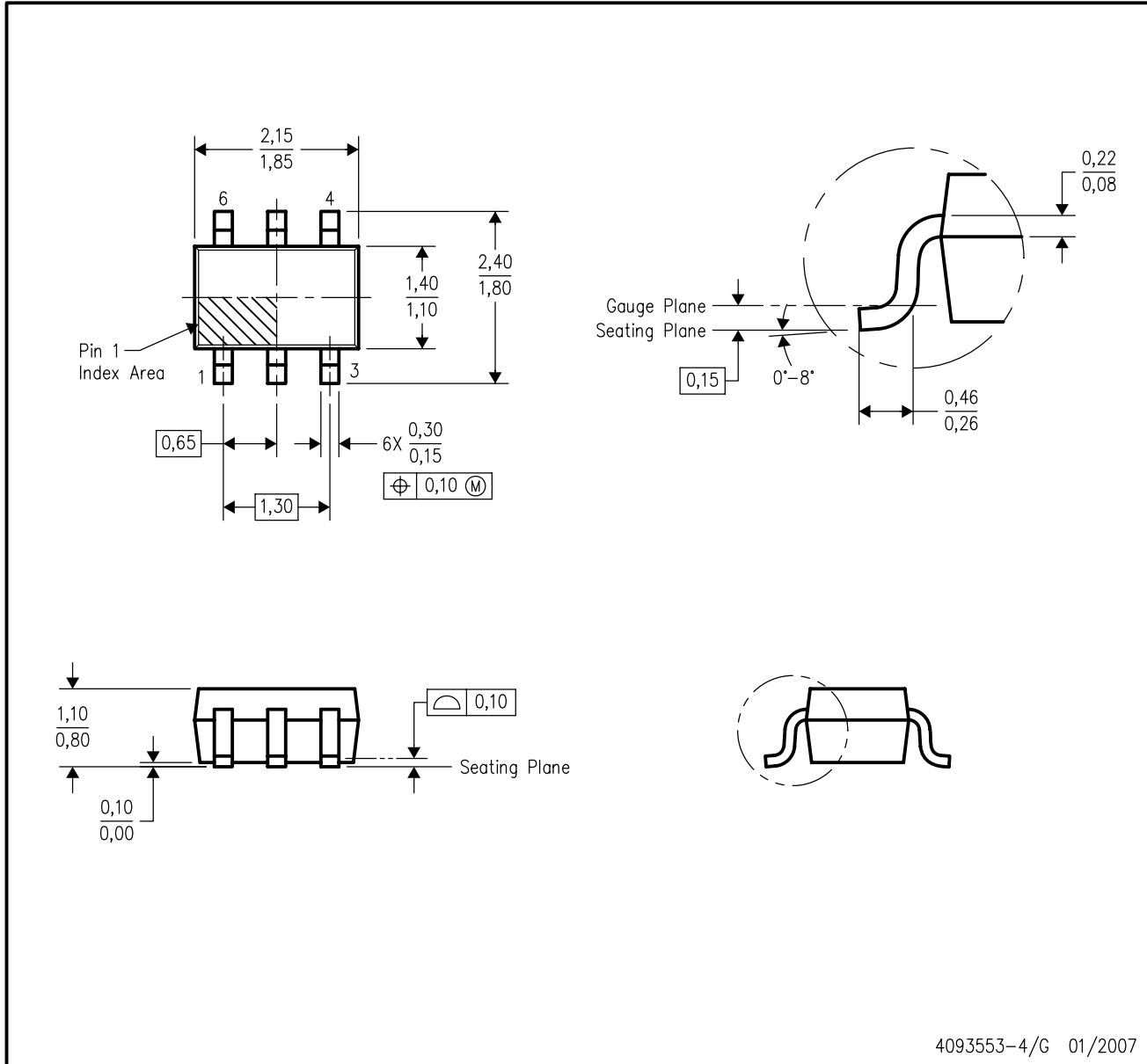
4214840/D 09/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

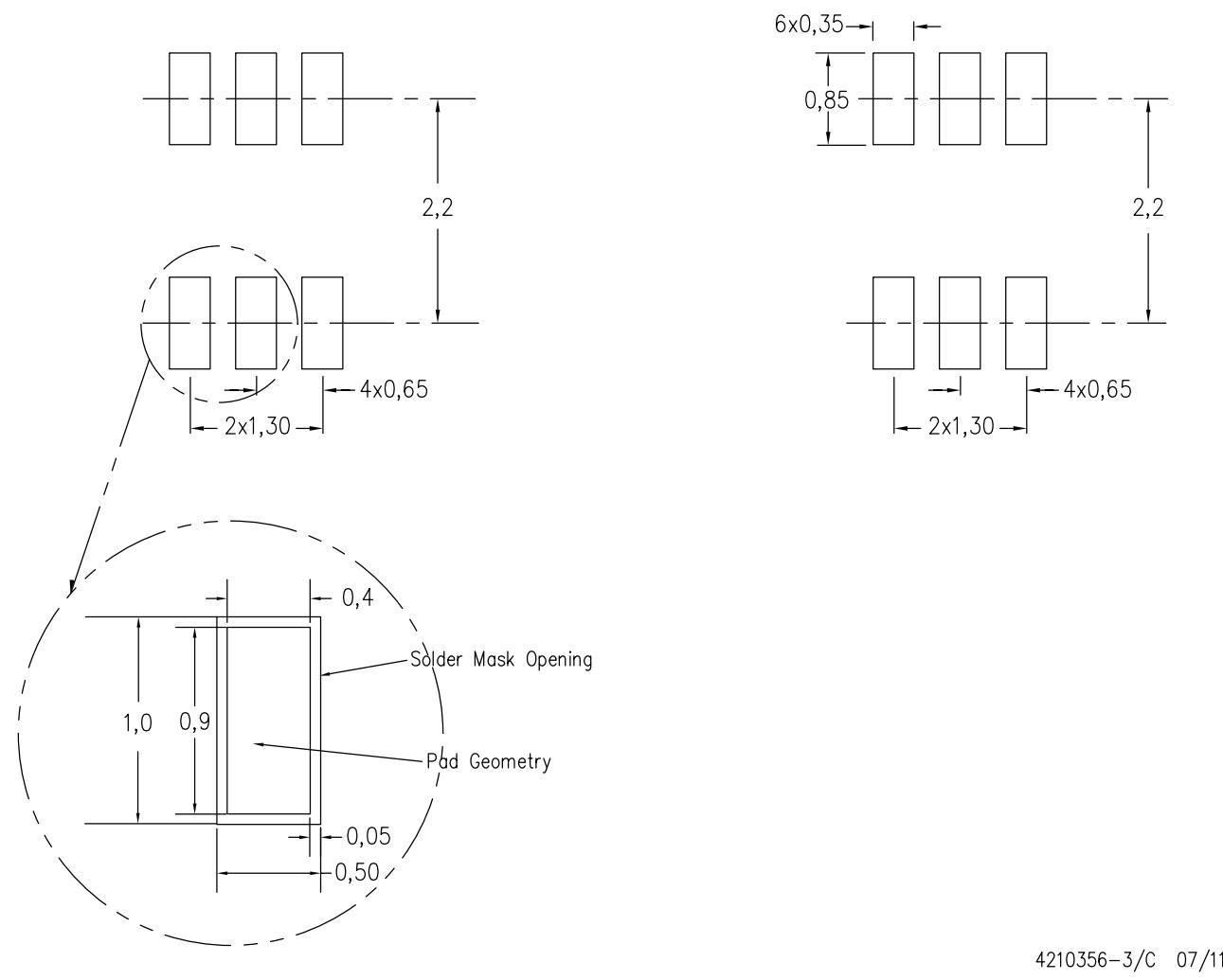
LAND PATTERN DATA

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE

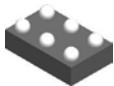
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

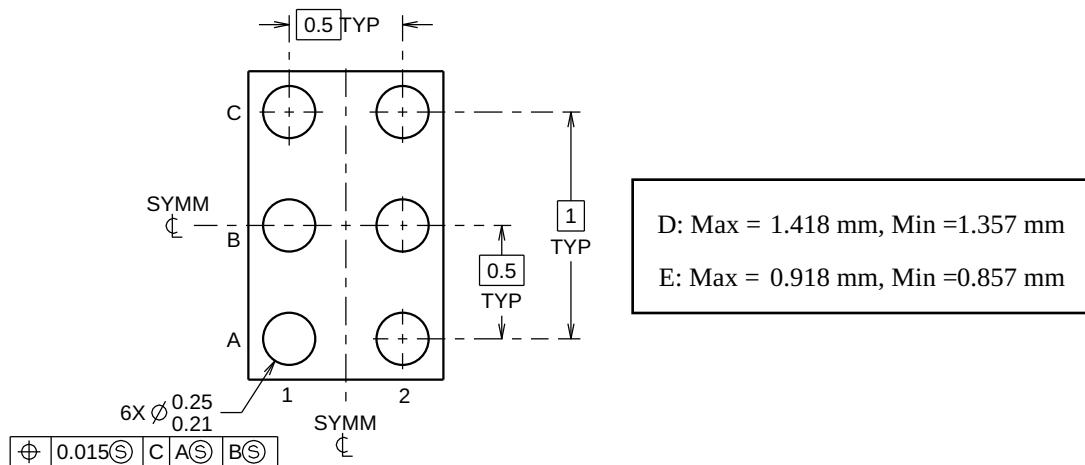
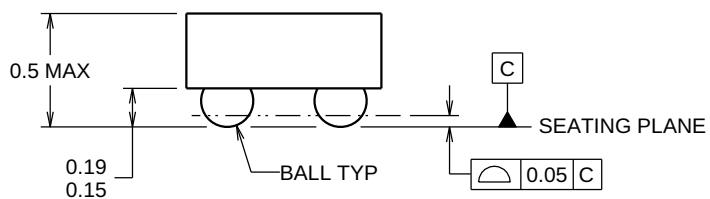
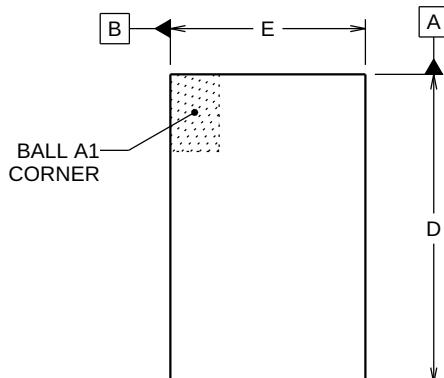
YZP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree is a trademark of Texas Instruments.

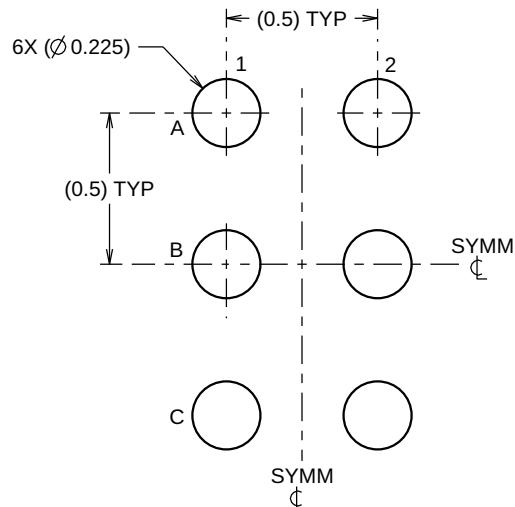
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

EXAMPLE BOARD LAYOUT

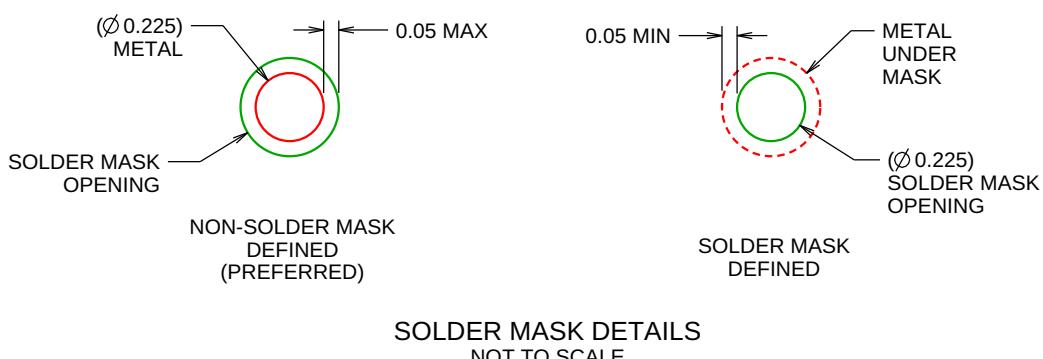
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

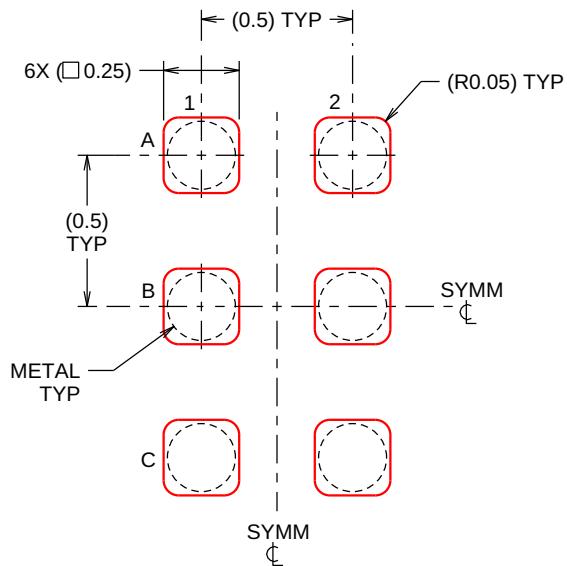
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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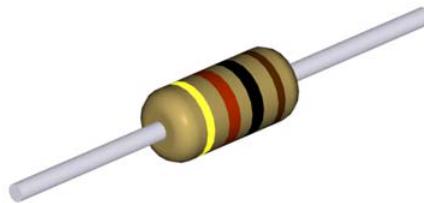
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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Data sheet

Carbon Film Leaded Resistor - RS Series

■Features

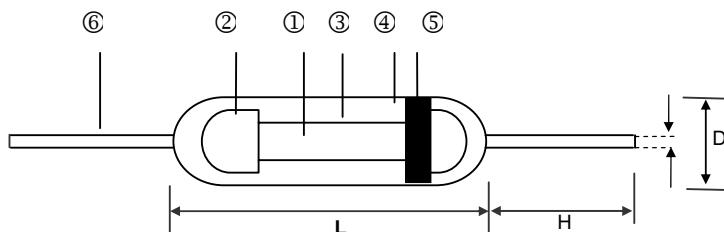
- The most economic industrial investment
- Standard tolerance: +/-5%
- Excellent long term stability
- Termination: Standard solder-plated copper lead



■Applications

- Automotive
- Telecommunication
- Medical Equipment

■Construction

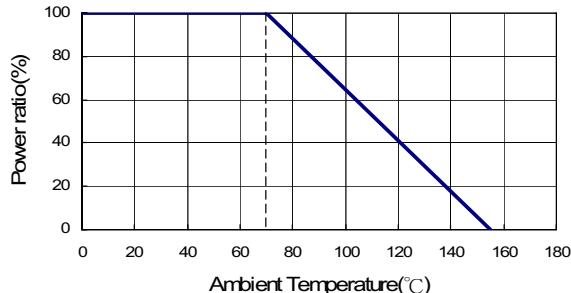
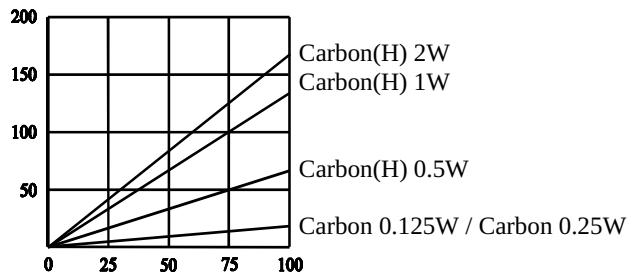


①	Ceramic Rod	④	Non-flame Paint With Sol Vent-proof
②	Tinned Iron Caps	⑤	Colour Code
③	Carbon Film	⑥	Lead Wire

■Dimensions

Unit: mm

Type	L	D	H	d	Weight (g) (1000pcs)
Carbon 0.125W	3.3+0.4/-0.2	1.8±0.3	29.3±2.0	0.452.3±0.03	92
Carbon 0.25W	6.3±0.5	2.3±0.3	28±2.0	0.55±0.03	155
Carbon 0.5W (H)	6.3±0.5	2.3±0.3	28±2.0	0.55±0.03	155
Carbon 1W (H)	9.0±0.5	3.2±0.5	26±2.0	0.65±0.03	352
Carbon 2W (H)	11.5±1.0	4.5±0.5	35±2.0	0.78±0.03	775

**■Derating Curve****■Hop-Spot Temperature****■Part Numbering**

RS-	Carbon-	1R-	5%-	0.125W
Series	Type	Resistance	Tolerance	Power rating @ 70°C
	Carbon Carbon(H)	0.5R: 0.5 Ω 1R: 1Ω 10R: 10Ω 10K: 10KΩ 100K: 100KΩ	±5%	0.125W 0.25W 0.5W 1W 2W

■Electrical Specifications

Type	Item	Power Rating at 70°C	Operating Temp. Range	Max. Working Voltage	Max. Overload Voltage	Dielectric Withstanding Voltage	Resistance Range
							±5%
Carbon	0.125W	-55 ~ +155°C	-55 ~ +155°C	150V	300V	300V	0.1Ω - 22MΩ
Carbon	0.25W			250V	500V	500V	1Ω - 10MΩ
Carbon(H)	0.5W			300V	500V	500V	0.1Ω - 22MΩ
Carbon(H)	1W			400V	800V	800V	1Ω - 10MΩ
Carbon(H)	2W			500V	1000V	1000V	0.1Ω - 10MΩ

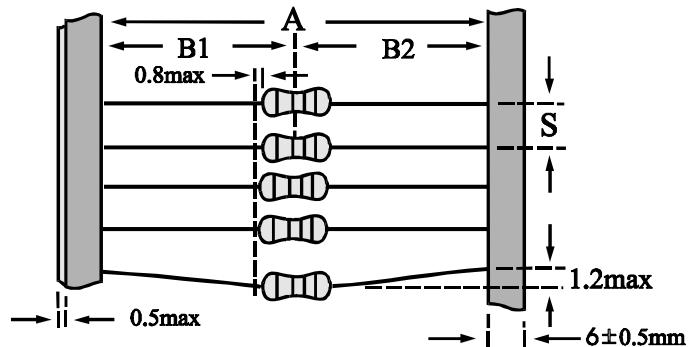
**■ Environmental Characteristics**

Item	Requirement	Test Method
Short Time Overload	$\pm(0.75\%+0.05\Omega)$	JIS-C-5201-1 5.5 RCWV*2.5 or Max. overload voltage for 5 seconds
Insulation Resistance	$> 1000M\Omega$	JIS-C-5201-1 5.6 Apply 100V _{DC} for 1 minute
Endurance	$\pm(3\%+0.05\Omega)$	JIS-C-5201-1 7.10 70 $\pm 2^\circ\text{C}$, Max. working voltage for 1000 hrs with 1.5 hrs "ON" and 0.5 hrs "OFF"
Damp Heat with Load	100K $\Omega \pm 3\%$ 100K $\Omega \pm 5\%$	JIS-C-5201-1 7.9 40 $\pm 2^\circ\text{C}$, 90~95% R.H. Max. working voltage for 1000 hrs with 1.5 hrs "ON" and 0.5 hrs "OFF"
Solderability	90% min. Coverage	JIS-C-5201-1 6.5 245 $\pm 5^\circ\text{C}$ for 3 seconds
Dielectric Withstanding Voltage	By Type	JIS-C-5201-1 5.7 Apply Max. Overload Voltage for 1 minute
Temperature Coefficient	< 100K Ω +350ppm~-500ppm 100K Ω ~1M Ω -0ppm~-700ppm > 1 M Ω -0ppm~-1500ppm	Resistance value at room temperature and room Temperature+100°C
Pulse Overload	$\pm(1\%+0.05\Omega)$	JIS-C-5201-1 5.8 4 times RCWV for 10000 cycles with 1 second "ON" and 25 seconds "OFF"
Resistance To Solvent	No deterioration of coatings and markings	JIS-C-5201-1 6.9 Trichroethane for 1 min. with ultrasonic
Terminal Strength	Tensile: 2.5 kg	Direct Load for 10 seconds In the direction off the terminal leads

■ Rated Continuous Working Voltage(RCWV) = $\sqrt{P*R}$ **■ Storage Temperature: 25 $\pm 3^\circ\text{C}$; Humidity < 80%RH**

■Taping/Packing Specifications

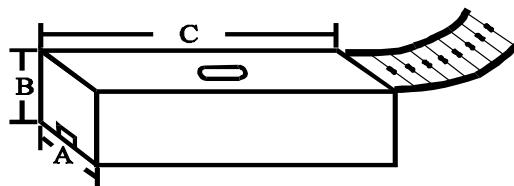
Packing Methods (Ammo)



Unit: mm

Packaging Type	Packing Methods		
	A	B1-B2	S
Carbon 0.125W	52+1/-0	1.2	5
Carbon 0.25W	52+1/-0	1.2	5
Carbon 0.5W (H)	52+1/-0	1.2	5
Carbon 1W (H)	52+1/-0	1.5	5
Carbon 2W (H)	52+1/-0	1.5	10

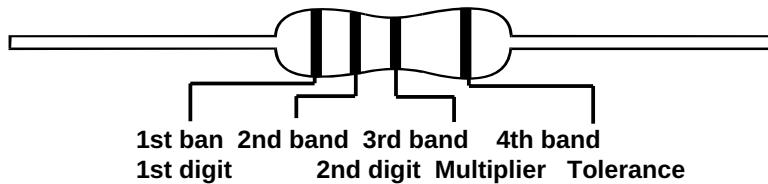
Ammo Packing



Unit: mm

Packaging Type	Packing Methods			Ammo Packing			
	A	B1-B2	S	A	B	C	Qty
Carbon 0.125W	26+1/-0	1.0	5	80	105	264	5,000
Carbon 0.25W	26+1/-0	1.0	5	80	105	264	5,000
Carbon 0.5W (H)	26+1/-0	1.0	5	80	105	264	5,000
Carbon 1W (H)	73+1/-0	1.5	5	103	82	265	1,000
Carbon 2W (H)	73+1/-0	1.5	10	103	96	265	1,000

■Marking & Resistance Tolerance



±5%	E-24	1.0	1.1	1.2	1.3	1.5	1.6	1.8	2.0	2.2	2.4	2.7	3.0	3.3	3.6	3.9	4.3	4.7	5.1	5.6	6.2	6.8	7.5	8.2	9.1
-----	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

Cold	Digit	Multiplier	Tolerance	
Without	-	-	-	-
Silver	-	10^{-2}	-	-
Gold	-	10^{-1}	±5.0%	J
Black	0	10^0	-	-
Brown	1	10^1	-	-
Red	2	10^2	-	-
Orange	3	10^3	-	-
Yellow	4	10^4	-	-
Green	5	10^5	-	-
Blue	6	10^6	-	-
Violet	7	10^7	-	-
Grey	8	10^8	-	-
White	9	10^9	-	-

**RS Stock number reference table****RS Carbon Film 0.25W Standard Power Rating Series**

Part Number	RS Stock Number
RS-Carbon-1R-5%-0.25W	707-7420
RS-Carbon-1R1-5%-0.25W	707-7439
RS-Carbon-1R2-5%-0.25W	707-7432
RS-Carbon-1R3-5%-0.25W	707-7436
RS-Carbon-1R5-5%-0.25W	707-7445
RS-Carbon-1R6-5%-0.25W	707-7448
RS-Carbon-1R8-5%-0.25W	707-7442
RS-Carbon-2R-5%-0.25W	707-7451
RS-Carbon-2R2-5%-0.25W	707-7454
RS-Carbon-2R4-5%-0.25W	707-7458
RS-Carbon-2R7-5%-0.25W	707-7467
RS-Carbon-3R-5%-0.25W	707-7460
RS-Carbon-3R3-5%-0.25W	707-7464
RS-Carbon-3R6-5%-0.25W	707-7473
RS-Carbon-3R9-5%-0.25W	707-7476
RS-Carbon-4R3-5%-0.25W	707-7470
RS-Carbon-4R7-5%-0.25W	707-7489
RS-Carbon-5R1-5%-0.25W	707-7482
RS-Carbon-5R6-5%-0.25W	707-7486
RS-Carbon-6R2-5%-0.25W	707-7495
RS-Carbon-6R8-5%-0.25W	707-7498
RS-Carbon-7R5-5%-0.25W	707-7492
RS-Carbon-8R2-5%-0.25W	707-7502
RS-Carbon-9R1-5%-0.25W	707-7505
RS-Carbon-10R-5%-0.25W	707-7509
RS-Carbon-11R-5%-0.25W	707-7518
RS-Carbon-12R-5%-0.25W	707-7511
RS-Carbon-13R-5%-0.25W	707-7515
RS-Carbon-15R-5%-0.25W	707-7524
RS-Carbon-16R-5%-0.25W	707-7527
RS-Carbon-18R-5%-0.25W	707-7521
RS-Carbon-20R-5%-0.25W	707-7530
RS-Carbon-22R-5%-0.25W	707-7533
RS-Carbon-24R-5%-0.25W	707-7537
RS-Carbon-27R-5%-0.25W	707-7546
RS-Carbon-30R-5%-0.25W	707-7549
RS-Carbon-33R-5%-0.25W	707-7543
RS-Carbon-36R-5%-0.25W	707-7552
RS-Carbon-39R-5%-0.25W	707-7555
RS-Carbon-43R-5%-0.25W	707-7559
RS-Carbon-47R-5%-0.25W	707-7568
RS-Carbon-51R-5%-0.25W	707-7561
RS-Carbon-56R-5%-0.25W	707-7565
RS-Carbon-62R-5%-0.25W	707-7574
RS-Carbon-68R-5%-0.25W	707-7577
RS-Carbon-75R-5%-0.25W	707-7571
RS-Carbon-82R-5%-0.25W	707-7580
RS-Carbon-91R-5%-0.25W	707-7583
RS-Carbon-100R-5%-0.25W	707-7587
RS-Carbon-110R-5%-0.25W	707-7596
RS-Carbon-120R-5%-0.25W	707-7599

**RS Carbon Film 0.25W Standard Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-130R-5%-0.25W	707-7593
RS-Carbon-150R-5%-0.25W	707-7603
RS-Carbon-160R-5%-0.25W	707-7606
RS-Carbon-180R-5%-0.25W	707-7600
RS-Carbon-200R-5%-0.25W	707-7619
RS-Carbon-220R-5%-0.25W	707-7612
RS-Carbon-240R-5%-0.25W	707-7616
RS-Carbon-270R-5%-0.25W	707-7625
RS-Carbon-300R-5%-0.25W	707-7628
RS-Carbon-330R-5%-0.25W	707-7622
RS-Carbon-360R-5%-0.25W	707-7631
RS-Carbon-390R-5%-0.25W	707-7634
RS-Carbon-430R-5%-0.25W	707-7638
RS-Carbon-470R-5%-0.25W	707-7647
RS-Carbon-510R-5%-0.25W	707-7640
RS-Carbon-560R-5%-0.25W	707-7644
RS-Carbon-620R-5%-0.25W	707-7653
RS-Carbon-680R-5%-0.25W	707-7656
RS-Carbon-750R-5%-0.25W	707-7650
RS-Carbon-820R-5%-0.25W	707-7669
RS-Carbon-910R-5%-0.25W	707-7662
RS-Carbon-1k-5%-0.25W	707-7666
RS-Carbon-1k1-5%-0.25W	707-7675
RS-Carbon-1k2-5%-0.25W	707-7678
RS-Carbon-1k3-5%-0.25W	707-7672
RS-Carbon-1k5-5%-0.25W	707-7681
RS-Carbon-1k6-5%-0.25W	707-7684
RS-Carbon-1k8-5%-0.25W	707-7688
RS-Carbon-2k-5%-0.25W	707-7697
RS-Carbon-2k2-5%-0.25W	707-7690
RS-Carbon-2k4-5%-0.25W	707-7694
RS-Carbon-2k7-5%-0.25W	707-7704
RS-Carbon-3k-5%-0.25W	707-7707
RS-Carbon-3k3-5%-0.25W	707-7701
RS-Carbon-3k6-5%-0.25W	707-7710
RS-Carbon-3k9-5%-0.25W	707-7713
RS-Carbon-4k3-5%-0.25W	707-7717
RS-Carbon-4k7-5%-0.25W	707-7726
RS-Carbon-5k1-5%-0.25W	707-7729
RS-Carbon-5k6-5%-0.25W	707-7723
RS-Carbon-6k2-5%-0.25W	707-7732
RS-Carbon-6k8-5%-0.25W	707-7735
RS-Carbon-7k5-5%-0.25W	707-7739
RS-Carbon-8k2-5%-0.25W	707-7748
RS-Carbon-9k1-5%-0.25W	707-7741
RS-Carbon-10k-5%-0.25W	707-7745
RS-Carbon-11k-5%-0.25W	707-7754
RS-Carbon-12k-5%-0.25W	707-7757
RS-Carbon-13k-5%-0.25W	707-7751
RS-Carbon-15k-5%-0.25W	707-7760
RS-Carbon-16k-5%-0.25W	707-7763
RS-Carbon-18k-5%-0.25W	707-7767
RS-Carbon-20k-5%-0.25W	707-7776
RS-Carbon-22k-5%-0.25W	707-7779

**RS Carbon Film 0.25W Standard Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-24k-5%-0.25W	707-7773
RS-Carbon-27k-5%-0.25W	707-7782
RS-Carbon-30k-5%-0.25W	707-7785
RS-Carbon-33k-5%-0.25W	707-7789
RS-Carbon-36k-5%-0.25W	707-7798
RS-Carbon-39k-5%-0.25W	707-7791
RS-Carbon-43k-5%-0.25W	707-7795
RS-Carbon-47k-5%-0.25W	707-7805
RS-Carbon-51k-5%-0.25W	707-7808
RS-Carbon-56k-5%-0.25W	707-7802
RS-Carbon-62k-5%-0.25W	707-7811
RS-Carbon-68k-5%-0.25W	707-7814
RS-Carbon-75k-5%-0.25W	707-7818
RS-Carbon-82k-5%-0.25W	707-7827
RS-Carbon-91k-5%-0.25W	707-7820
RS-Carbon-100k-5%-0.25W	707-7824
RS-Carbon-110k-5%-0.25W	707-7833
RS-Carbon-120k-5%-0.25W	707-7836
RS-Carbon-130k-5%-0.25W	707-7830
RS-Carbon-150k-5%-0.25W	707-7849
RS-Carbon-160k-5%-0.25W	707-7842
RS-Carbon-180k-5%-0.25W	707-7846
RS-Carbon-200k-5%-0.25W	707-7855
RS-Carbon-220k-5%-0.25W	707-7858
RS-Carbon-240k-5%-0.25W	707-7852
RS-Carbon-270k-5%-0.25W	707-7861
RS-Carbon-300k-5%-0.25W	707-7864
RS-Carbon-330k-5%-0.25W	707-7868
RS-Carbon-360k-5%-0.25W	707-7877
RS-Carbon-390k-5%-0.25W	707-7870
RS-Carbon-430k-5%-0.25W	707-7874
RS-Carbon-470k-5%-0.25W	707-7883
RS-Carbon-510k-5%-0.25W	707-7886
RS-Carbon-560k-5%-0.25W	707-7880
RS-Carbon-620k-5%-0.25W	707-7899
RS-Carbon-680k-5%-0.25W	707-7892
RS-Carbon-750k-5%-0.25W	707-7896
RS-Carbon-820k-5%-0.25W	707-7906
RS-Carbon-910k-5%-0.25W	707-7909
RS-Carbon-1M-5%-0.25W	707-7903
RS-Carbon-1M1-5%-0.25W	707-7912
RS-Carbon-1M2-5%-0.25W	707-7915
RS-Carbon-1M3-5%-0.25W	707-7919
RS-Carbon-1M5-5%-0.25W	707-7928
RS-Carbon-1M6-5%-0.25W	707-7921
RS-Carbon-1M8-5%-0.25W	707-7925
RS-Carbon-2M-5%-0.25W	707-7934
RS-Carbon-2M2-5%-0.25W	707-7937
RS-Carbon-2M4-5%-0.25W	707-7931
RS-Carbon-2M7-5%-0.25W	707-7940
RS-Carbon-3M-5%-0.25W	707-7943
RS-Carbon-3M3-5%-0.25W	707-7947
RS-Carbon-3M6-5%-0.25W	707-7956
RS-Carbon-3M9-5%-0.25W	707-7959

**RS Carbon Film 0.25W Standard Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-4M3-5%-0.25W	707-7953
RS-Carbon-4M7-5%-0.25W	707-7962
RS-Carbon-5M1-5%-0.25W	707-7965
RS-Carbon-5M6-5%-0.25W	707-7969
RS-Carbon-6M2-5%-0.25W	707-7978
RS-Carbon-6M8-5%-0.25W	707-7971
RS-Carbon-7M5-5%-0.25W	707-7975
RS-Carbon-8M2-5%-0.25W	707-7984
RS-Carbon-9M1-5%-0.25W	707-7987

RS Carbon Film 0.5W High Power Rating Series

Part Number	RS Stock Number
RS-Carbon-1R-5%-0.5W	707-7981
RS-Carbon-1R1-5%-0.5W	707-7990
RS-Carbon-1R2-5%-0.5W	707-7993
RS-Carbon-1R3-5%-0.5W	707-7997
RS-Carbon-1R5-5%-0.5W	707-8000
RS-Carbon-1R6-5%-0.5W	707-8003
RS-Carbon-1R8-5%-0.5W	707-8007
RS-Carbon-2R-5%-0.5W	707-8016
RS-Carbon-2R2-5%-0.5W	707-8019
RS-Carbon-2R4-5%-0.5W	707-8013
RS-Carbon-2R7-5%-0.5W	707-8022
RS-Carbon-3R-5%-0.5W	707-8025
RS-Carbon-3R3-5%-0.5W	707-8029
RS-Carbon-3R6-5%-0.5W	707-8038
RS-Carbon-3R9-5%-0.5W	707-8031
RS-Carbon-4R3-5%-0.5W	707-8035
RS-Carbon-4R7-5%-0.5W	707-8044
RS-Carbon-5R1-5%-0.5W	707-8047
RS-Carbon-5R6-5%-0.5W	707-8041
RS-Carbon-6R2-5%-0.5W	707-8050
RS-Carbon-6R8-5%-0.5W	707-8053
RS-Carbon-7R5-5%-0.5W	707-8057
RS-Carbon-8R2-5%-0.5W	707-8066
RS-Carbon-9R1-5%-0.5W	707-8069
RS-Carbon-10R-5%-0.5W	707-8063
RS-Carbon-11R-5%-0.5W	707-8072
RS-Carbon-12R-5%-0.5W	707-8075
RS-Carbon-13R-5%-0.5W	707-8079
RS-Carbon-15R-5%-0.5W	707-8088
RS-Carbon-16R-5%-0.5W	707-8081
RS-Carbon-18R-5%-0.5W	707-8085
RS-Carbon-20R-5%-0.5W	707-8094
RS-Carbon-22R-5%-0.5W	707-8097
RS-Carbon-24R-5%-0.5W	707-8091
RS-Carbon-27R-5%-0.5W	707-8101
RS-Carbon-30R-5%-0.5W	707-8104
RS-Carbon-33R-5%-0.5W	707-8108
RS-Carbon-36R-5%-0.5W	707-8117
RS-Carbon-39R-5%-0.5W	707-8110
RS-Carbon-43R-5%-0.5W	707-8114

**RS Carbon Film 0.5W High Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-47R-5%-0.5W	707-8123
RS-Carbon-51R-5%-0.5W	707-8126
RS-Carbon-56R-5%-0.5W	707-8120
RS-Carbon-62R-5%-0.5W	707-8139
RS-Carbon-68R-5%-0.5W	707-8132
RS-Carbon-75R-5%-0.5W	707-8136
RS-Carbon-82R-5%-0.5W	707-8145
RS-Carbon-91R-5%-0.5W	707-8148
RS-Carbon-100R-5%-0.5W	707-8142
RS-Carbon-110R-5%-0.5W	707-8151
RS-Carbon-120R-5%-0.5W	707-8154
RS-Carbon-130R-5%-0.5W	707-8158
RS-Carbon-150R-5%-0.5W	707-8167
RS-Carbon-160R-5%-0.5W	707-8160
RS-Carbon-180R-5%-0.5W	707-8164
RS-Carbon-200R-5%-0.5W	707-8173
RS-Carbon-220R-5%-0.5W	707-8176
RS-Carbon-240R-5%-0.5W	707-8170
RS-Carbon-270R-5%-0.5W	707-8189
RS-Carbon-300R-5%-0.5W	707-8182
RS-Carbon-330R-5%-0.5W	707-8186
RS-Carbon-360R-5%-0.5W	707-8195
RS-Carbon-390R-5%-0.5W	707-8198
RS-Carbon-430R-5%-0.5W	707-8192
RS-Carbon-470R-5%-0.5W	707-8202
RS-Carbon-510R-5%-0.5W	707-8205
RS-Carbon-560R-5%-0.5W	707-8209
RS-Carbon-620R-5%-0.5W	707-8218
RS-Carbon-680R-5%-0.5W	707-8211
RS-Carbon-750R-5%-0.5W	707-8215
RS-Carbon-820R-5%-0.5W	707-8224
RS-Carbon-910R-5%-0.5W	707-8227
RS-Carbon-1k-5%-0.5W	707-8221
RS-Carbon-1k1-5%-0.5W	707-8230
RS-Carbon-1k2-5%-0.5W	707-8233
RS-Carbon-1k3-5%-0.5W	707-8237
RS-Carbon-1k5-5%-0.5W	707-8246
RS-Carbon-1k6-5%-0.5W	707-8249
RS-Carbon-1k8-5%-0.5W	707-8243
RS-Carbon-2k-5%-0.5W	707-8252
RS-Carbon-2k2-5%-0.5W	707-8255
RS-Carbon-2k4-5%-0.5W	707-8259
RS-Carbon-2k7-5%-0.5W	707-8268
RS-Carbon-3k-5%-0.5W	707-8261
RS-Carbon-3k3-5%-0.5W	707-8265
RS-Carbon-3k6-5%-0.5W	707-8274
RS-Carbon-3k9-5%-0.5W	707-8277
RS-Carbon-4k3-5%-0.5W	707-8271
RS-Carbon-4k7-5%-0.5W	707-8280
RS-Carbon-5k1-5%-0.5W	707-8283
RS-Carbon-5k6-5%-0.5W	707-8287
RS-Carbon-6k2-5%-0.5W	707-8296
RS-Carbon-6k8-5%-0.5W	707-8299
RS-Carbon-7k5-5%-0.5W	707-8293

**RS Carbon Film 0.5W High Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-8k2-5%-0.5W	707-8303
RS-Carbon-9k1-5%-0.5W	707-8306
RS-Carbon-10k-5%-0.5W	707-8300
RS-Carbon-11k-5%-0.5W	707-8319
RS-Carbon-12k-5%-0.5W	707-8312
RS-Carbon-13k-5%-0.5W	707-8316
RS-Carbon-15k-5%-0.5W	707-8325
RS-Carbon-16k-5%-0.5W	707-8328
RS-Carbon-18k-5%-0.5W	707-8322
RS-Carbon-20k-5%-0.5W	707-8331
RS-Carbon-22k-5%-0.5W	707-8334
RS-Carbon-24k-5%-0.5W	707-8338
RS-Carbon-27k-5%-0.5W	707-8347
RS-Carbon-30k-5%-0.5W	707-8340
RS-Carbon-33k-5%-0.5W	707-8344
RS-Carbon-36k-5%-0.5W	707-8353
RS-Carbon-39k-5%-0.5W	707-8356
RS-Carbon-43k-5%-0.5W	707-8350
RS-Carbon-47k-5%-0.5W	707-8369
RS-Carbon-51k-5%-0.5W	707-8362
RS-Carbon-56k-5%-0.5W	707-8366
RS-Carbon-62k-5%-0.5W	707-8375
RS-Carbon-68k-5%-0.5W	707-8378
RS-Carbon-75k-5%-0.5W	707-8372
RS-Carbon-82k-5%-0.5W	7078-381
RS-Carbon-91k-5%-0.5W	707-8384
RS-Carbon-100k-5%-0.5W	707-8388
RS-Carbon-110k-5%-0.5W	707-8397
RS-Carbon-120k-5%-0.5W	707-8390
RS-Carbon-130k-5%-0.5W	707-8394
RS-Carbon-150k-5%-0.5W	707-8404
RS-Carbon-160k-5%-0.5W	707-8407
RS-Carbon-180k-5%-0.5W	707-8401
RS-Carbon-200k-5%-0.5W	707-8410
RS-Carbon-220k-5%-0.5W	707-8413
RS-Carbon-240k-5%-0.5W	707-8417
RS-Carbon-270k-5%-0.5W	707-8426
RS-Carbon-300k-5%-0.5W	707-8429
RS-Carbon-330k-5%-0.5W	707-8423
RS-Carbon-360k-5%-0.5W	707-8432
RS-Carbon-390k-5%-0.5W	707-8435
RS-Carbon-430k-5%-0.5W	707-8439
RS-Carbon-470k-5%-0.5W	707-8448
RS-Carbon-510k-5%-0.5W	707-8441
RS-Carbon-560k-5%-0.5W	707-8445
RS-Carbon-620k-5%-0.5W	707-8454
RS-Carbon-680k-5%-0.5W	707-8457
RS-Carbon-750k-5%-0.5W	707-8451
RS-Carbon-820k-5%-0.5W	707-8460
RS-Carbon-910k-5%-0.5W	707-8463
RS-Carbon-1M-5%-0.5W	707-8467
RS-Carbon-1M1-5%-0.5W	707-8476
RS-Carbon-1M2-5%-0.5W	707-8479
RS-Carbon-1M3-5%-0.5W	707-8473

**RS Carbon Film 0.5W High Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-1M5-5%-0.5W	707-8482
RS-Carbon-1M6-5%-0.5W	707-8485
RS-Carbon-1M8-5%-0.5W	707-8489
RS-Carbon-2M-5%-0.5W	707-8498
RS-Carbon-2M2-5%-0.5W	707-8491
RS-Carbon-2M4-5%-0.5W	707-8495
RS-Carbon-2M7-5%-0.5W	707-8505
RS-Carbon-3M-5%-0.5W	707-8508
RS-Carbon-3M3-5%-0.5W	707-8502
RS-Carbon-3M6-5%-0.5W	707-8511
RS-Carbon-3M9-5%-0.5W	707-8514
RS-Carbon-4M3-5%-0.5W	707-8518
RS-Carbon-4M7-5%-0.5W	707-8527
RS-Carbon-5M1-5%-0.5W	707-8520
RS-Carbon-5M6-5%-0.5W	707-8524
RS-Carbon-6M2-5%-0.5W	707-8533
RS-Carbon-6M8-5%-0.5W	707-8536
RS-Carbon-7M5-5%-0.5W	707-8530
RS-Carbon-8M2-5%-0.5W	707-8549
RS-Carbon-9M1-5%-0.5W	707-8542

RS Carbon Film 1W High Power Rating Series

RS-Carbon-1R-5%-1W	707-8546
RS-Carbon-1R2-5%-1W	707-8555
RS-Carbon-1R5-5%-1W	707-8558
RS-Carbon-1R8-5%-1W	707-8552
RS-Carbon-2R2-5%-1W	707-8561
RS-Carbon-2R7-5%-1W	707-8564
RS-Carbon-3R3-5%-1W	707-8568
RS-Carbon-3R9-5%-1W	707-8577
RS-Carbon-4R7-5%-1W	707-8570
RS-Carbon-5R6-5%-1W	707-8574
RS-Carbon-6R8-5%-1W	707-8583
RS-Carbon-8R2-5%-1W	707-8586
RS-Carbon-10R-5%-1W	707-8580
RS-Carbon-12R-5%-1W	707-8599
RS-Carbon-15R-5%-1W	707-8592
RS-Carbon-18R-5%-1W	707-8596
RS-Carbon-22R-5%-1W	707-8606
RS-Carbon-27R-5%-1W	707-8609
RS-Carbon-33R-5%-1W	707-8603
RS-Carbon-39R-5%-1W	707-8612
RS-Carbon-47R-5%-1W	707-8615
RS-Carbon-56R-5%-1W	707-8619
RS-Carbon-68R-5%-1W	707-8628
RS-Carbon-82R-5%-1W	707-8621
RS-Carbon-100R-5%-1W	707-8625
RS-Carbon-120R-5%-1W	707-8634
RS-Carbon-150R-5%-1W	707-8637
RS-Carbon-180R-5%-1W	707-8631
RS-Carbon-220R-5%-1W	707-8640
RS-Carbon-270R-5%-1W	707-8643
RS-Carbon-330R-5%-1W	707-8647

**RS Carbon Film 1W High Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-390R-5%-1W	707-8656
RS-Carbon-470R-5%-1W	707-8659
RS-Carbon-560R-5%-1W	707-8653
RS-Carbon-680R-5%-1W	707-8662
RS-Carbon-820R-5%-1W	707-8665
RS-Carbon-1k-5%-1W	707-8669
RS-Carbon-1k2-5%-1W	707-8678
RS-Carbon-1k5-5%-1W	707-8671
RS-Carbon-1k8-5%-1W	707-8675
RS-Carbon-2k2-5%-1W	707-8684
RS-Carbon-2k7-5%-1W	707-8687
RS-Carbon-3k3-5%-1W	707-8681
RS-Carbon-3k9-5%-1W	707-8690
RS-Carbon-4k7-5%-1W	707-8693
RS-Carbon-5k6-5%-1W	707-8697
RS-Carbon-6k8-5%-1W	707-8707
RS-Carbon-8k2-5%-1W	707-8700
RS-Carbon-10k-5%-1W	707-8704
RS-Carbon-12k-5%-1W	707-8713
RS-Carbon-15k-5%-1W	707-8716
RS-Carbon-18k-5%-1W	707-8710
RS-Carbon-22k-5%-1W	707-8729
RS-Carbon-27k-5%-1W	707-8722
RS-Carbon-33k-5%-1W	707-8726
RS-Carbon-39k-5%-1W	707-8735
RS-Carbon-47k-5%-1W	707-8738
RS-Carbon-56k-5%-1W	707-8732
RS-Carbon-68k-5%-1W	707-8741
RS-Carbon-82k-5%-1W	707-8744
RS-Carbon-100k-5%-1W	707-8748
RS-Carbon-120k-5%-1W	707-8757
RS-Carbon-150k-5%-1W	707-8750
RS-Carbon-180k-5%-1W	707-8754
RS-Carbon-220k-5%-1W	707-8763
RS-Carbon-270k-5%-1W	707-8766
RS-Carbon-330k-5%-1W	707-8760
RS-Carbon-390k-5%-1W	707-8779
RS-Carbon-470k-5%-1W	707-8772
RS-Carbon-560k-5%-1W	707-8776
RS-Carbon-680k-5%-1W	707-8785
RS-Carbon-820k-5%-1W	707-8788

RS Carbon Film 2W High Power Rating Series

Part Number	RS Stock Number
RS-Carbon-10R-5%-2W	707-8782
RS-Carbon-12R-5%-2W	707-8791
RS-Carbon-15R-5%-2W	707-8794
RS-Carbon-18R-5%-2W	707-8798
RS-Carbon-22R-5%-2W	707-8808
RS-Carbon-27R-5%-2W	707-8801
RS-Carbon-33R-5%-2W	707-8805
RS-Carbon-39R-5%-2W	707-8814
RS-Carbon-47R-5%-2W	707-8817

**RS Carbon Film 2W High Power Rating Series continued**

Part Number	RS Stock Number
RS-Carbon-56R-5%-2W	707-8811
RS-Carbon-68R-5%-2W	707-8820
RS-Carbon-82R-5%-2W	707-8823
RS-Carbon-100R-5%-2W	707-8827
RS-Carbon-120R-5%-2W	707-8836
RS-Carbon-150R-5%-2W	707-8839
RS-Carbon-180R-5%-2W	707-8833
RS-Carbon-220R-5%-2W	707-8842
RS-Carbon-270R-5%-2W	707-8845
RS-Carbon-330R-5%-2W	707-8849
RS-Carbon-390R-5%-2W	707-8858
RS-Carbon-470R-5%-2W	707-8851
RS-Carbon-560R-5%-2W	707-8855
RS-Carbon-680R-5%-2W	707-8864
RS-Carbon-820R-5%-2W	707-8867
RS-Carbon-1k-5%-2W	707-8861
RS-Carbon-1k2-5%-2W	707-8870
RS-Carbon-1k5-5%-2W	707-8873
RS-Carbon-1k8-5%-2W	707-8877
RS-Carbon-2k2-5%-2W	707-8886
RS-Carbon-2k7-5%-2W	707-8889
RS-Carbon-3k3-5%-2W	707-8883
RS-Carbon-3k9-5%-2W	707-8892
RS-Carbon-4k7-5%-2W	707-8895
RS-Carbon-5k6-5%-2W	707-8899
RS-Carbon-6k8-5%-2W	707-8909
RS-Carbon-8k2-5%-2W	707-8902
RS-Carbon-10k-5%-2W	707-8906
RS-Carbon-12k-5%-2W	707-8915
RS-Carbon-15k-5%-2W	707-8918
RS-Carbon-18k-5%-2W	707-8912
RS-Carbon-22k-5%-2W	707-8921
RS-Carbon-27k-5%-2W	707-8924
RS-Carbon-33k-5%-2W	707-8928
RS-Carbon-39k-5%-2W	707-8937
RS-Carbon-47k-5%-2W	707-8930
RS-Carbon-56k-5%-2W	707-8934
RS-Carbon-68k-5%-2W	707-8943
RS-Carbon-82k-5%-2W	707-8946
RS-Carbon-100k-5%-2W	707-8940
RS-Carbon-120k-5%-2W	707-8959
RS-Carbon-150k-5%-2W	707-8952
RS-Carbon-180k-5%-2W	707-8956
RS-Carbon-220k-5%-2W	707-8965
RS-Carbon-270k-5%-2W	707-8968
RS-Carbon-330k-5%-2W	707-8962
RS-Carbon-390k-5%-2W	707-8971
RS-Carbon-470k-5%-2W	707-8974
RS-Carbon-560k-5%-2W	707-8978
RS-Carbon-680k-5%-2W	707-8987
RS-Carbon-820k-5%-2W	707-8980