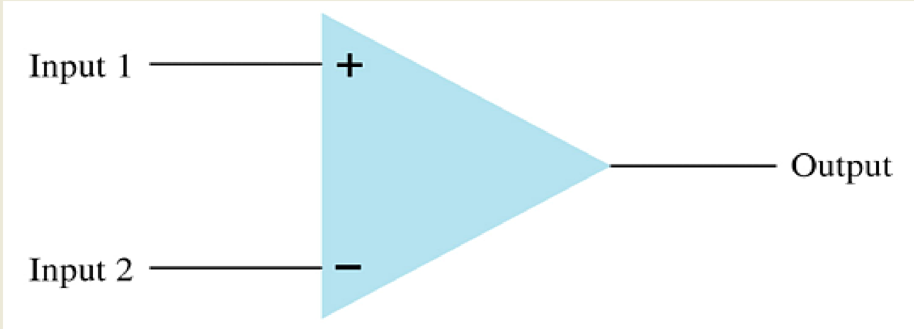
10.1 Introduction

Construction of op-amp

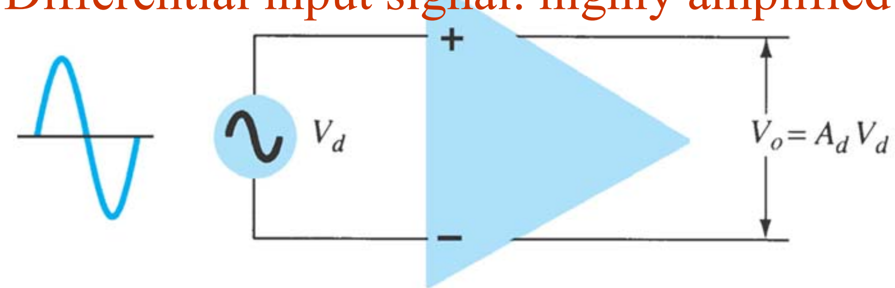
Note the op-amp has two inputs and one output.

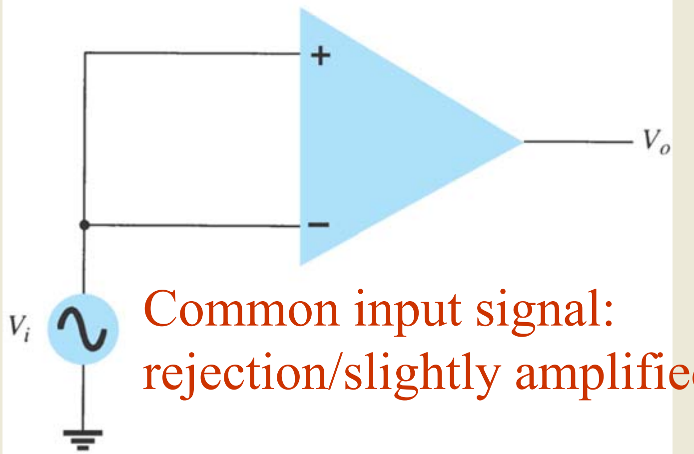


Characteristics of op-amp

- **amplifying the differential signal while rejecting the common signal at the two inputs**
- **very high gain differential amplifier**
- **high input impedance (typically a few meg-Ohms)**
- **low output impedance (less than 100 Ω).**

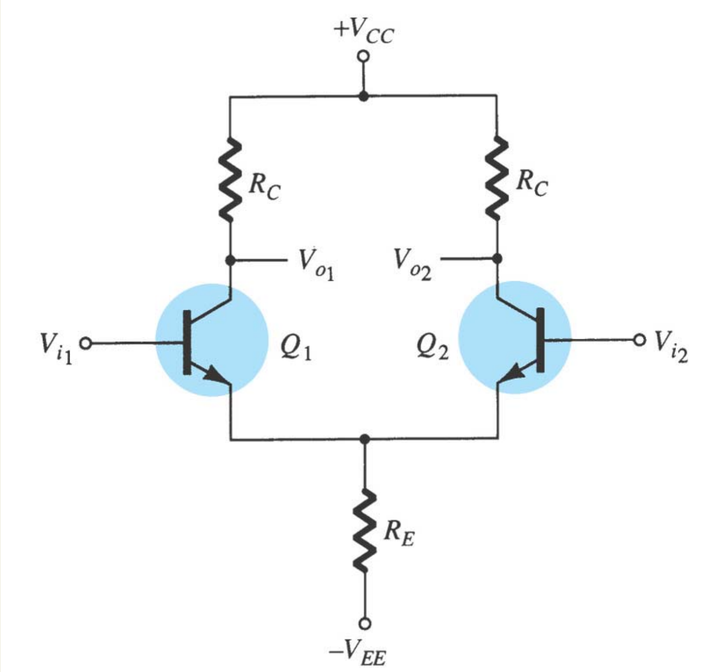
Differential input signal: highly amplified

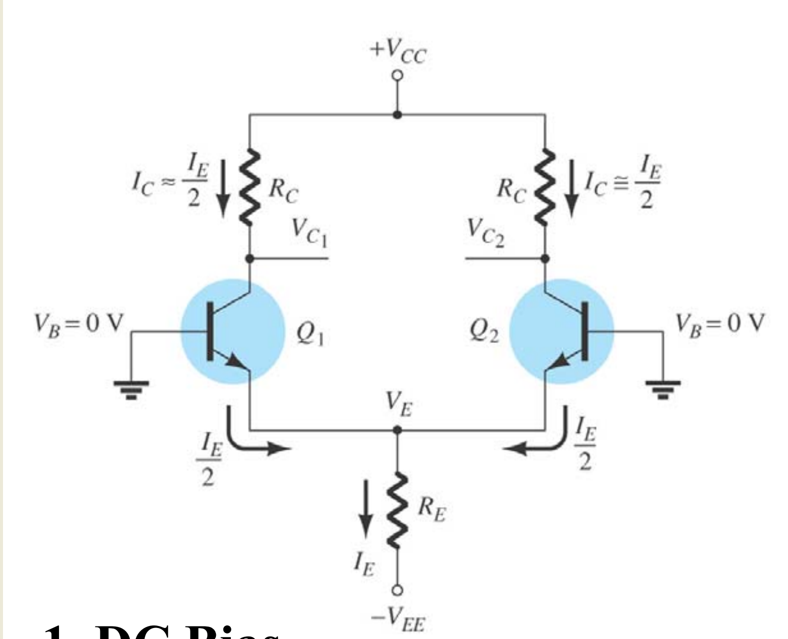




Common input signal: rejection/slightly amplified

10.2 Differential Amplifier Circuit





(1) A fundemental building block of analog ICs.

(2) Two possible inputs and two possible outputs

(3) Identical transistor characteristics of the differntial-pair

(4) Amplifying differential-mode input voltage $V_d=V_{i1}-V_{i2}$, rejecting differential-mode input voltage $V_c=(V_{i1}+V_{i2})/2$

(5) High gain, high input impedance, and low output impedance

Differential Inputs	$V_d = V_{i1} - V_{i2}$
Common Inputs	$V_c = \frac{1}{2}(V_{i1} + V_{i2})$

$\Leftrightarrow$

$$V_{i1} = V_c + \frac{1}{2} V_d$$

$$V_{i2} = V_c - \frac{1}{2} V_d$$

1. DC Bias

$$V_E = -0.7V \qquad I_E = \frac{-0.7V - (-V_{EE})}{R_E}$$

$$I_{C1} = I_{C2} = \frac{I_{EE}}{2} \qquad V_{C1} = V_{C2} = V_{CC} - \frac{I_E}{2} R_C$$

2. AC operation

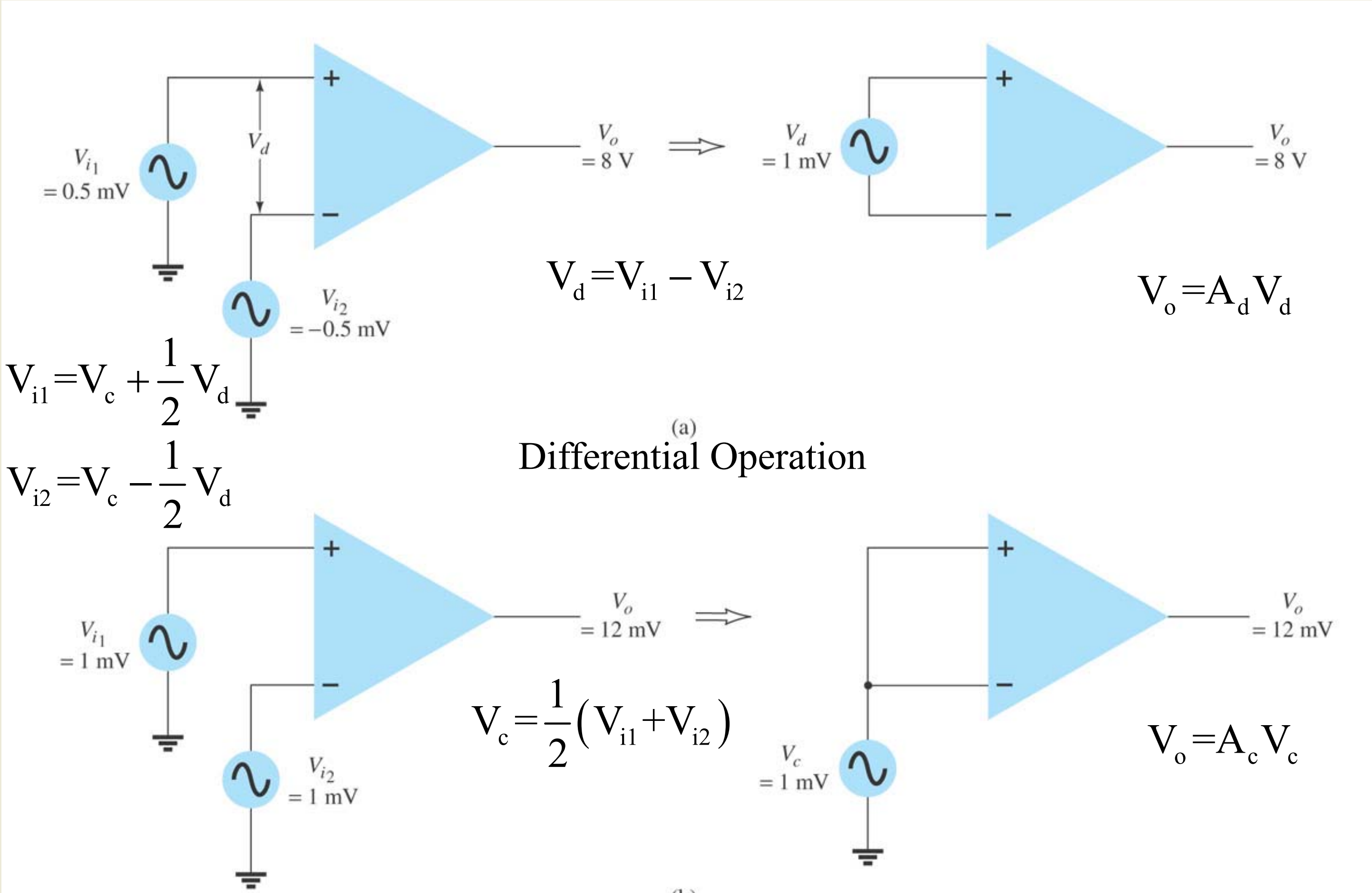
- **Differential-mode operation** $V_o=A_dV_d$

  double ended with input $\frac{V_d}{2}, -\frac{V_d}{2}$

- **Common-mode operation** $V_o=A_cV_c$

  double ended with input V_c, V_c

10.3 Differential And Common-mode Operation



(a) Differential Operation

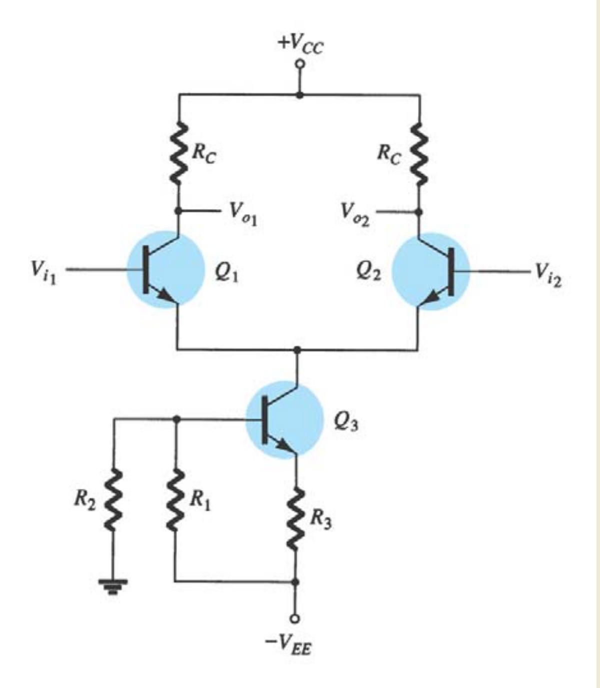
(b) Common-mode Operation

CMRR:

Any signal that is common to both inputs will be cancelled. A measure of the ability to cancel out common signals is called CMRR (common-mode rejection ratio).

$$\text{CMRR} = \frac{A_d}{A_c} \qquad \text{CMRR (log)} = 20 \log_{10} \frac{A_d}{A_c} = A_d(\text{dB}) - A_c(\text{dB})$$

Use of Constant-Current Source



-To provide operating point as well as increasing common-mode rejection ability (provide a large value of the emitter resistance to reduce A_c).

- To be used as active load to improve the differential gain

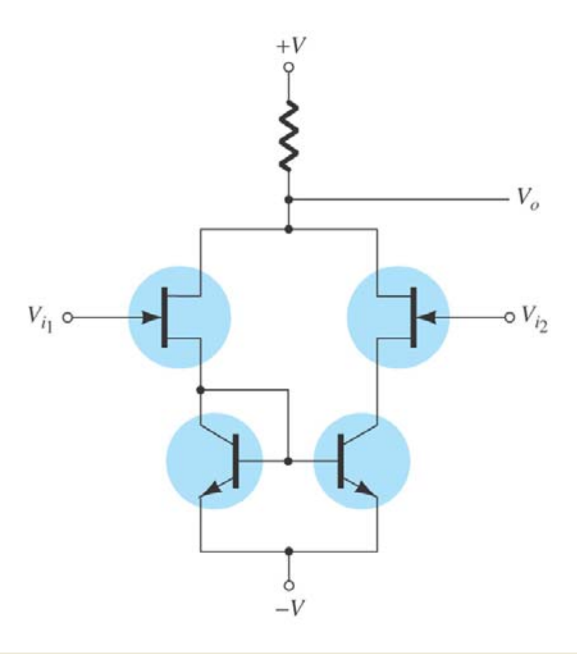
Use of BiFET, BiMOS, and CMOS Differential Amplifier Circuits

-BiFET: a differential amplifier by both BJT and JFET

-BiMOS: a differential amplifier by both BJT and MOSFET

  -Combine BJT and MOS transistors on the same semiconductor chip

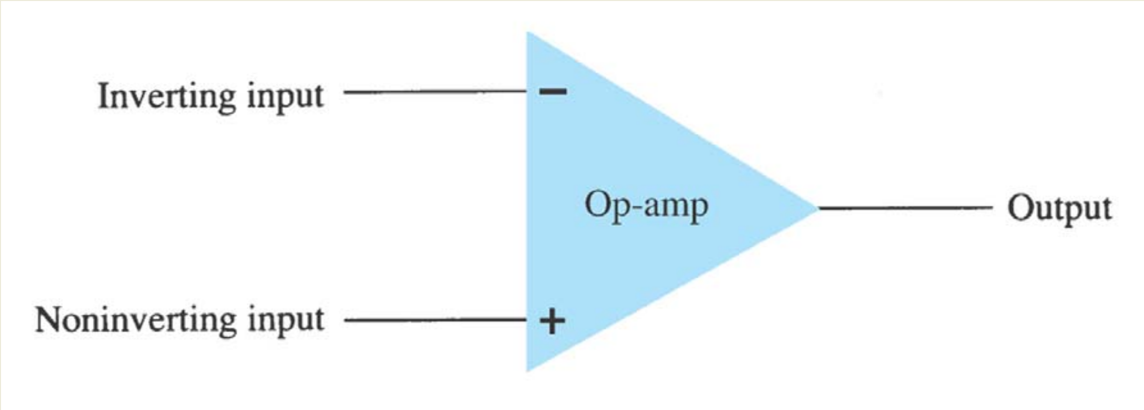
  -The advantages of the MOSFET high input impedance and the BJT high gain can be combined and utilized in the same circuit



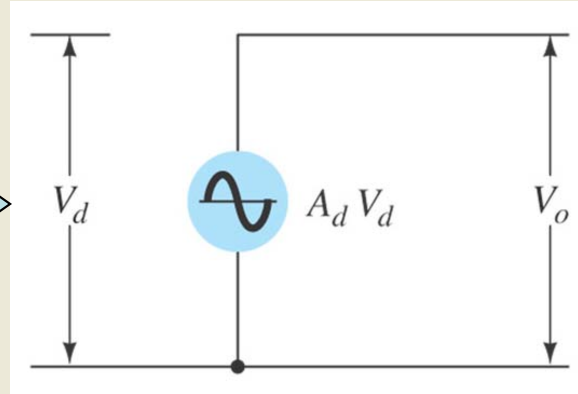
-CMOS: a differential amplifier by complementary type MOSFET

  -Low power dissipation

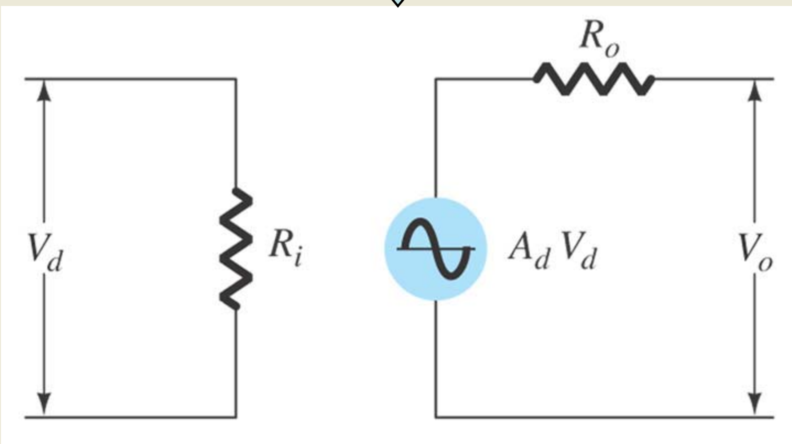
10.5 Op-Amp Basics



Ideal



Practical



Ideal features of op-amp:

- $A_d = \infty$, $A_c = 0$
- $R_i = \infty$
- $R_o = 0$

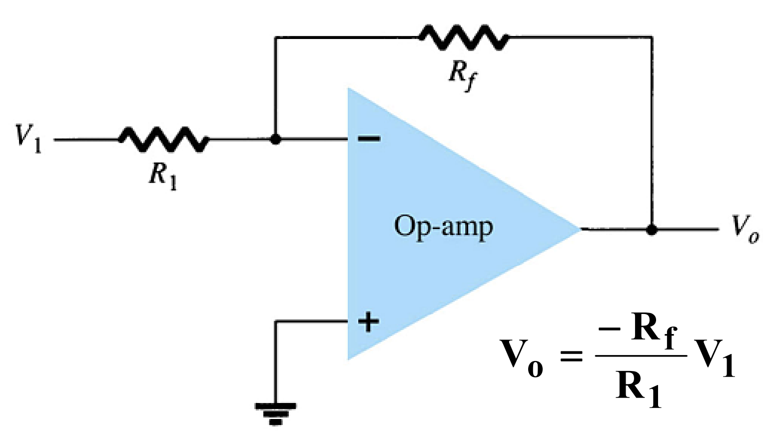
$$V_d = \frac{V_o}{A_d} \Rightarrow \text{Virtual Short: } V_d = 0$$

$$I_d = \frac{V_d}{R_i} \Rightarrow \text{Virtual Open: } I_d = 0$$

Practical features of op-amp:

- very high gain A_d for differential input V_d
- high input impedance R_i (typically a few meg-Ohms)
- low output impedance R_o (less than 100 Ω).

(1) Inverting constant gain amplifier

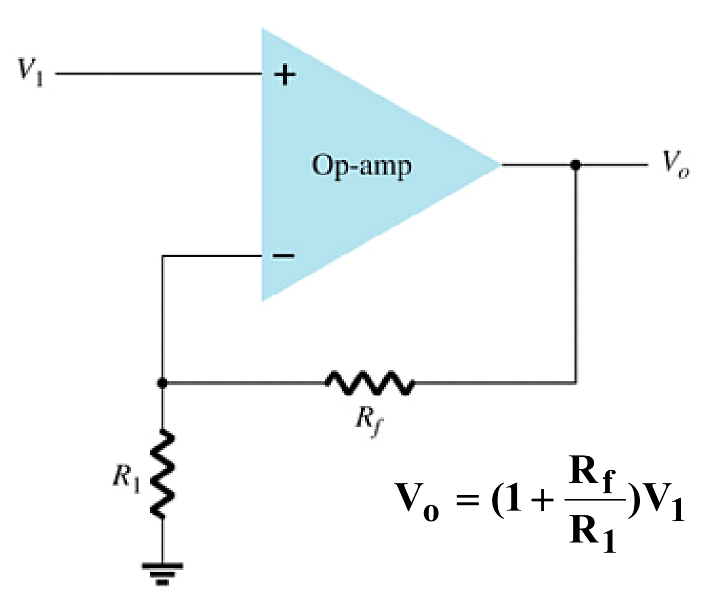


$$V_o = \frac{-R_f}{R_1} V_1$$

- The signal input is applied to the inverting (–) input
- The non-inverting input (+) is grounded
- The resistor R_f is the feedback resistor.

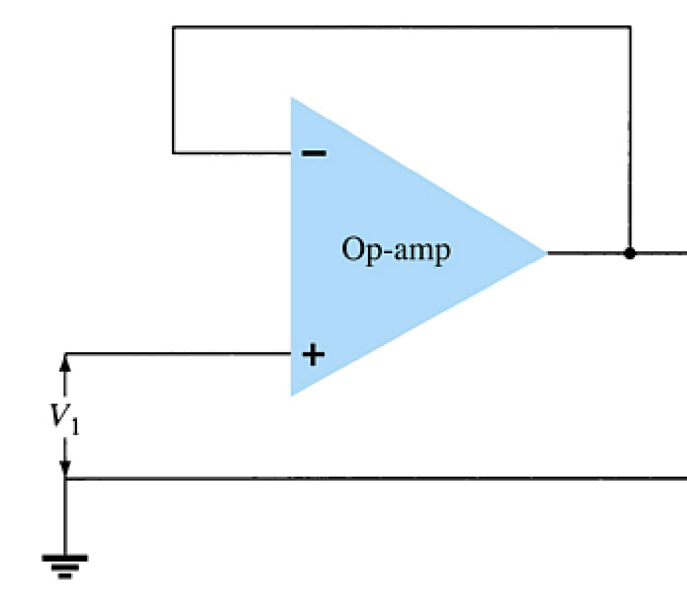
The *non-inverting input* pin is at ground. *The inverting input* pin is also at 0V for an AC signal due to virtual short concept. *The inverting input* is at virtual ground.

(2) Noninverting constant gain amplifier



$$V_o = (1 + \frac{R_f}{R_1}) V_1$$

(3) Unity follower →Voltage buffer



$$V_o = V_1$$

10.6 Op-Amp Specifications—DC Offset Parameters

Even when the input voltage is zero, there will be an output called offset. The following can cause this offset:

- **Input offset voltage (V_{IO})**
- **Input offset current (I_{IO})**

- **Total offset voltage may due to both input offset voltage *and* input offset current**

$$V_o(\text{offset}) = Vo(\text{offset due to } V_{IO}) + V_o(\text{offset due to } I_{IO})$$

- **Input bias current (I_{IB})**

$$I_{IB}^{-} = I_{IB} - \frac{I_{IO}}{2} \qquad I_{IB}^{+} = I_{IB} + \frac{I_{IO}}{2} \qquad I_{IB} = \frac{I_{IB}^{-} + I_{IB}^{+}}{2}$$

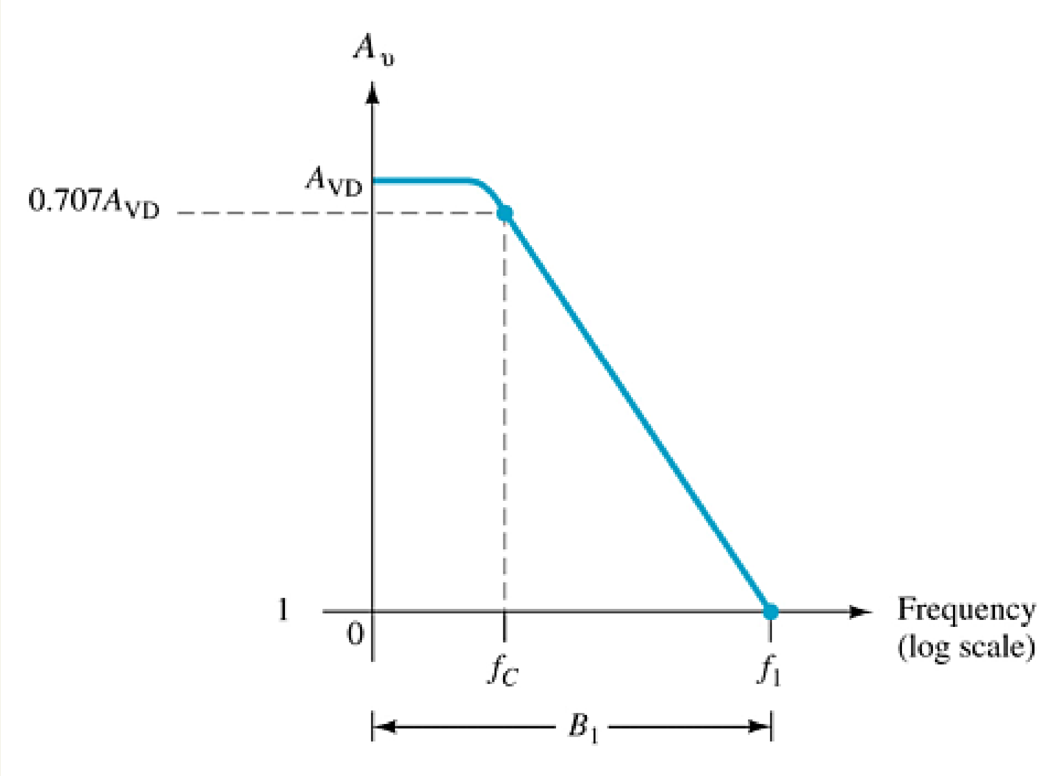
In experiments and actual applications, adjusting circuits for zero-input zero-output is employed.

10.7 Op-Amp Specifications—Frequency Parameters

An op-amp is a wide-bandwidth amplifier. The following affect the bandwidth of the op-amp:

- **Gain**
- **Slew rate**

• The plot shown is for an open loop gain (A_{OL} or A_{VD}).
• The op-amp's high frequency response is limited by internal circuitry.
• In the open loop, the op-amp has a narrow bandwidth.
• The bandwidth widens in closed-loop operation, but then the gain is lower.



$$f = f_1, \quad A_{VD} = 1$$

$$f = f_c, \quad A_{VD} = 0.707A_{VD0}$$

$$f_1 = f_c A_{VD0}$$

f_1 is called the gain-bandwidth

Summary of Chapter 10

- Characteristics of Differential Amplifier
    - Differential mode operation
    - Common mode operation
    - CMRR
- Characteristics of Op-Amp.
    - Ideal assumptions (Virtual short and Virtual open)
    - Practical
- Linear applications of Op-Amp
    - Inverting and nuninverting amplifier
    - Unity follower