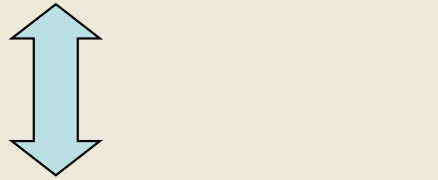
FET Amplifiers

- Excellent voltage gain
- High input impedance
- Low-power consumption
- Good frequency range

Chapter 7: FET Biasing

Chapter 8: FET Amplifiers



Step 1: DC analysis
Based on DC network:
- V_{GSQ}
- I_{DQ}
- V_{DSQ}

Using V_{GSQ} to determine g_m for AC equivalent model

Step 2: AC analysis
Based on AC network and AC equivalent model:
- **Input impedance**
- **Output impedance**
- **Voltage gain**

Three basic configurations for FET amplifiers

CS: Common Source Configuration

CG: Common Gate Configuration

Source Follower: Common Drain

Common FET Biasing Circuits

JFET

- Fixed-Bias
- Self-Bias
- Voltage-Divider Bias

Depletion-Type MOSFET

- Self-Bias
- Voltage-Divider Bias

Enhancement-Type MOSFET

- Feedback Configuration
- Voltage-Divider Bias

DC analysis methods: V_{GSQ}, I_{DQ}, V_{DSQ}

- Mathematical approach
- Graphical approach

General Relationships

For all FETs:

$$I_G \cong 0A$$

$$I_D = I_S$$

For JFETS and depletion-type MOSFETs:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

7.2 Fixed-Bias Configuration

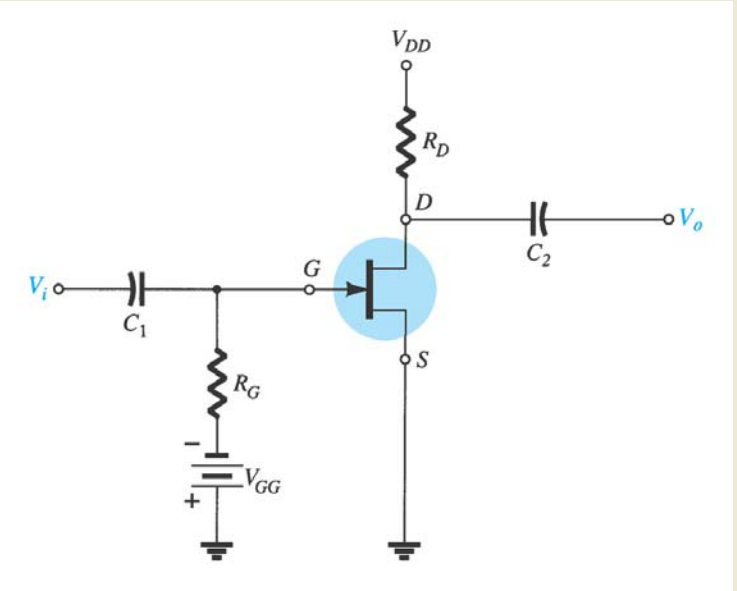
Mathematical Approach

$$I_G \cong 0A$$

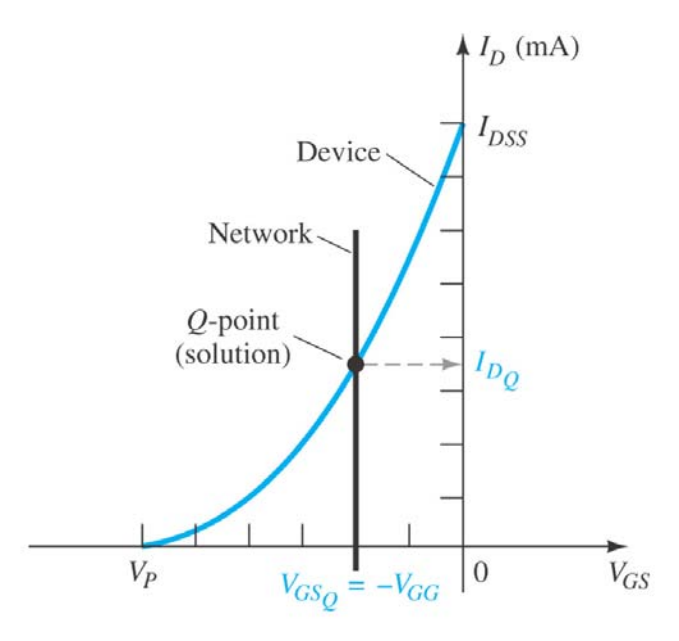
$$V_{GSQ} = -V_{GG}$$

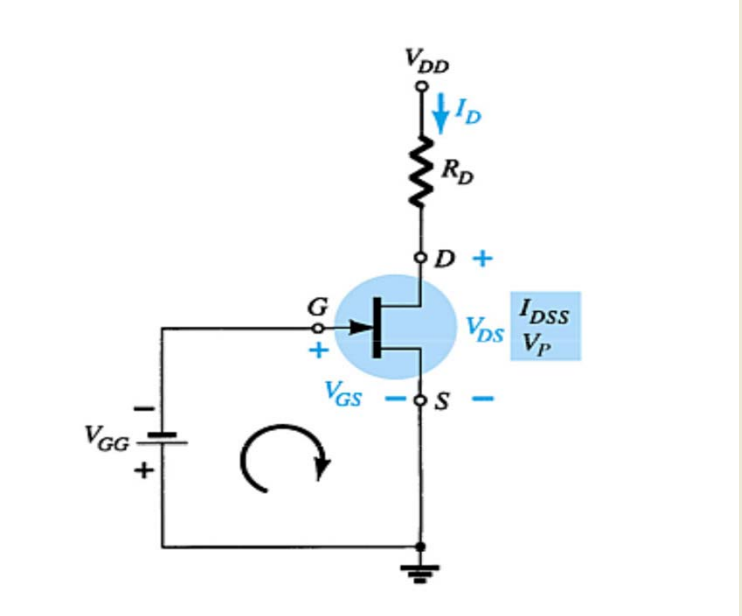
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \rightarrow I_{DQ}$$

$$V_{DS} = V_{DD} - I_D R_D \rightarrow V_{DSQ}$$



Graphical Approach





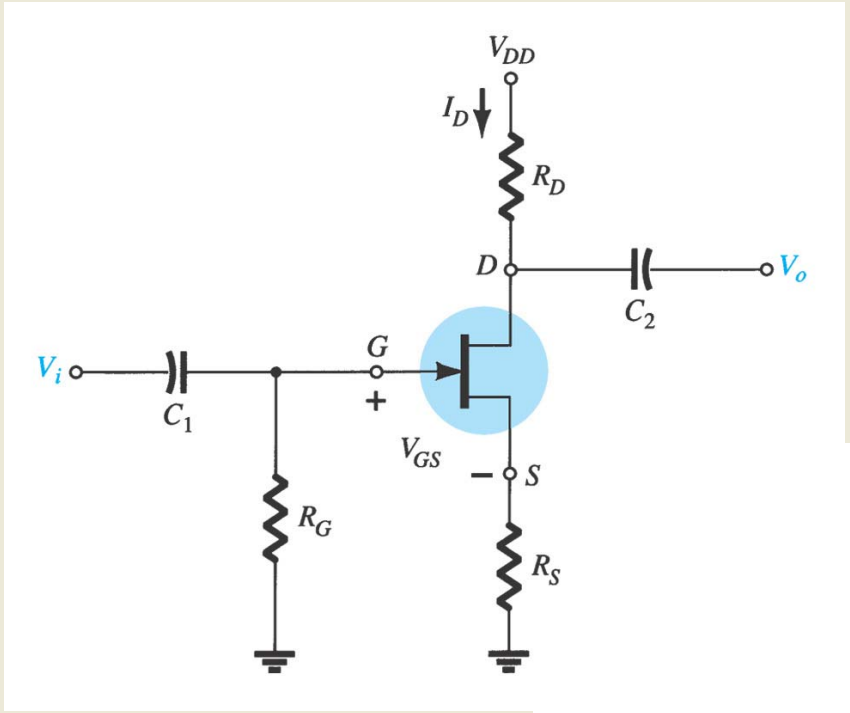
7.3 Self-Bias Configuration

Mathematical Approach

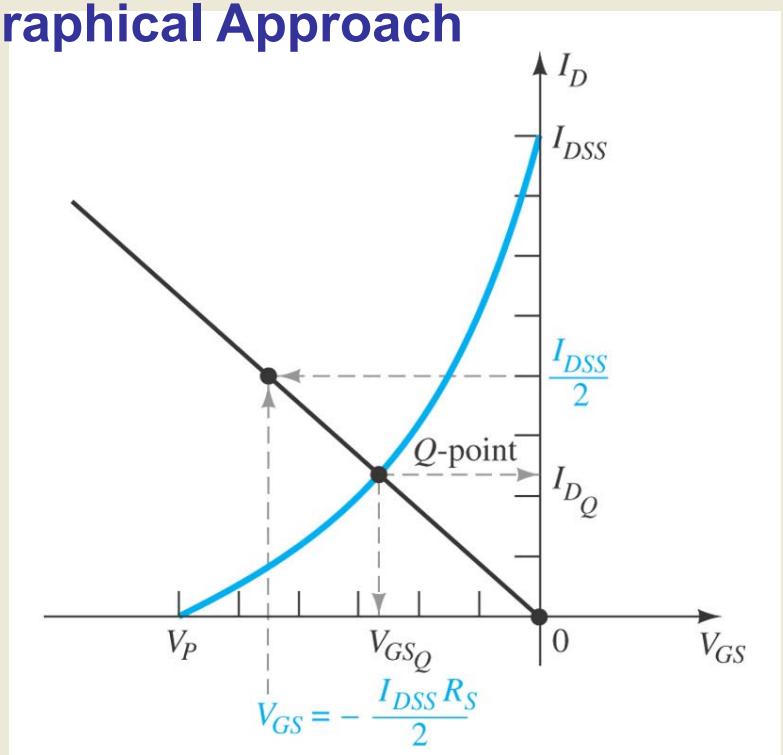
$$I_G \cong 0A, \quad I_D = I_S$$

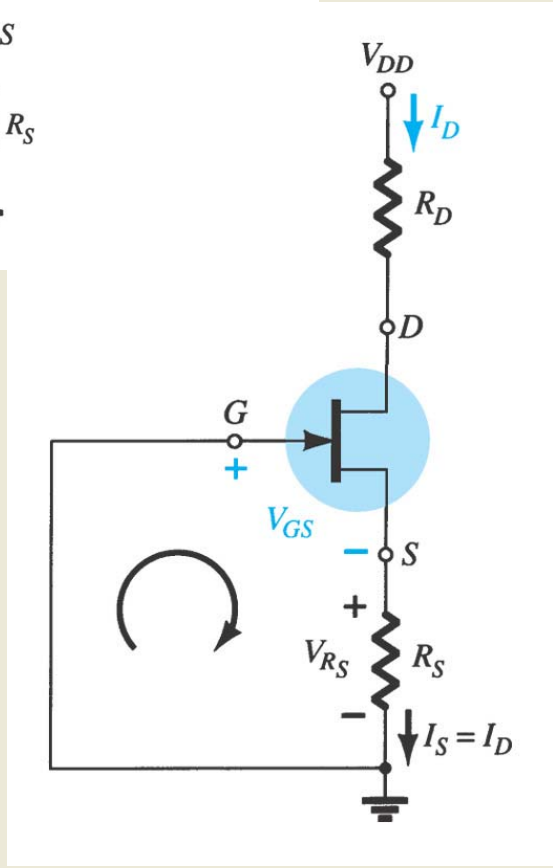
$$\left.\begin{aligned} V_{GS} &= -I_D R_S \\ I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \end{aligned}\right\} \Rightarrow V_{GSQ}, I_{DQ}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_s) \rightarrow V_{DSQ}$$



Graphical Approach





7.4 Voltage-Divider Biasing

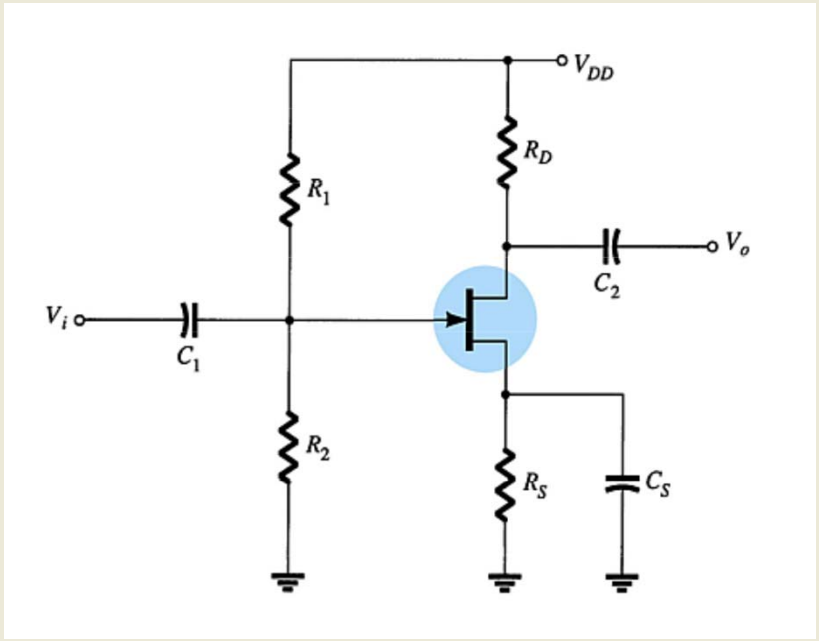
Mathematical Approach

$$I_G \cong 0A, \quad I_D = I_S$$

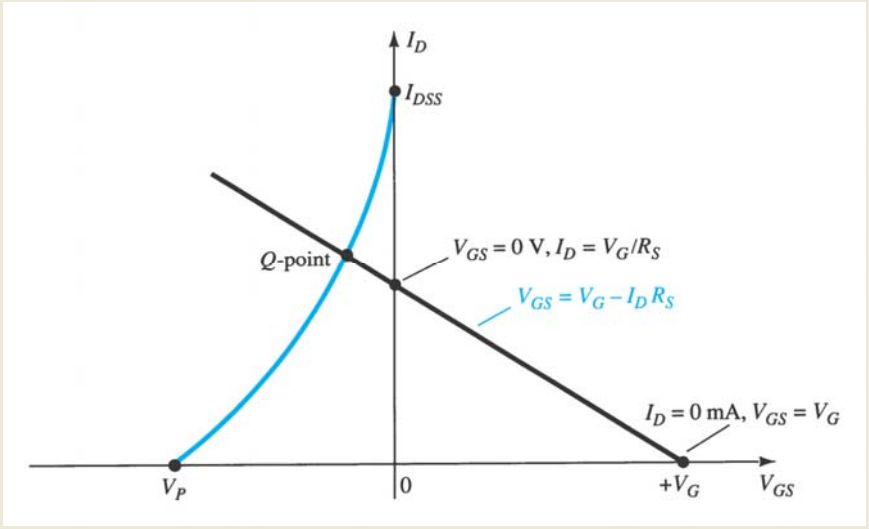
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

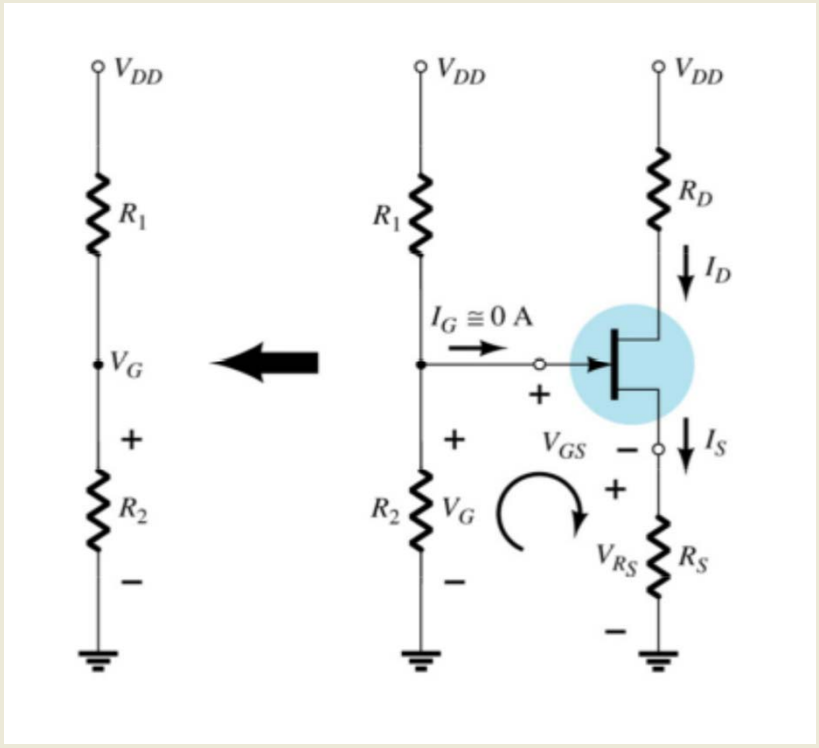
$$\left.\begin{aligned} V_{GS} &= V_G - I_D R_S \\ I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \end{aligned}\right\} \Rightarrow V_{GSQ}, I_{DQ}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_s) \rightarrow V_{DSQ}$$



Graphical Approach





7.6 Feedback Biasing for E-MOSFETs

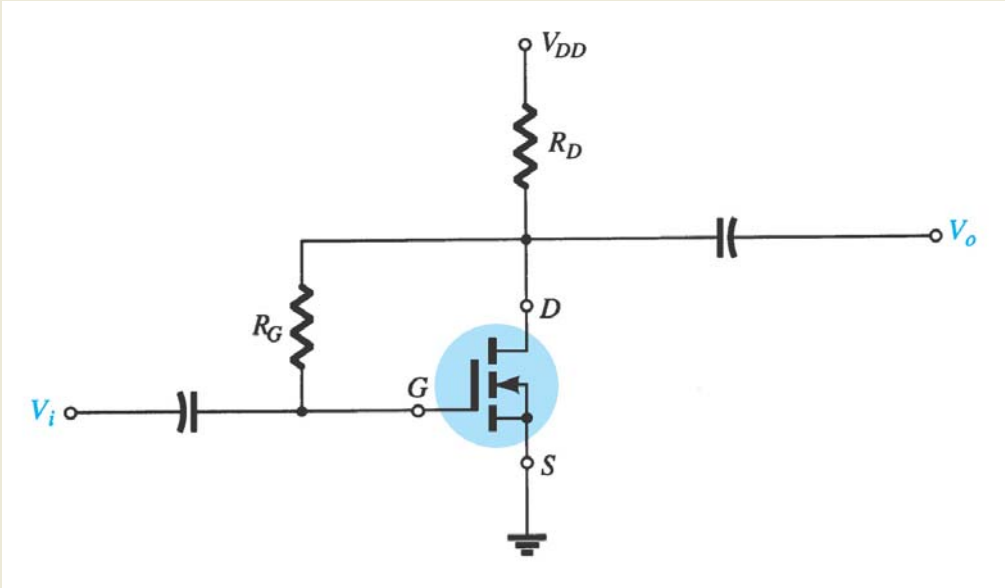
Mathematical Approach

$$I_G \cong 0A, \quad V_D = V_G$$

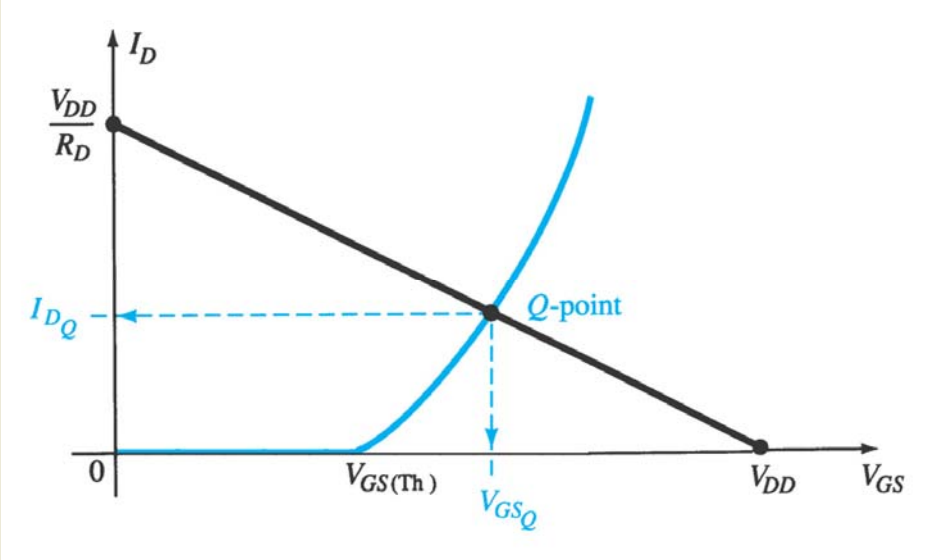
$$V_{GS} = V_{DS}$$

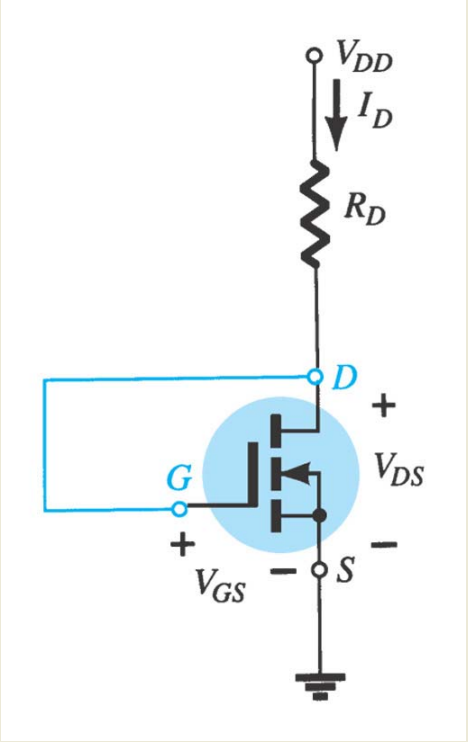
$$\left.\begin{aligned} V_{GS} &= V_{DD} - I_D R_D \\ I_D &= k\left(V_{GS} - V_{GS(TH)}\right)^2 \end{aligned}\right\} \Rightarrow V_{GSQ}, I_{DQ}$$

$$V_{DS} = V_{DD} - I_D R_D \rightarrow V_{DSQ}$$



Graphical Approach





8.2 FET Small-Signal Model

Transconductance

The relationship of $V_{GS(input)}$ to $I_{D(output)}$) is called transconductance denoted by g_m.

Mathematical Determinations of g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

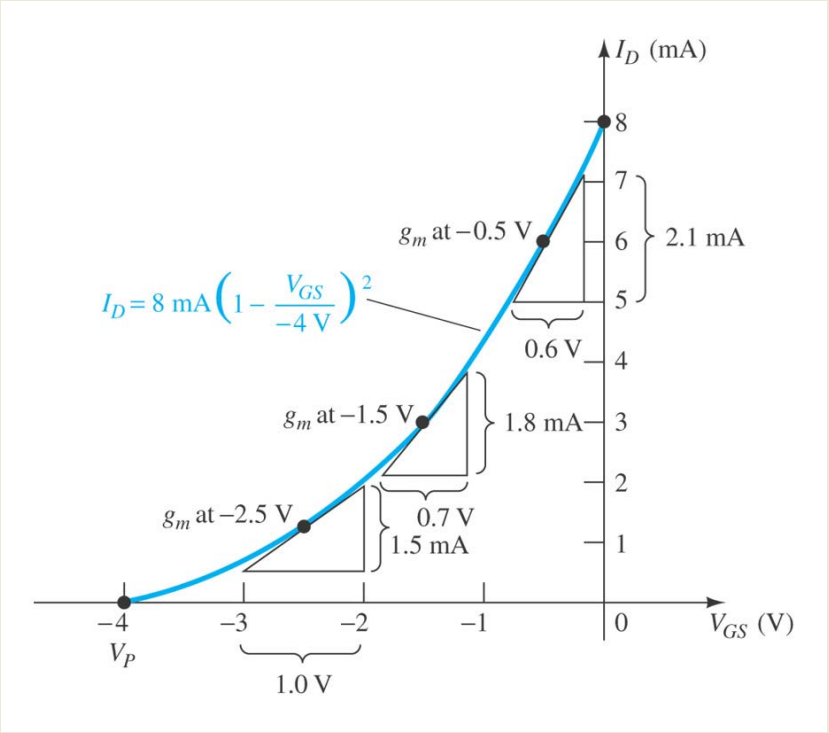
Where V_{GS} =0V $\quad g_{m0} = \dfrac{2I_{DSS}}{|V_P|}$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

Where $\quad 1 - \dfrac{V_{GS}}{V_P} = \sqrt{\dfrac{I_D}{I_{DSS}}}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

Graphical Determination of g_m



With a small signal input, FET acts as a linear device: $I_d = g_m V_{gs}$

FET Impedance

Input impedance:

$$Z_i = \infty\Omega$$

Output Impedance:

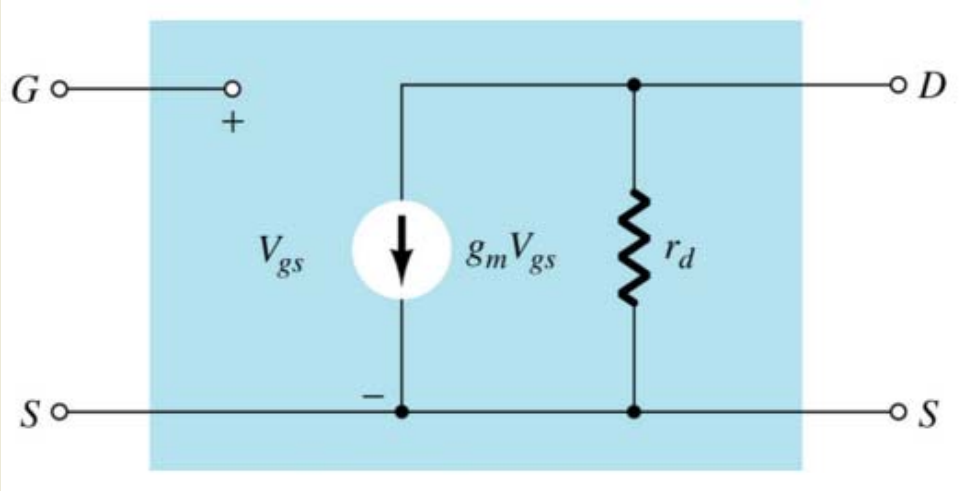
$$Z_o = r_d = \frac{1}{y_{os}}$$

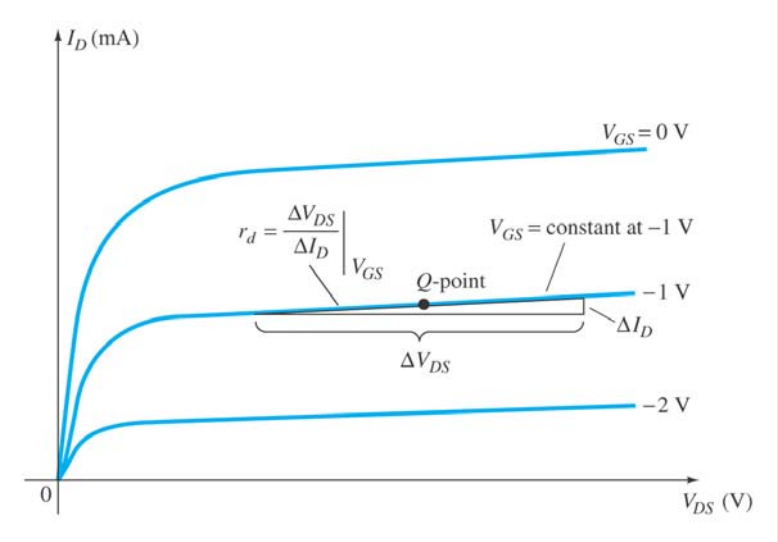
where:

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}=\text{constant}}$$

y_{os}= admittance equivalent circuit parameter listed on FET specification sheets.

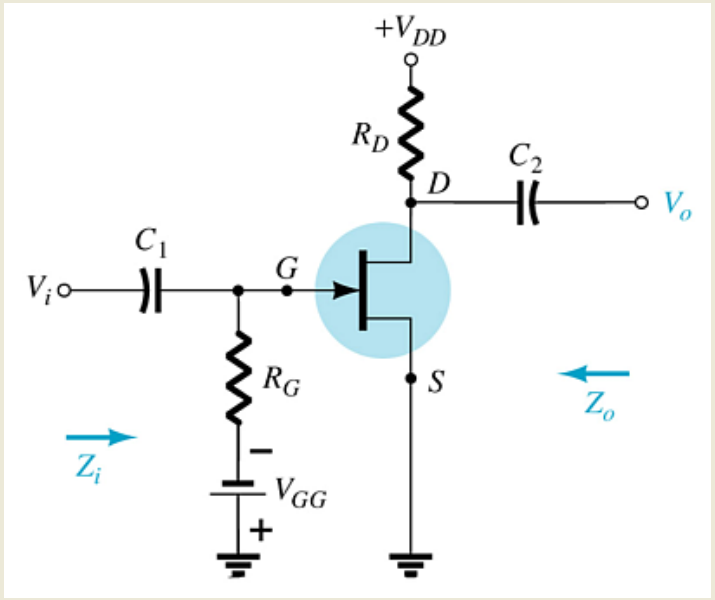
FET AC Equivalent Circuit





8.3 JFET Common-Source (CS) Fixed-Bias Configuration

The input is on the gate and the output is on the drain



Input impedance:

$$Z_i = R_G$$

Output impedance:

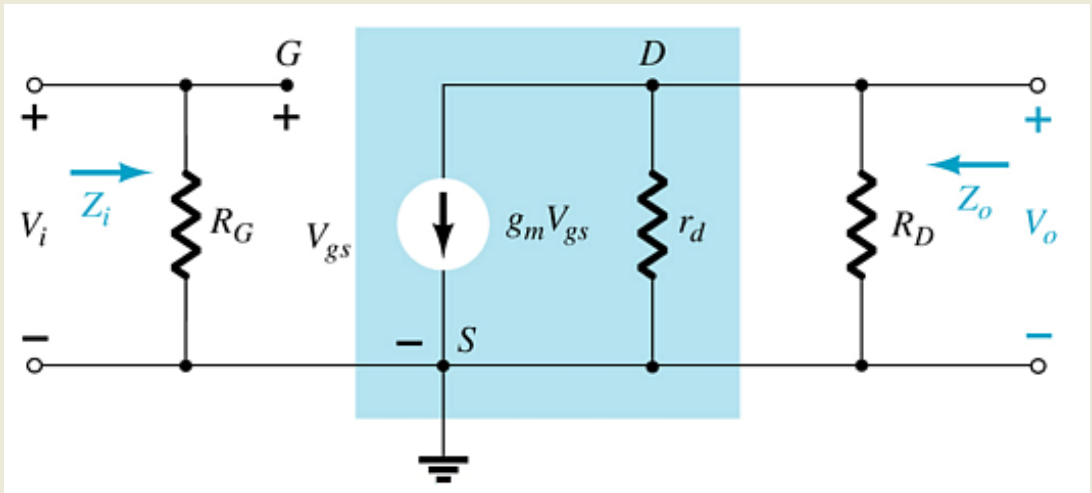
$$Z_o = R_D \| r_d$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

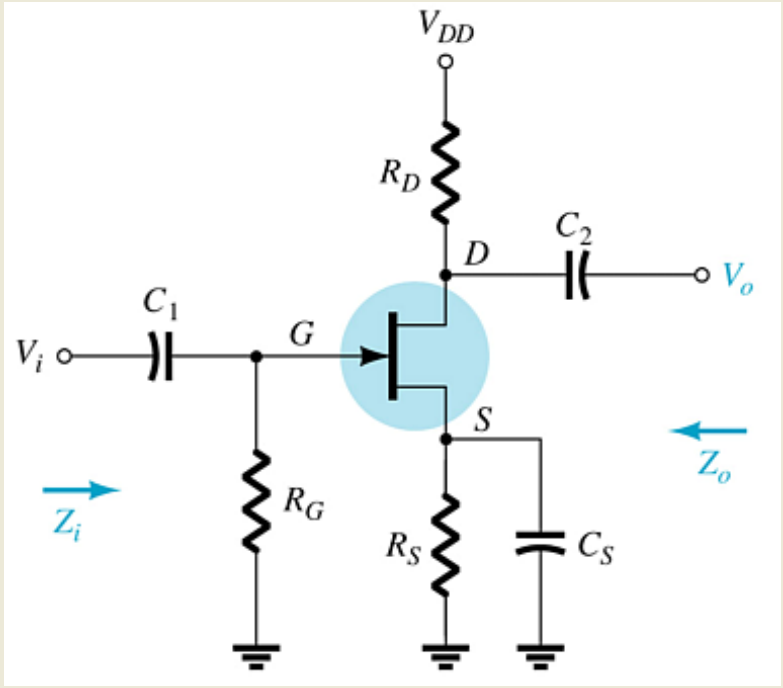
$$A_v = \frac{V_o}{V_i} = -g_m R_D \Big|_{r_d \geq 10R_D}$$



CS: There is a 180° phase shift between input and output

8.4 JFET Common-Source Self-Bias Configuration

The input is on the gate and the output is on the drain



Input impedance:

$$Z_i = R_G$$

Output impedance:

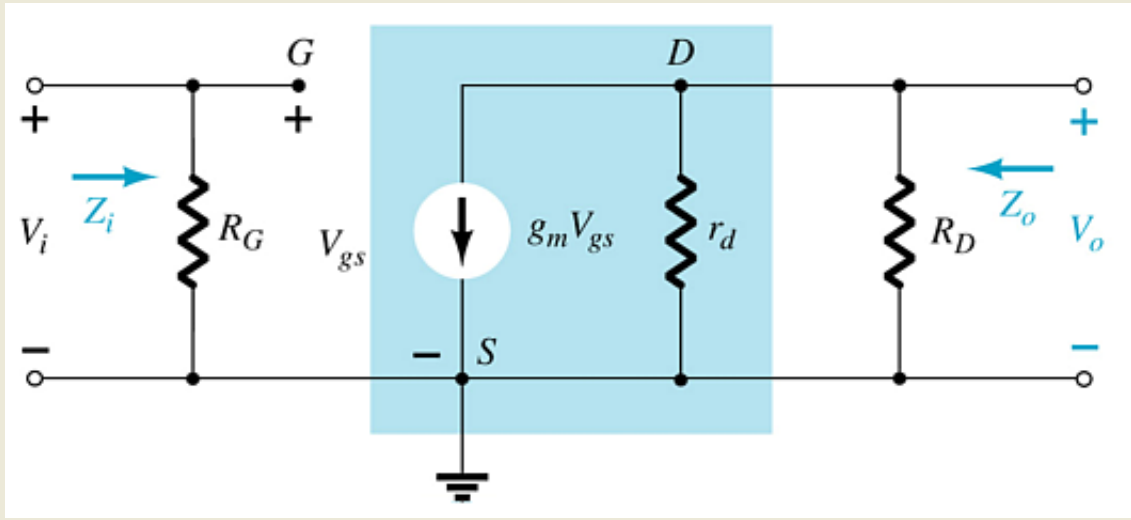
$$Z_o = r_d \,\|\, R_D$$

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

Voltage gain:

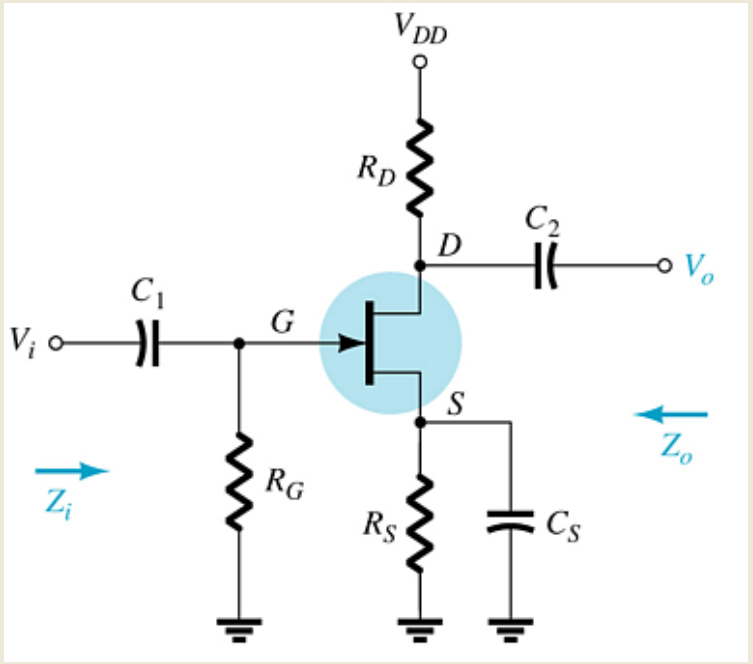
$$A_v = -g_m(r_d \,\|\, R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$



JFET Common-Source Self-Bias Configuration

Removing C_s affects the gain of the circuit.

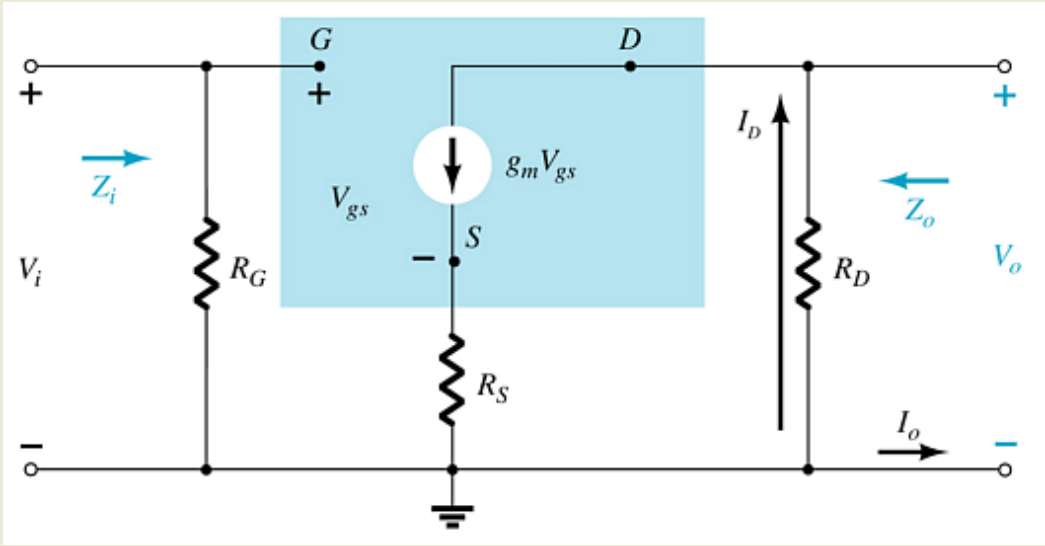


Input impedance:

$$Z_i = R_G$$

Output impedance:

$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$



Voltage gain:

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S}\Bigg|_{r_d \geq 10(R_D + R_S)}$$

8.5 JFET CS Voltage-Divider Configuration

The input is on the gate and the output is on the drain.

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

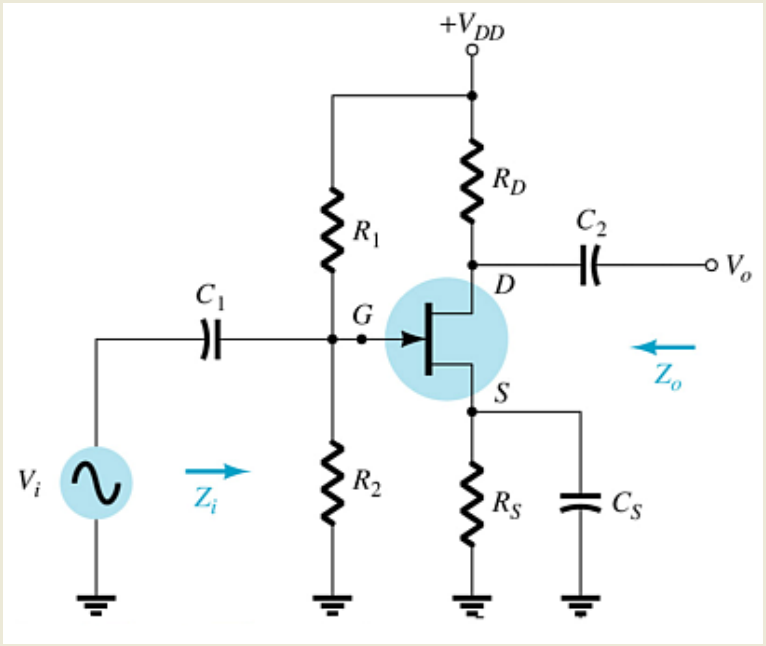
$$Z_o = r_d \| R_D$$

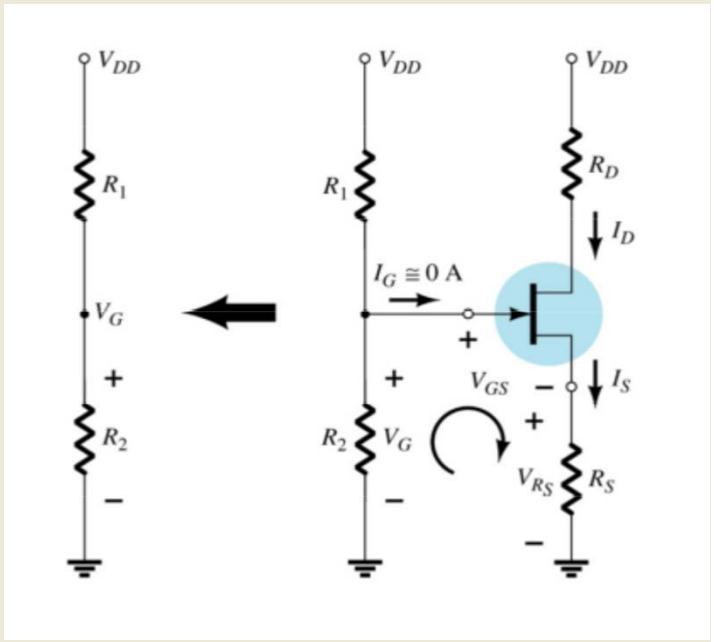
$$Z_o \cong R_D \Big|_{r_d \geq 10R_D}$$

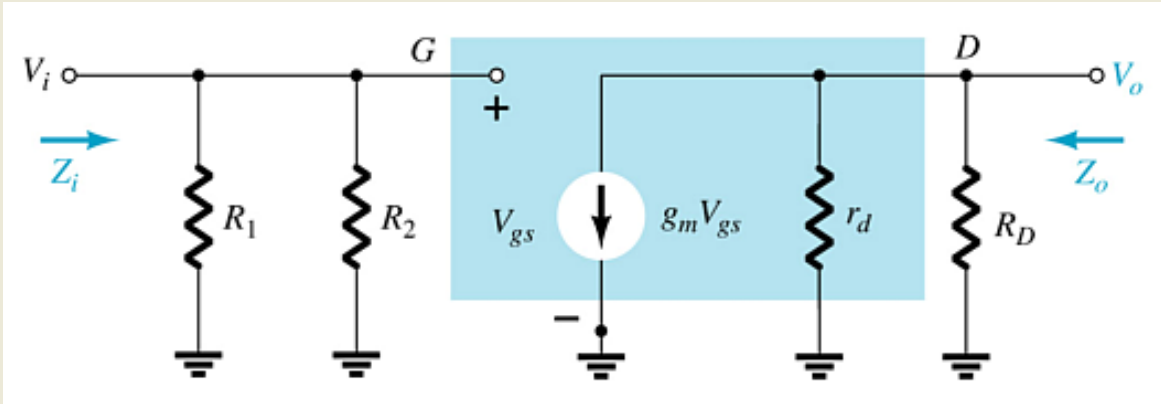
Voltage gain:

$$A_v = -g_m(r_d \| R_D)$$

$$A_v = -g_m R_D \Big|_{r_d \geq 10R_D}$$



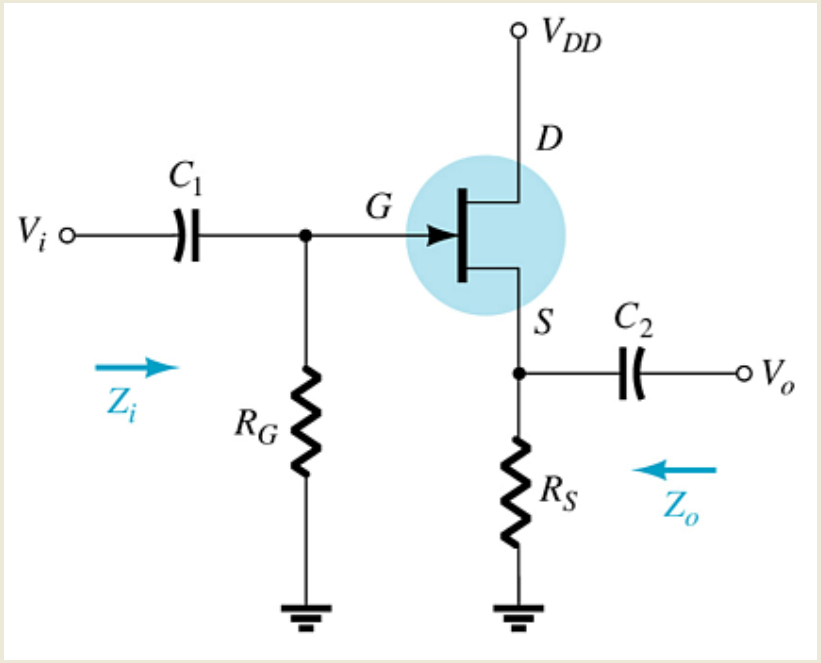




8.6 JFET Source Follower (Common-Drain) Configuration

In a common-drain amplifier configuration, the input is on the gate, but the output is from the source.

There is no phase shift between input and output.



Input impedance:

$$Z_i = R_G$$

Output impedance:

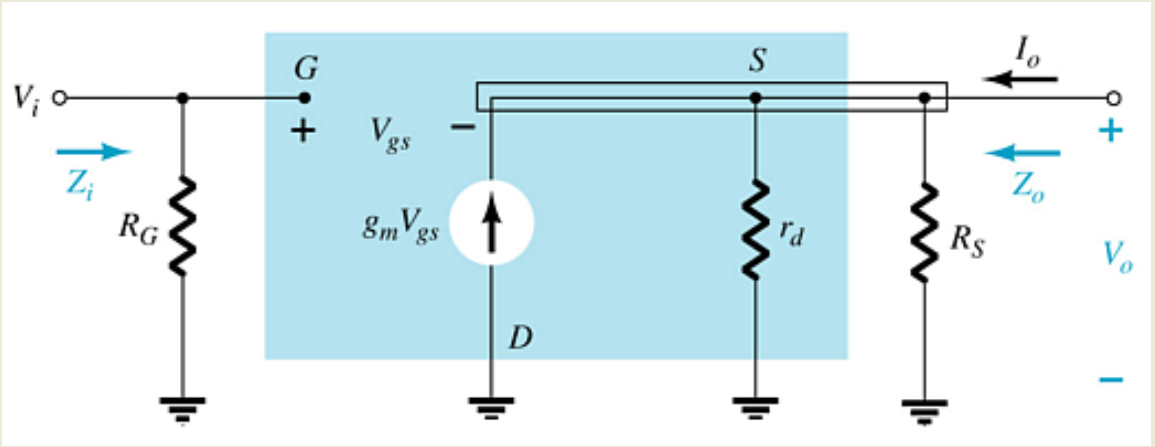
$$Z_o = r_d \parallel R_S \parallel \frac{1}{g_m}$$

$$Z_o \cong R_S \parallel \frac{1}{g_m} \Big|_{r_d \geq 10R_S}$$

Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \parallel R_S)}{1 + g_m(r_d \parallel R_S)}$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \Big|_{r_d \geq 10}$$



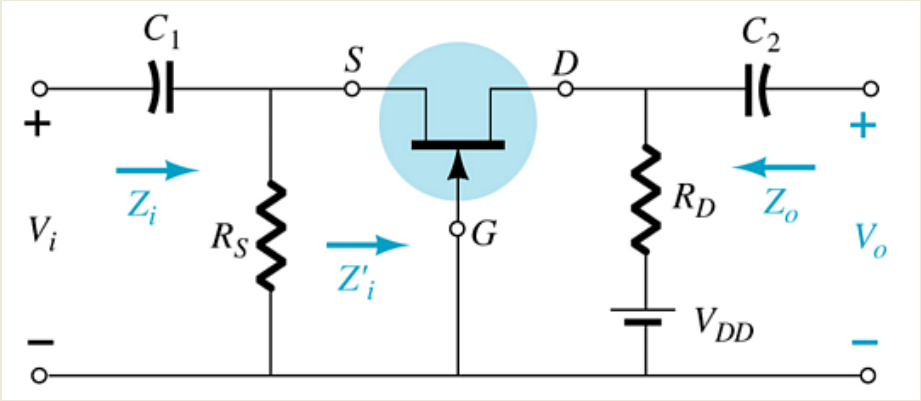
8.7 JFET Common-Gate Configuration

The input is on the source and the output is on the drain.

Input impedance:

$$Z_i = R_S \parallel \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

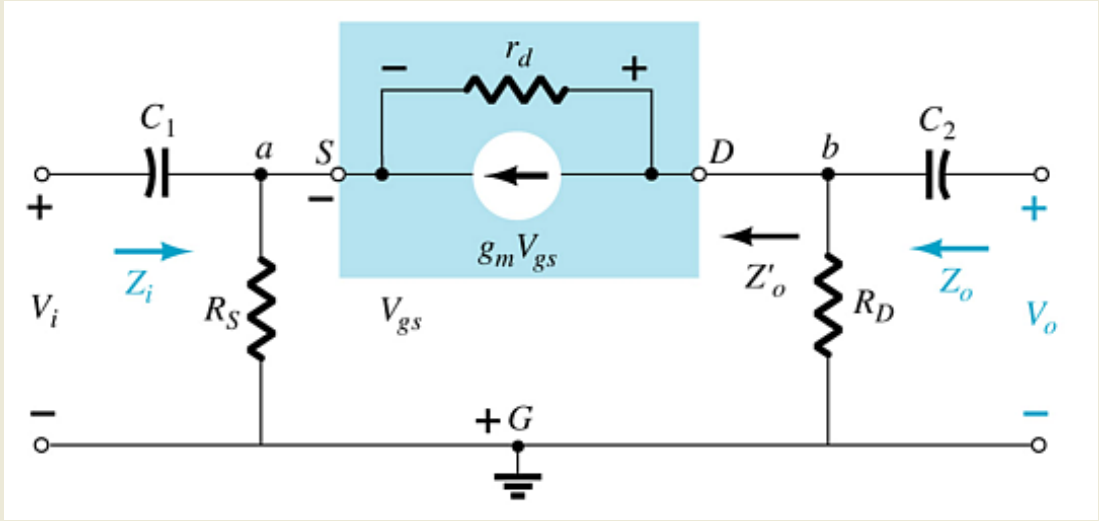
$$Z_i \cong R_S \parallel \frac{1}{g_m}\Big|_{r_d \geq 10R_D}$$



Output impedance:

$$Z_o = R_D \parallel r_d$$

$$Z_o \cong R_D\Big|_{r_d \geq 10}$$



Voltage gain:

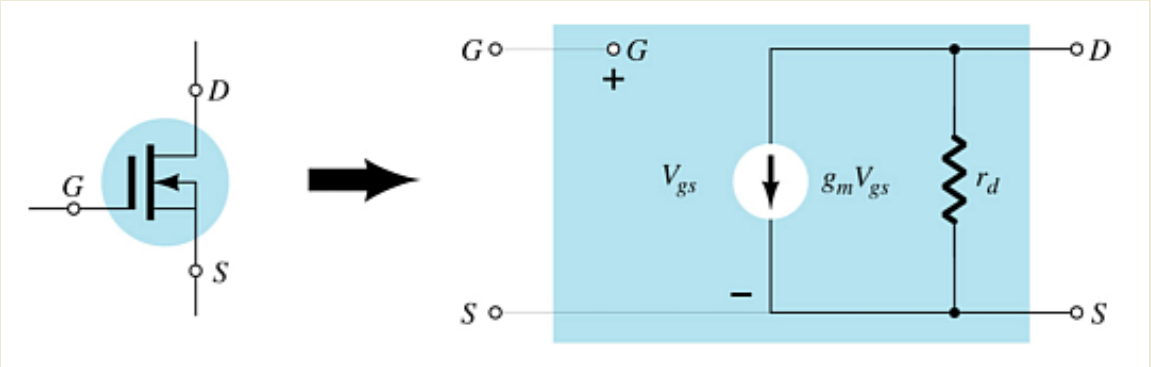
$$A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \frac{R_D}{r_d}\right]}{\left[1 + \frac{R_D}{r_d}\right]}$$

$$A_v = g_m R_D\Big|_{r_d \geq 10R_D}$$

There is no phase shift between input and output.

8.8 Depletion-Type MOSFETs

- D-MOSFETs have the same AC equivalent model and same equation for g_m with JFETs .
- The only difference is that V_{GSQ} can be positive for *n*-channel devices and negative for *p*-channel devices. This means that g_m can be greater than g_{m0}.



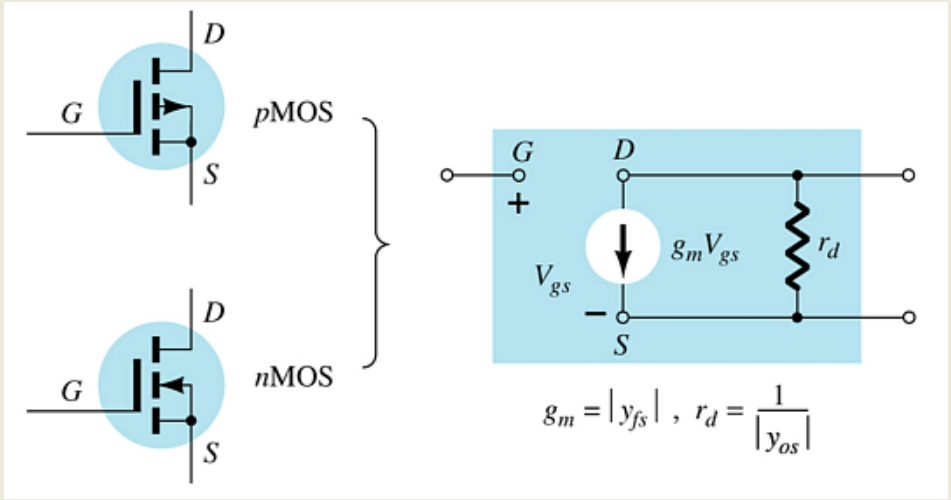
8.9 Enhancement-Type MOSFETs

- E-MOSFETs have the similar AC equivalent model with JFETs .
- Equation for g_m is different.

Transfer equation for E-MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_Q \qquad g_m = 2k(V_{GSQ} - V_{GS(Th)})$$



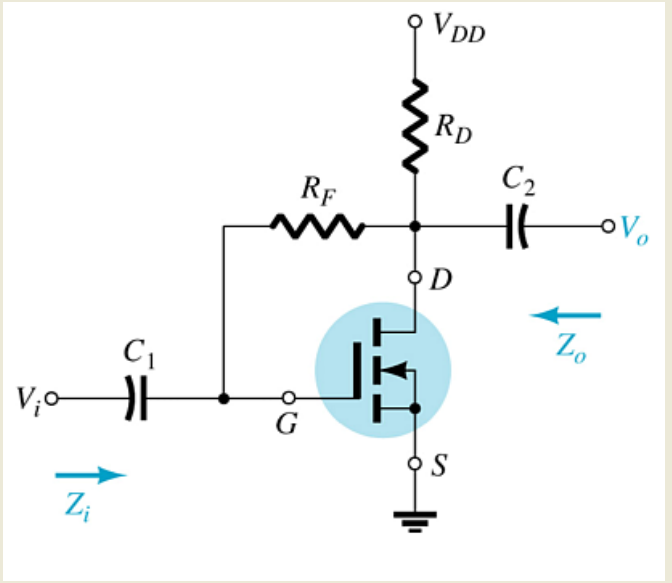
8.10 E-MOSFET CS Drain-Feedback Configuration

There is a 180° phase shift between input and output for CS amplifiers.

Input impedance:

$$Z_i = \frac{R_F + r_d \,||\, R_D}{1 + g_m (r_d \,||\, R_D)}$$

$$Z_i \cong \frac{R_F}{1 + g_m R_D} \Big|_{R_F >> r_d \,||\, R_D,\, r_d \geq 10 R_D}$$



Output impedance:

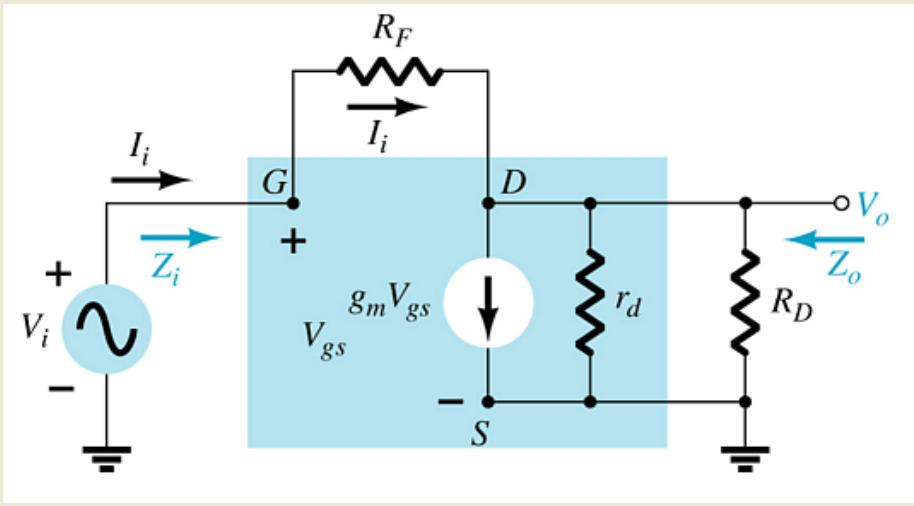
$$Z_o = R_F \,||\, r_d \,||\, R_D$$

$$Z_o \cong R_D \Big|_{R_F >> r_d \,||\, R_D,\, r_d \geq 10 R_D}$$

Voltage gain:

$$A_v = -g_m (R_F \,||\, r_d \,||\, R_D)$$

$$A_v \cong -g_m R_D \Big|_{R_F >> r_d \,||\, R_D,\, r_d \geq 10 R_D}$$



8.11 E-MOSFET CS Voltage-Divider Configuration

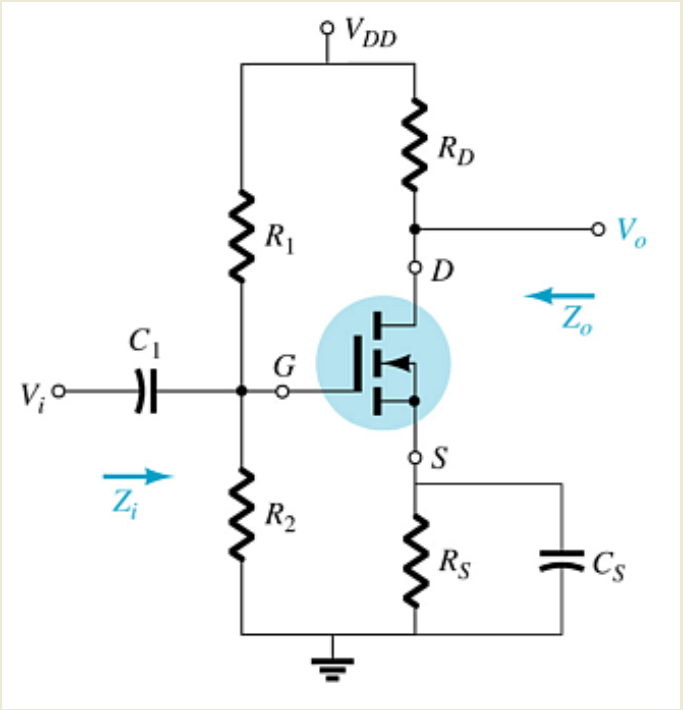
Input impedance:

$$Z_i = R_1 \| R_2$$

Output impedance:

$$Z_o = r_d \| R_D$$

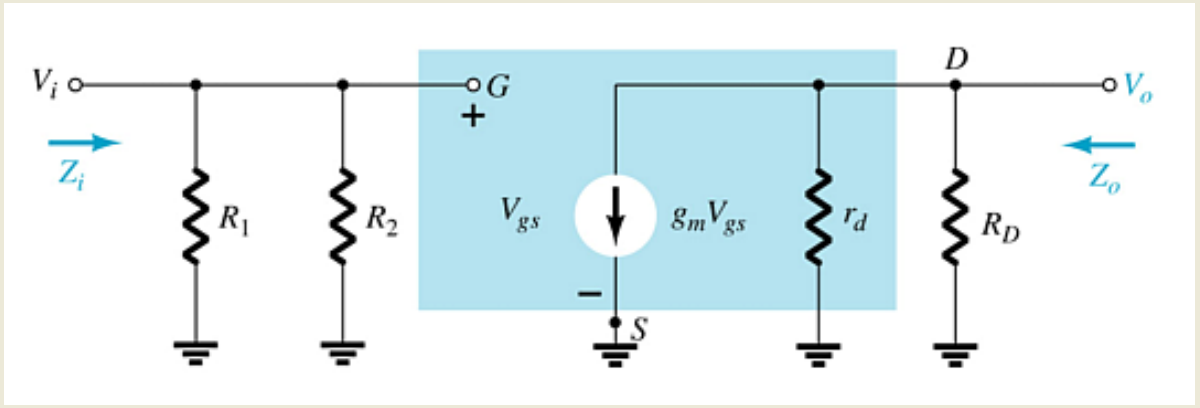
$$Z_o \cong R_D \Big|_{r_d \geq 10}$$



Voltage gain:

$$A_v = -g_m (r_d \| R_D)$$

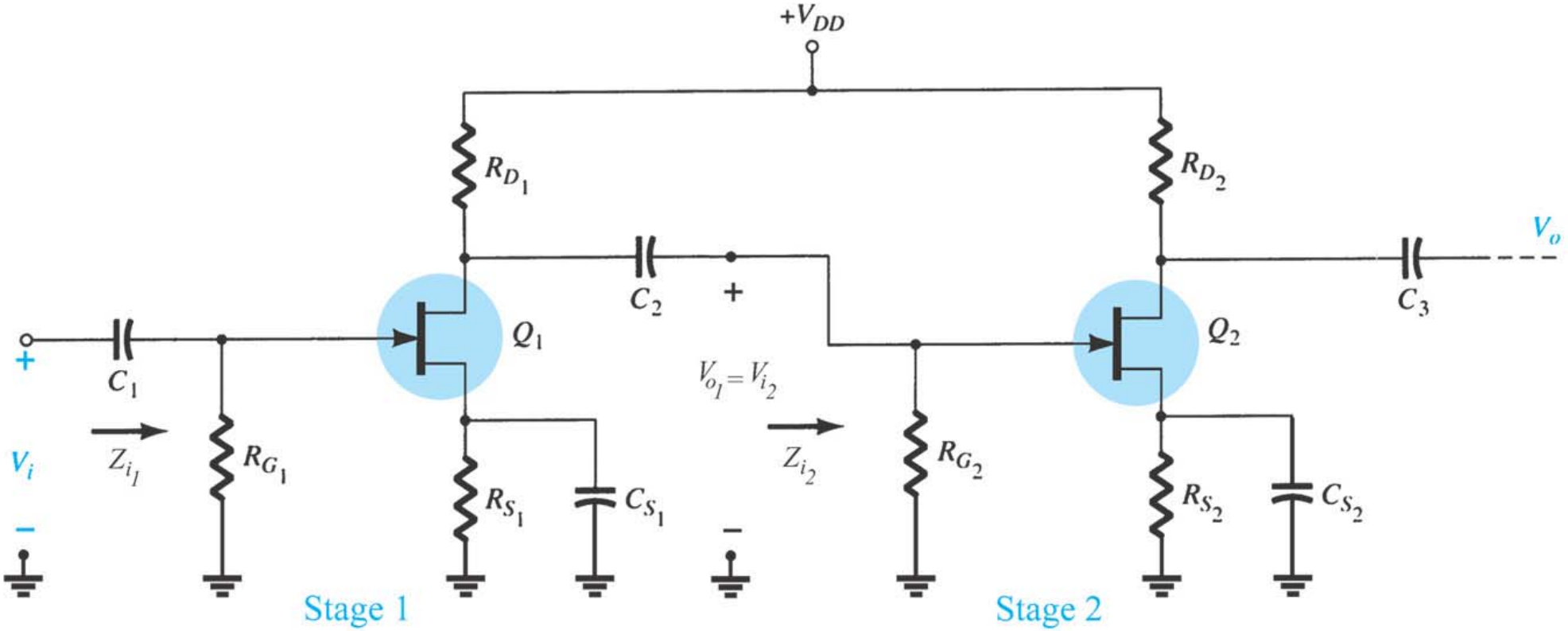
$$A_v \cong -g_m R_D \Big|_{r_d \geq 10 R_D}$$



8.13 Effect of R_L and R_S

8.14 Cascade Configuration

Note: Methods and conclusions are the same with that for BJT amplifiers in 5.16, 5.19.



Summary of FET Amplifiers

- **Comparisons of FETs and BJTs**
  - **Voltage controlled**
  - **High input impedance**
  - **Less sensitive to temperature**
  - **Low power consumption**

- **FET Amplifiers**
  - **Analysis methods are same for FET amplifiers and BJT amplifiers except their specific characteristics and small-signal model**
    - **DC and AC analysis**
    - **cascaded systems**
  - **CS, CG, CD**