

NATIONAL INSTITUTE OF TECHNOLOGY
SRINAGAR

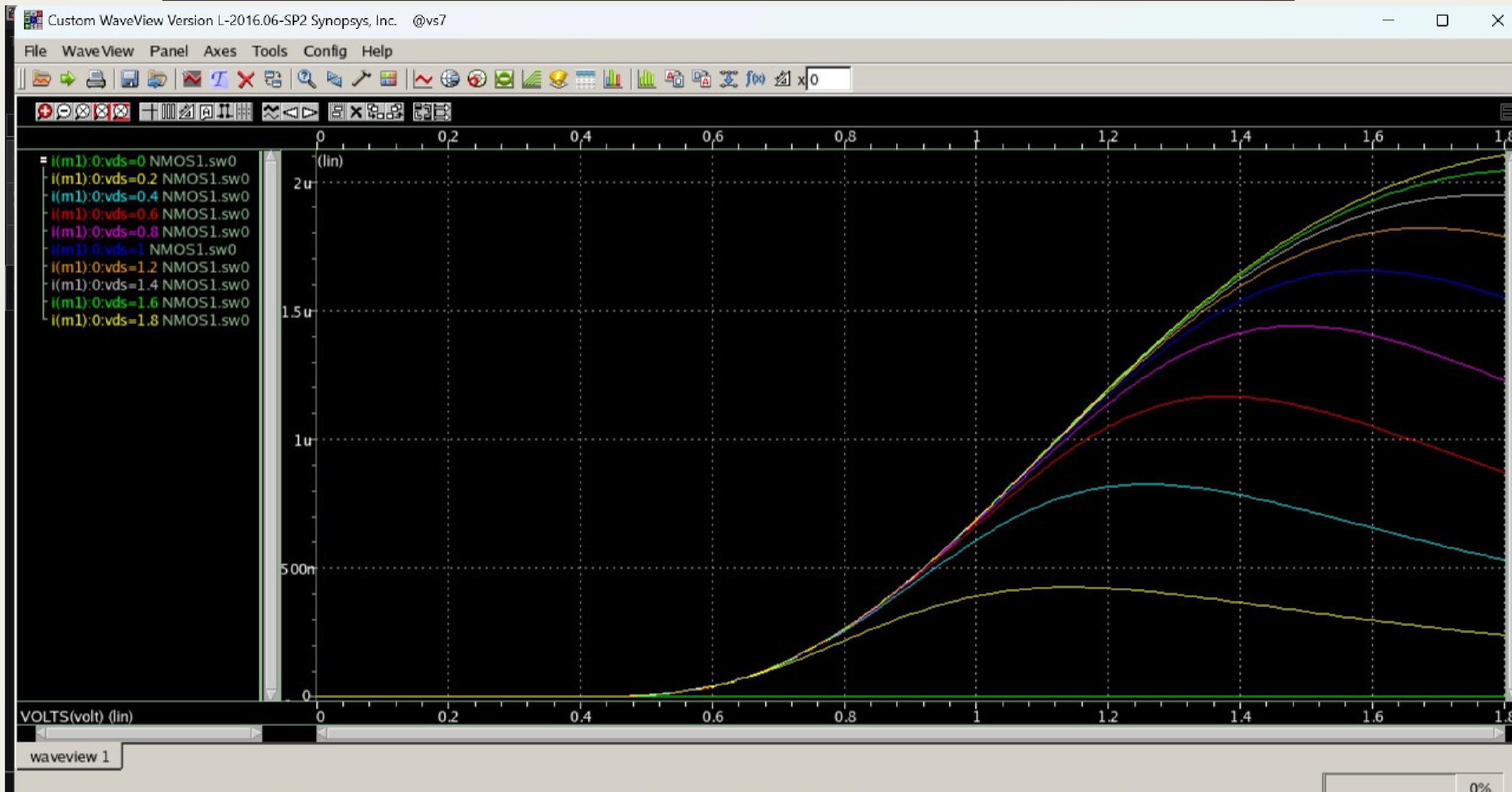
SRAM Design

Presented by Nitendra Kumar

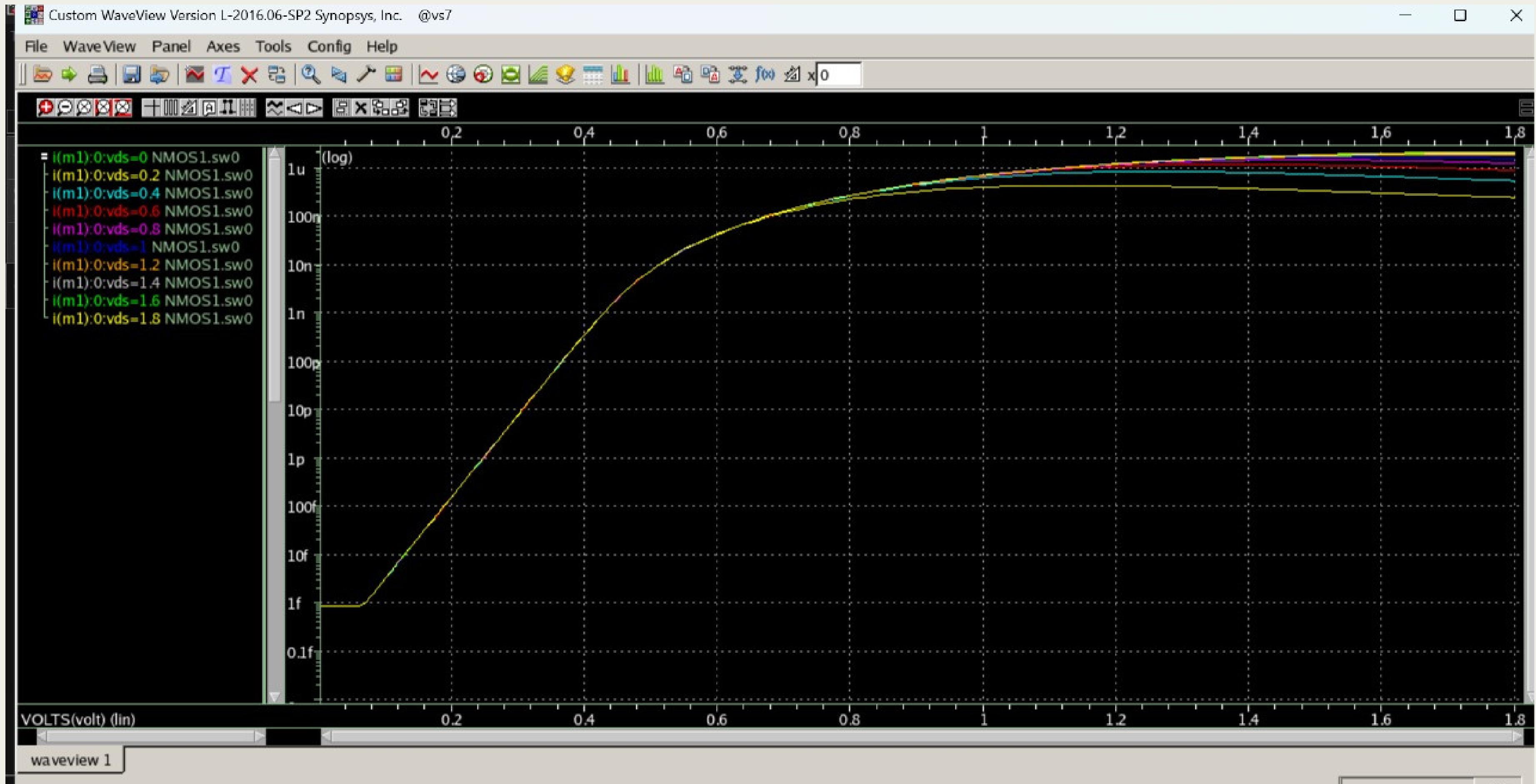
Netlist of Input characteristics of NMOS

```
*input characteristics of nmos*
*****
.model nmos1 nmos LEVEL=72
*Vgnd gnd 0 dc 0*
.option post
*****
Vgs g 0 dc 1.8
Vds d 0 dc 1.8
M1 d g 0 0 nmos1 w=20um l=10um
.dc Vgs 0 1.8 0.01 Vds 0 1.8 0.2
*****
.prob dc i(M1)
.end
```

Ids Vs Vgs at different value of Vds at linear scale



Ids Vs Vgs at different value of Vds at log scale



Netlist of Output characteristics of NMOS

output characteristics of nmos

.model nmos1 nmos LEVEL=72

.option post

Vgs g 0 dc 1.8

Vds d 0 dc 1.8

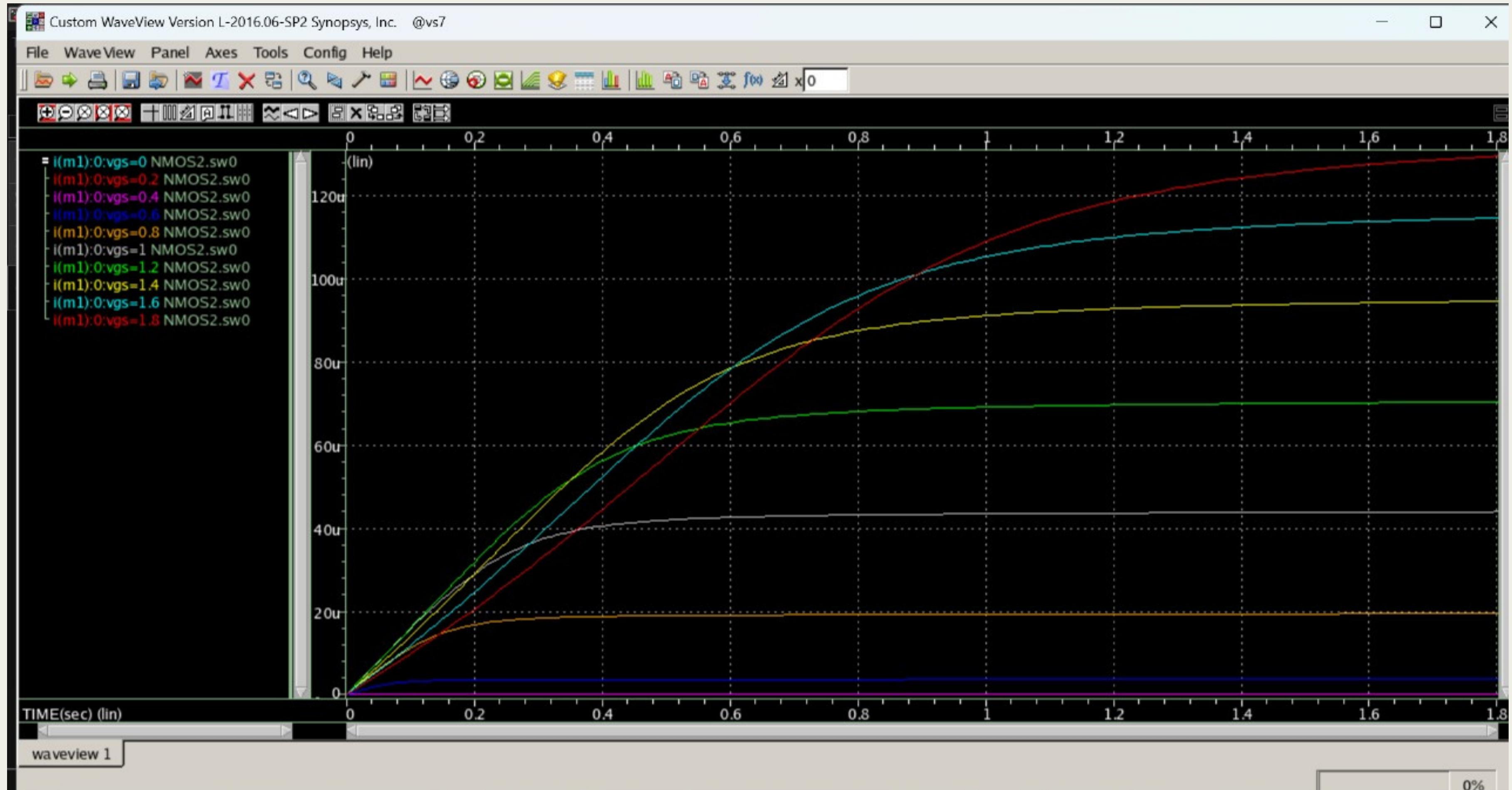
M1 d g 0 0 nmos1 w=200n l=100n

.dc Vds 0 1.8 0.01 Vgs 0 1.8 0.2

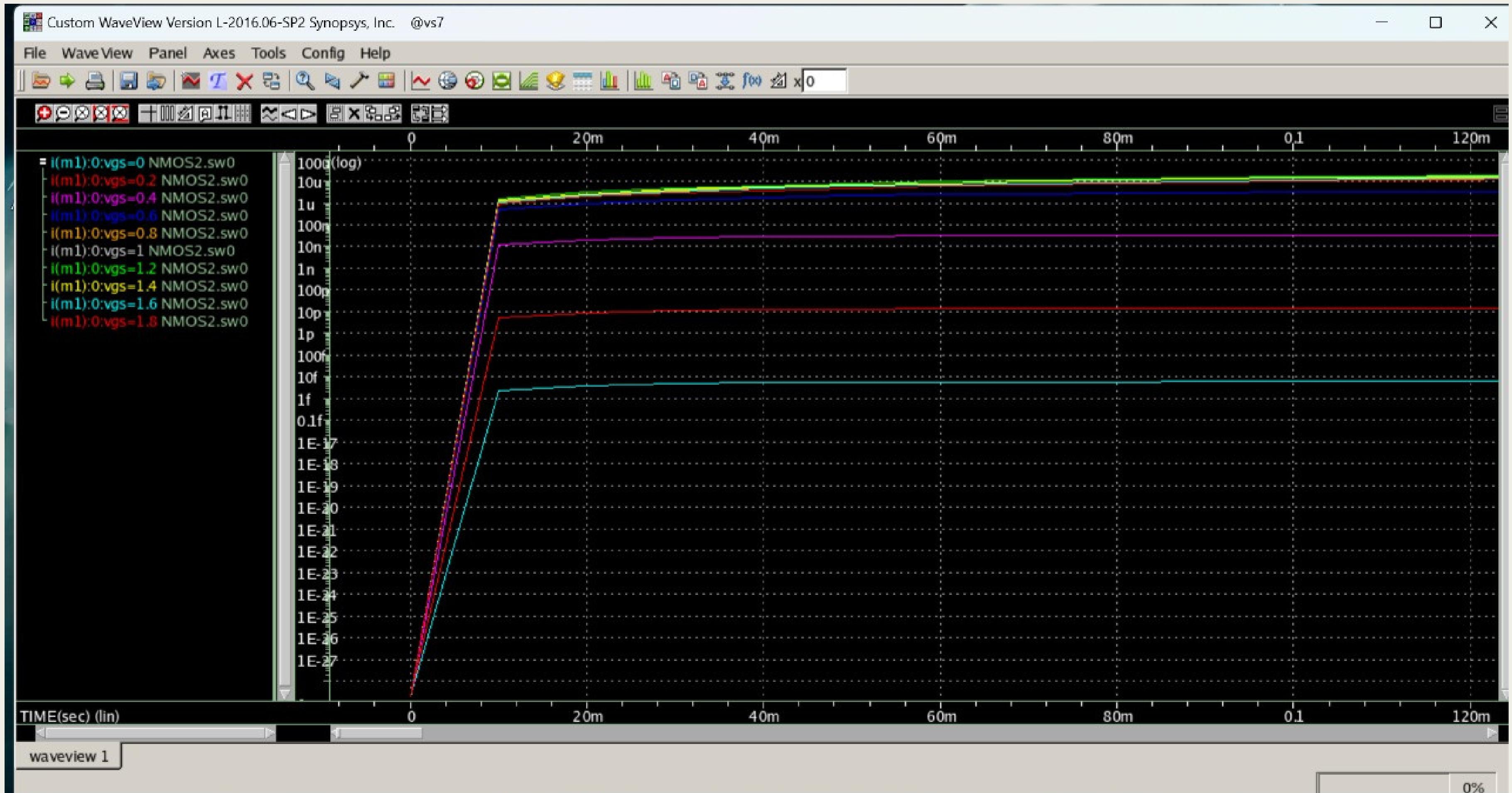
.prob dc i(M1)

.end

Ids Vs Vds at different value of Vgs at linear scale



Ids Vs Vds at different value of Vgs at log scale



Netlist of Input characteristics of PMOS

input characteristics of PMOS

.model pmos1 pmos LEVEL=72

.option post

Vgs g 0 dc -1.8

Vds d 0 dc -1.8

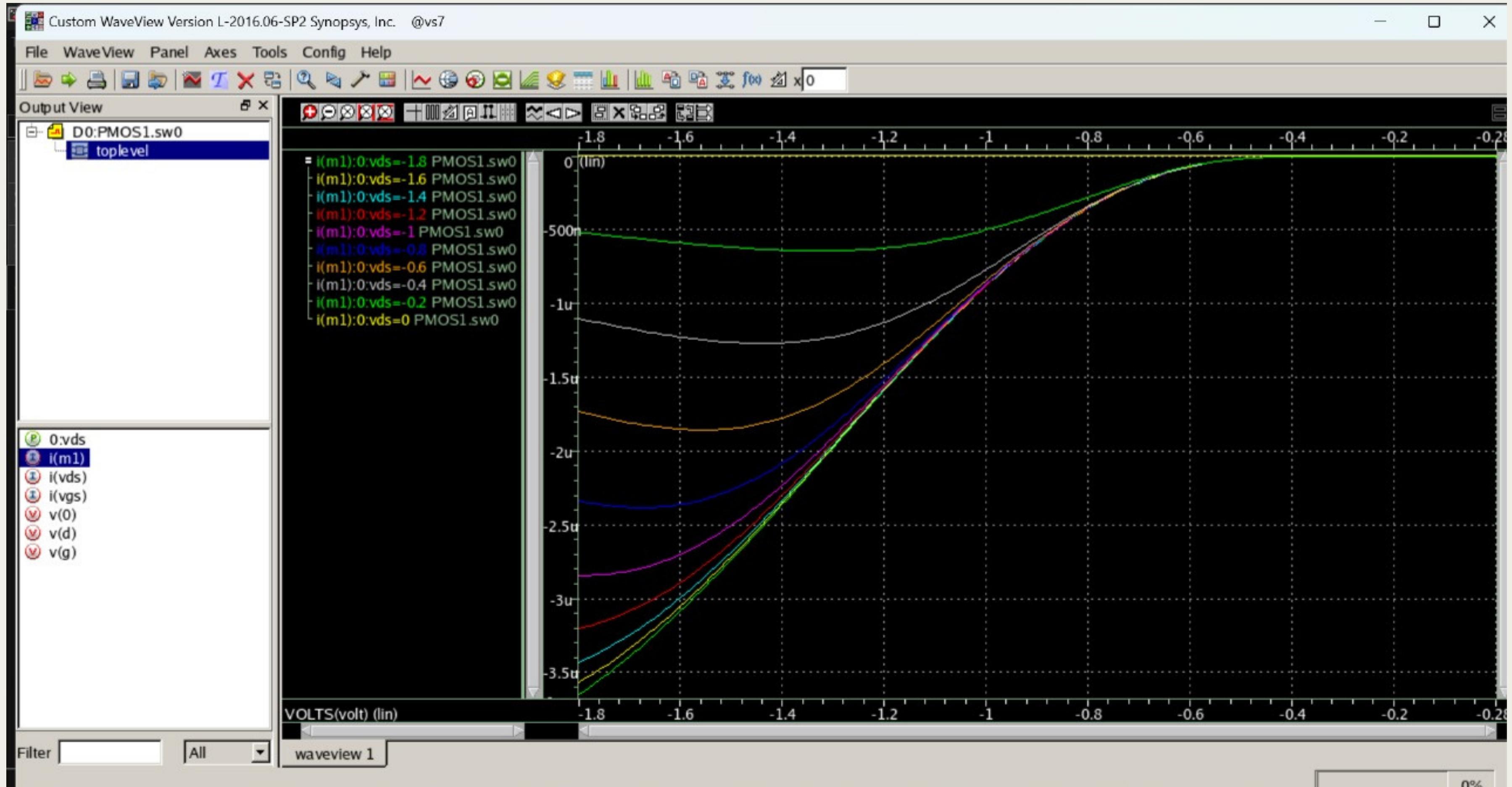
M1 d g 0 0 pmos1 w=20um l=10um

.dc Vgs -1.8 0 0.01 Vds -1.8 0 0.2

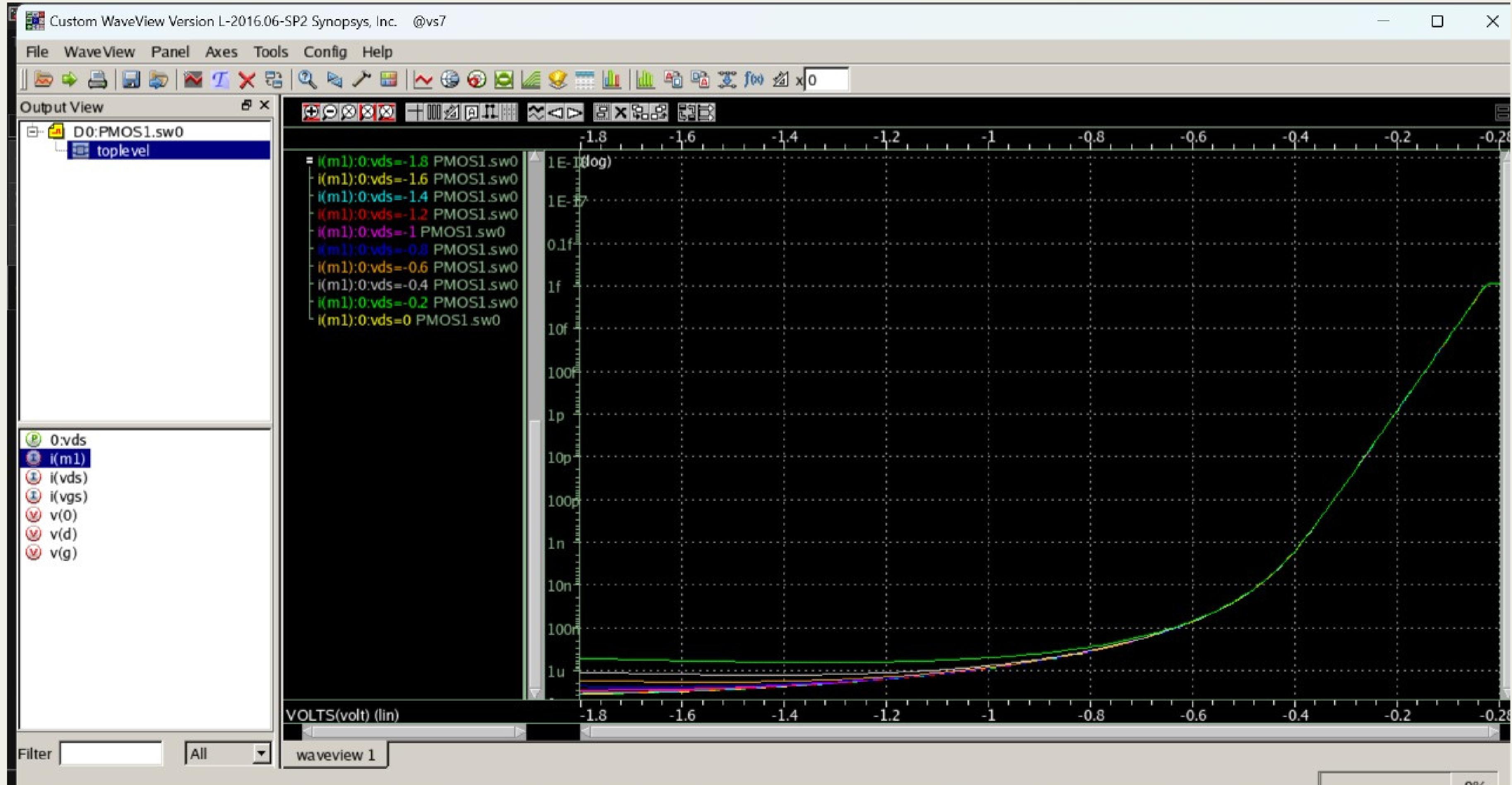
.prob dc i(M1)

.end

Ids Vs Vgs at different value of Vds at linear scale



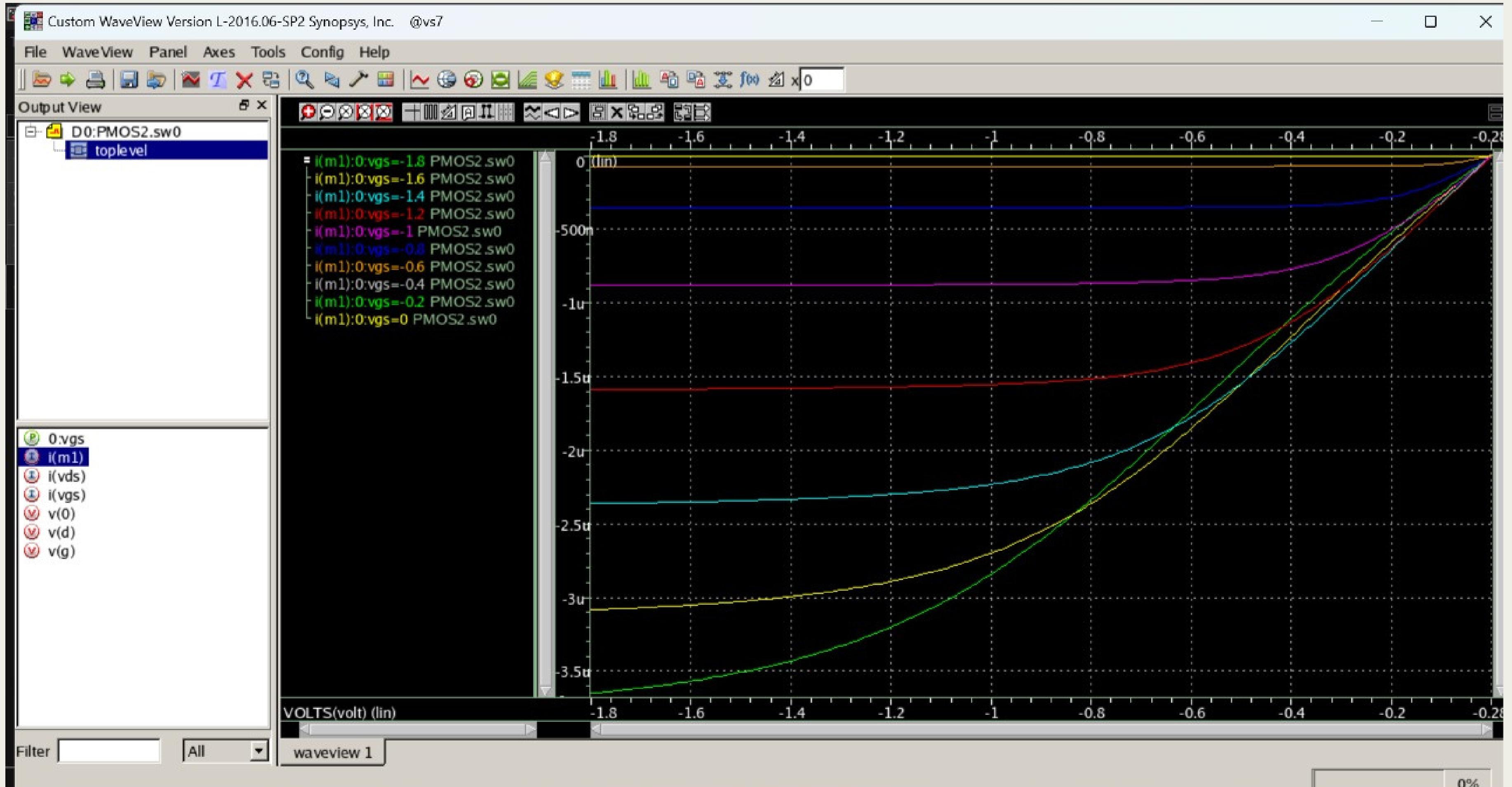
Ids Vs Vgs at different value of Vds at log scale



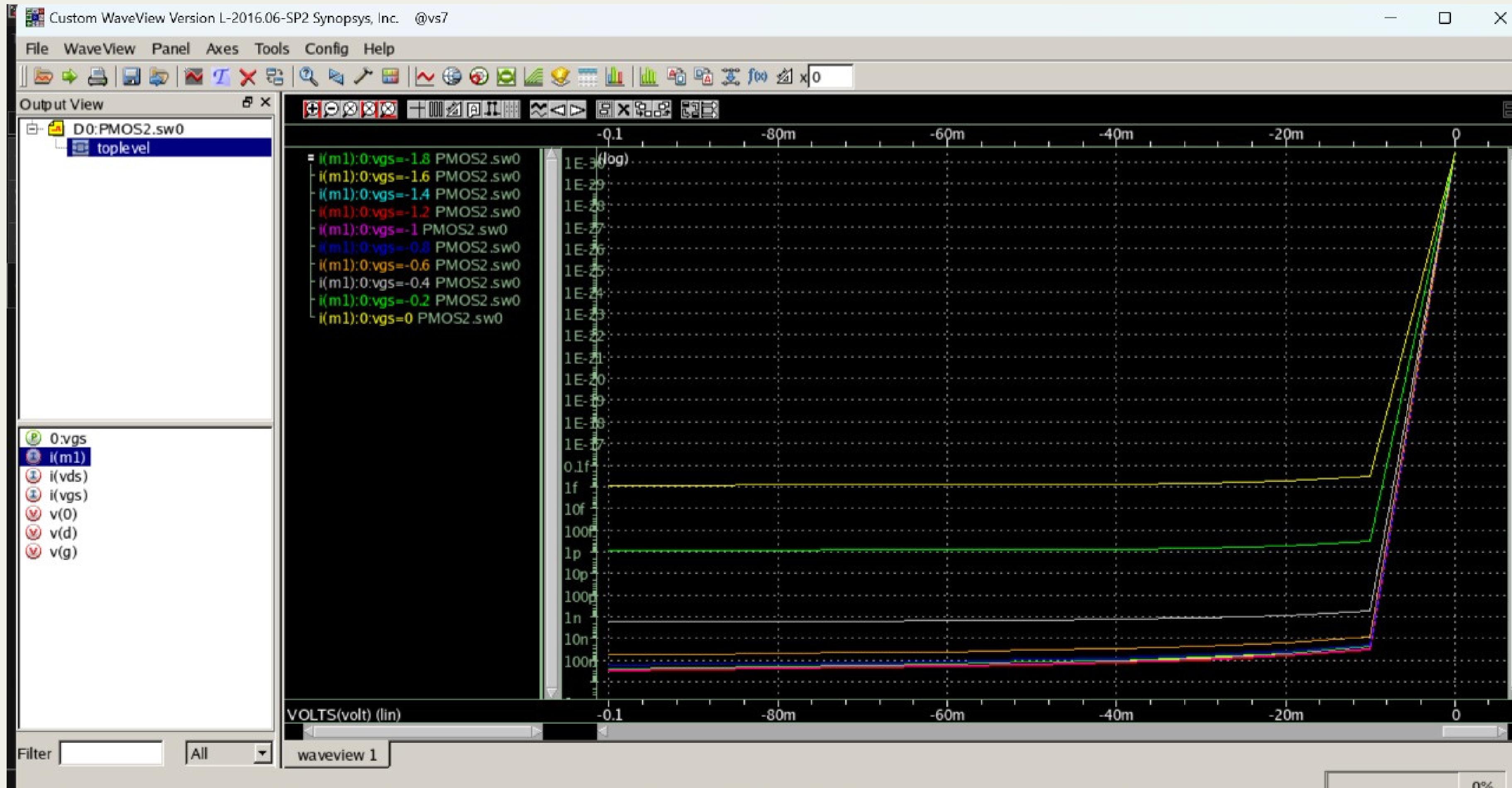
Netlist of Output characteristics of PMOS

```
*output characteristics of PMOS*
*****
.model pmos1 pmos LEVEL=72
.option post
*****
Vgs g 0 dc -1.8
Vds d 0 dc -1.8
M1 d g 0 0 pmos1 w=20um l=10um
.dc Vds -1.8 0 0.01 Vgs -1.8 0 0.2
*****
.prob dc i(M1)
.end
```

Ids Vs Vds at different value of Vgs at linear scale



Ids Vs Vds at different value of Vgs at log scale



Netlist of CMOS Inverter

cmosinverter voltage Transfer characteristics

.model nmos1 nmos LEVEL=72

.model pmos1 pmos LEVEL=72

.option post

MP1 d g a a pmos1 w=360nm l=180nm

MN1 d g 0 0 nmos1 w=180nm l=180nm

Vin g 0 dc 1.8

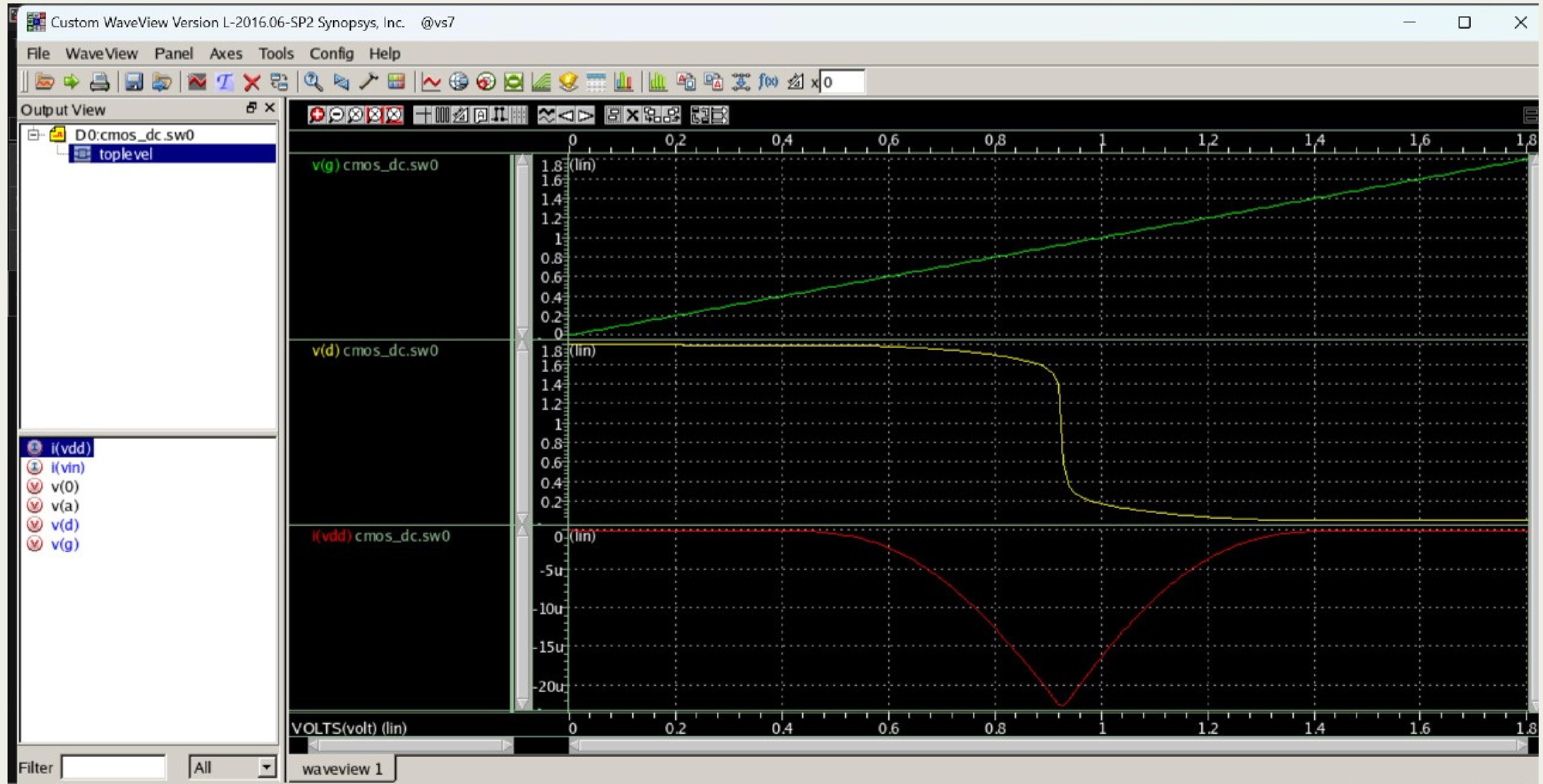
Vdd a 0 dc 1.8

.dc Vin 0 1.8 0.01

.probe dc

.end

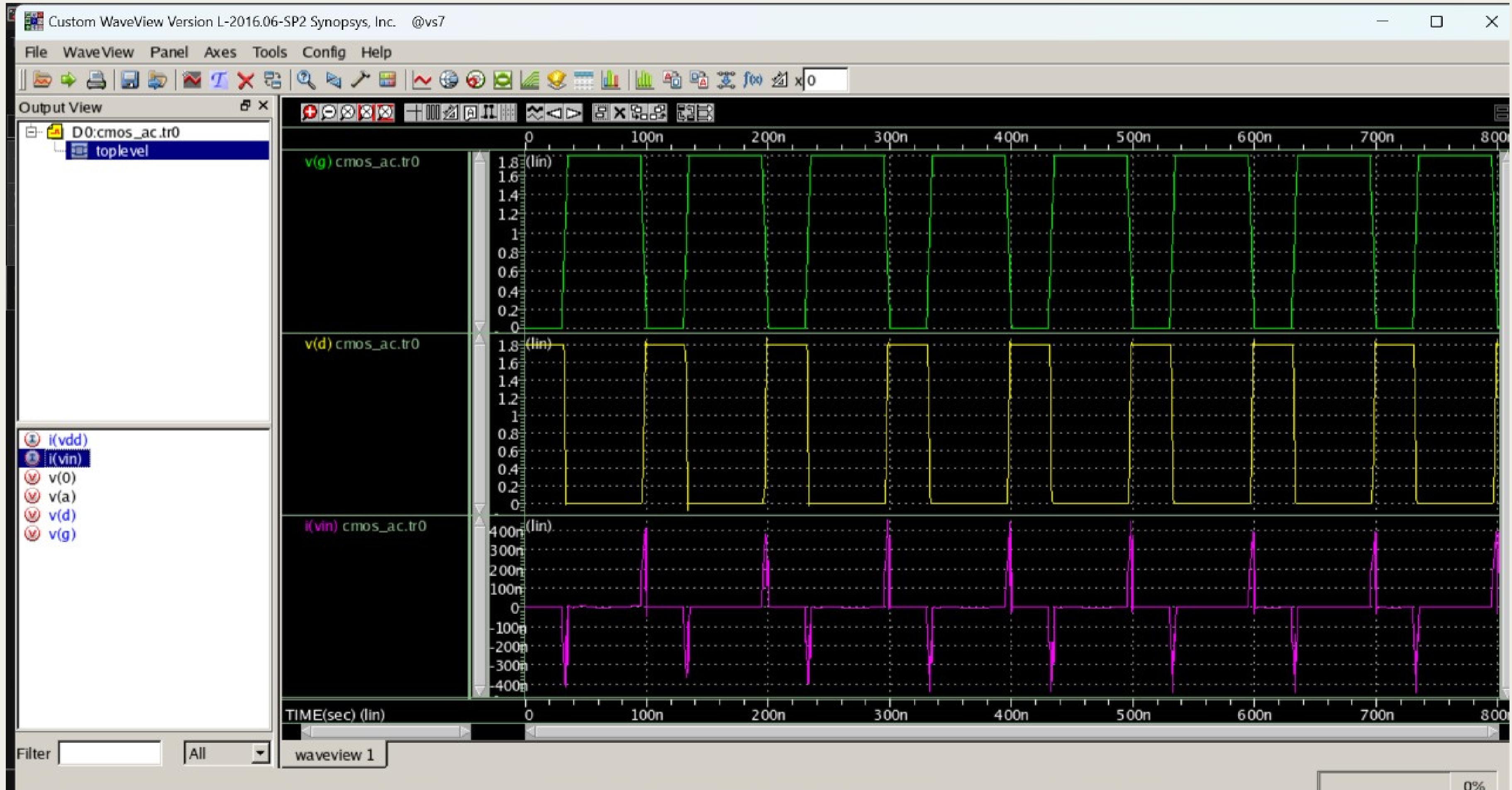
CMOS Inverter Voltage Transfer Characteristics



Netlist of CMOS Inverter(Transient Analysis)

```
*cmosinverter Transient Analysis*
*****
.model nmos1 nmos LEVEL=72
.model pmos1 pmos LEVEL=72
.option post
*****
MP1 d g a a pmos1 w=360nm l=180nm
MN1 d g 0 0 nmos1 w=180nm l=180nm
Vin g 0 pulse(0 1.8 30n 5n 5n 60n 100n)
Vdd a 0 dc 1.8
*****
.tran 1n 800n
.probe tran
.end
```

CMOS Inverter Transient Analysis



Netlist of SRAM Design

```
*****SRAM design*****
```

```
*****
```

```
.model nmos1 nmos LEVEL=49
```

```
.model pmos1 pmos LEVEL=49
```

```
.option post
```

```
*****
```

```
Vwl wl 0 pulse(0 2.5 0 1n 1n 12m 32m)
```

```
Vbl bl 0 pulse(0 2.5 0 1n 1n 8m 16m)
```

```
Vbl_b bl_b 0 pulse(0 2.5 0 1n 1n 4m 8m)
```

```
Vdd a 0 dc 2.5
```

```
M1 Q_b Q a a pmos1 w=360nm l=180nm
```

```
M3 Q Q_b a a pmos1 w=390nm l=180nm
```

```
M2 Q_b Q 0 0 nmos1 w=500nm l=180nm
```

```
M4 Q Q_b 0 0 nmos1 w=180nm l=180nm
```

```
M5 bl_b wl Q_b 0 nmos1 w=420nm l=180nm
```

```
M6 bl wl Q 0 nmos1 w=420nm l=180nm
```

```
C1 bl_b 0 20pF
```

```
C2 bl 0 20pF
```

```
*****
```

```
.tran 1n 180m
```

```
.probe tran
```

```
.end
```

SRAM Read / Write Operations :at Level 49



Netlist of SRAM Design

```
*****SRAM design*****
```

```
*****
```

```
.model nmos1 nmos LEVEL=72
```

```
.model pmos1 pmos LEVEL=72
```

```
.option post
```

```
*****
```

```
Vwl wl 0 pulse(0 1.8 0 1n 1n 12m 32m)
```

```
Vbl bl 0 pulse(0 1.8 0 1n 1n 8m 16m)
```

```
Vbl_b bl_b 0 pulse(0 1.8 0 1n 1n 4m 8m)
```

```
Vdd a 0 dc 1.8
```

```
M1 Q_b Q a a pmos1 w=100um l=100um
```

```
M3 Q Q_b a a pmos1 w=130um l=100um
```

```
M2 Q_b Q 0 0 nmos1 w=200um l=100um
```

```
M4 Q Q_b 0 0 nmos1 w=80um l=130um
```

```
M5 bl_b wl Q_b 0 nmos1 w=150um l=100um
```

```
M6 bl wl Q 0 nmos1 w=150um l=100um
```

```
C1 bl_b 0 20pF
```

```
C2 bl 0 20pF
```

```
*****
```

```
.tran 1n 180m
```

```
.probe tran
```

```
.end
```

SRAM Read / Write Operations :at Level 72



6T SRAM Cell with diff sense amp and precharge circuit

NETLIST of Level 49

*SRAM using Differential based sense Amplifier and
precharge circuitry*

```
.model pmos1 pmos level=49
.model nmos1 nmos level=49
.option post
*****
Vwl wl 0 pulse(0 3.3 1m 1p 1p 2m 5m)
Vwrt wc 0 pulse(0 3 1.5m 1p 1p 10m 20m)
Vdata data 0 pulse(0 3 0 1p 1p 10m 20m)
Vpc pc 0 pulse(3 0 3m 1p 1p 1m 10m)
Vse se 0 pulse(0 3 6m 1p 1p 2m 10m)
*Vse_b se_b 0 pulse(3 0 6m 1p 1p 2m 10m)
```

```
Vdd a 0 dc 3
```

```
M1 Q_b Q_a a pmos1 w=1u l=0.18u
M3 Q_b a a pmos1 w=1u l=0.18u
M2 Q_b Q_0 0 nmos1 w=1u l=0.18u
M4 Q_b 0 0 nmos1 w=1u l=0.18u
M5 bl_b wl_Q_b 0 nmos1 w=1u l=0.18u
M6 bl wl_Q_0 nmos1 w=1u l=0.18u
```

Write clock

```
M7 1 data a a pmos1 w=1u l=0.18u
M9 2 1 a a pmos1 w=1u l=0.18u
M8 1 data 0 0 nmos1 w=1u l=0.18u
M10 2 1 0 0 nmos1 w=1u l=0.18u
M11 1 wc bl_b 0 nmos1 w=1u l=0.18u
M12 2 wc bl_0 nmos1 w=1u l=0.18u
```

* Precharge

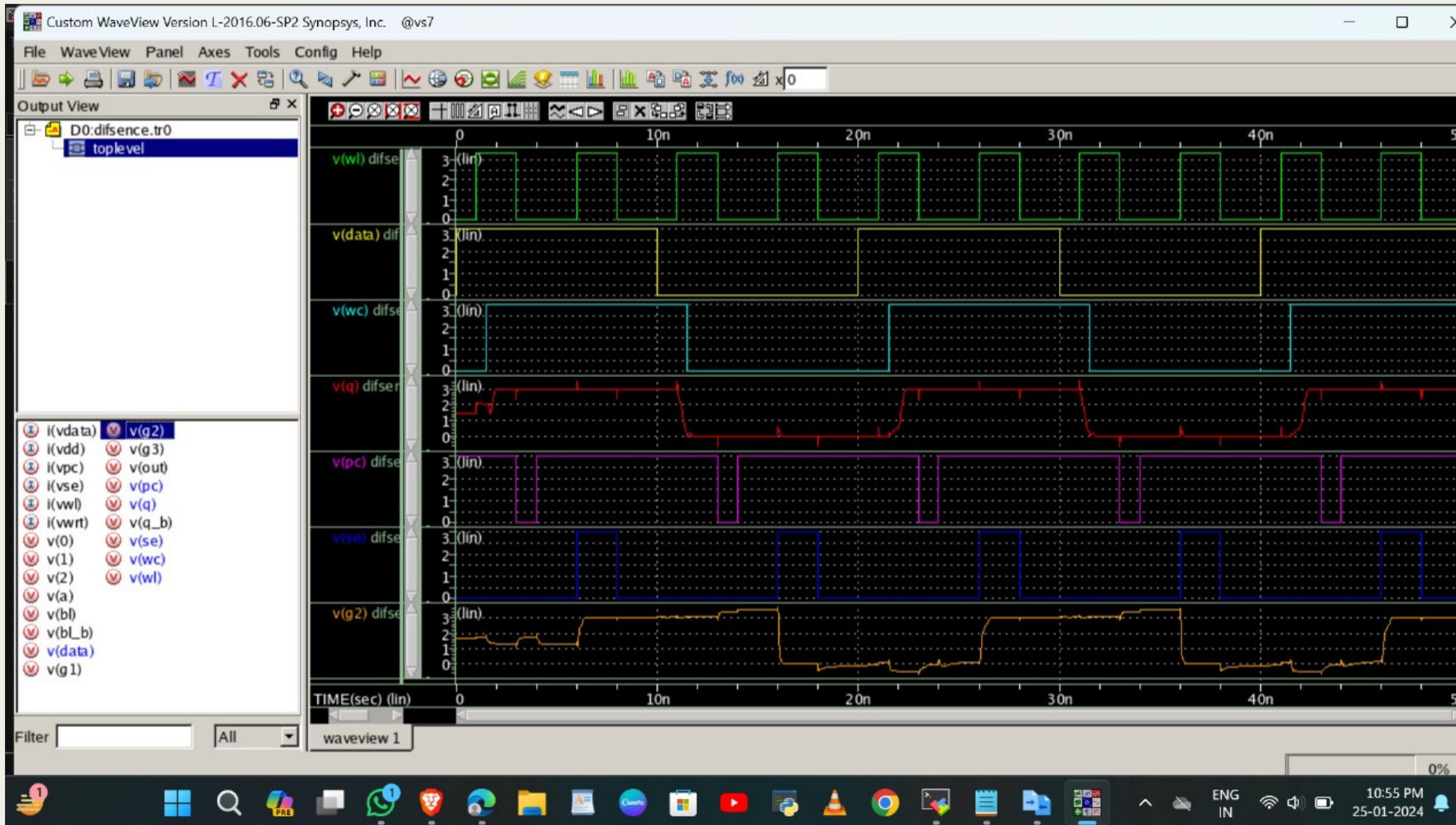
```
M13 bl_b pc a a pmos1 w=1u l=0.18u
M14 bl_pc a a pmos1 w=1u l=0.18u
M15 bl_pc bl_b a pmos1 w=1u l=0.18u
```

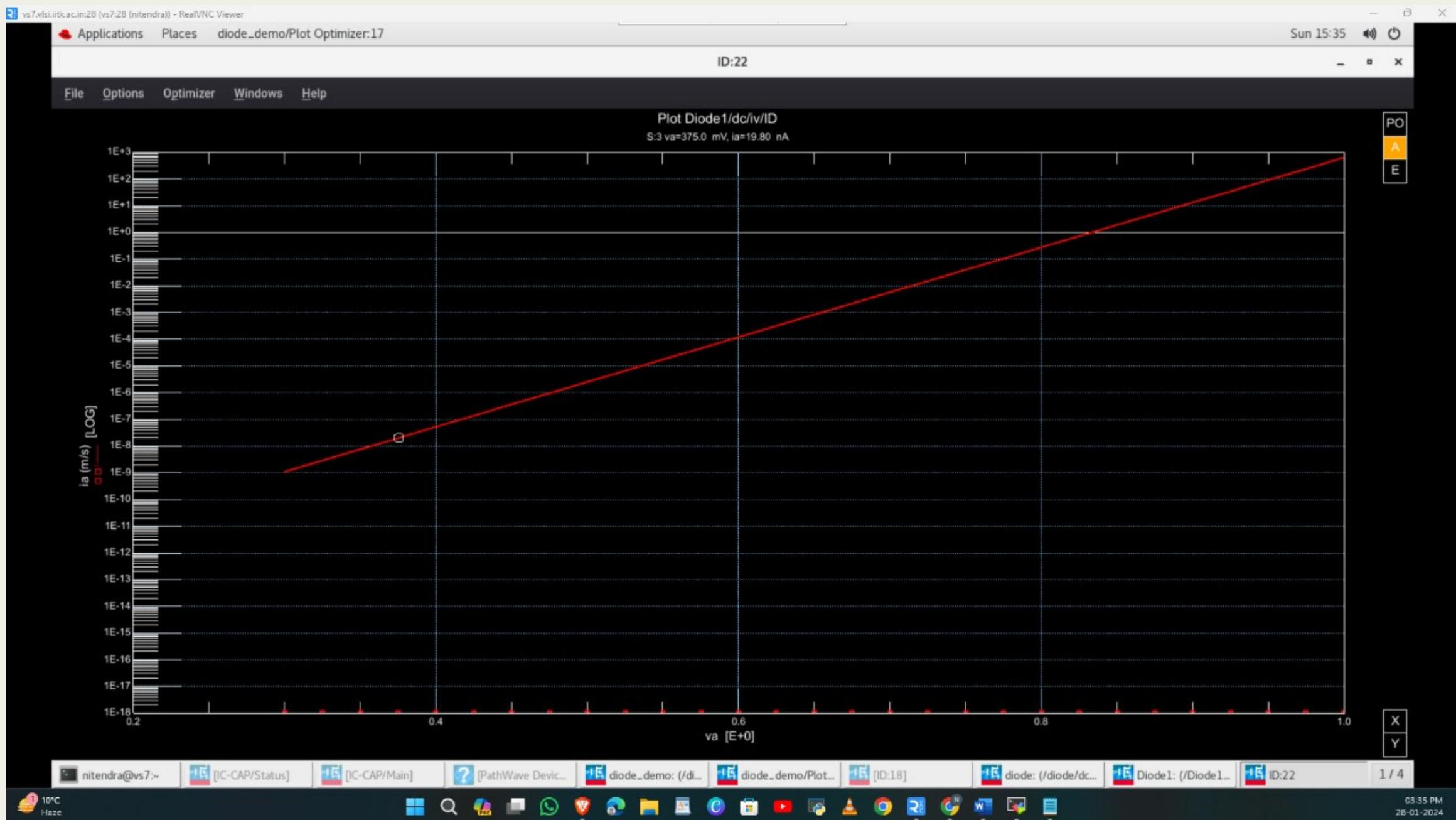
*sense amplifier

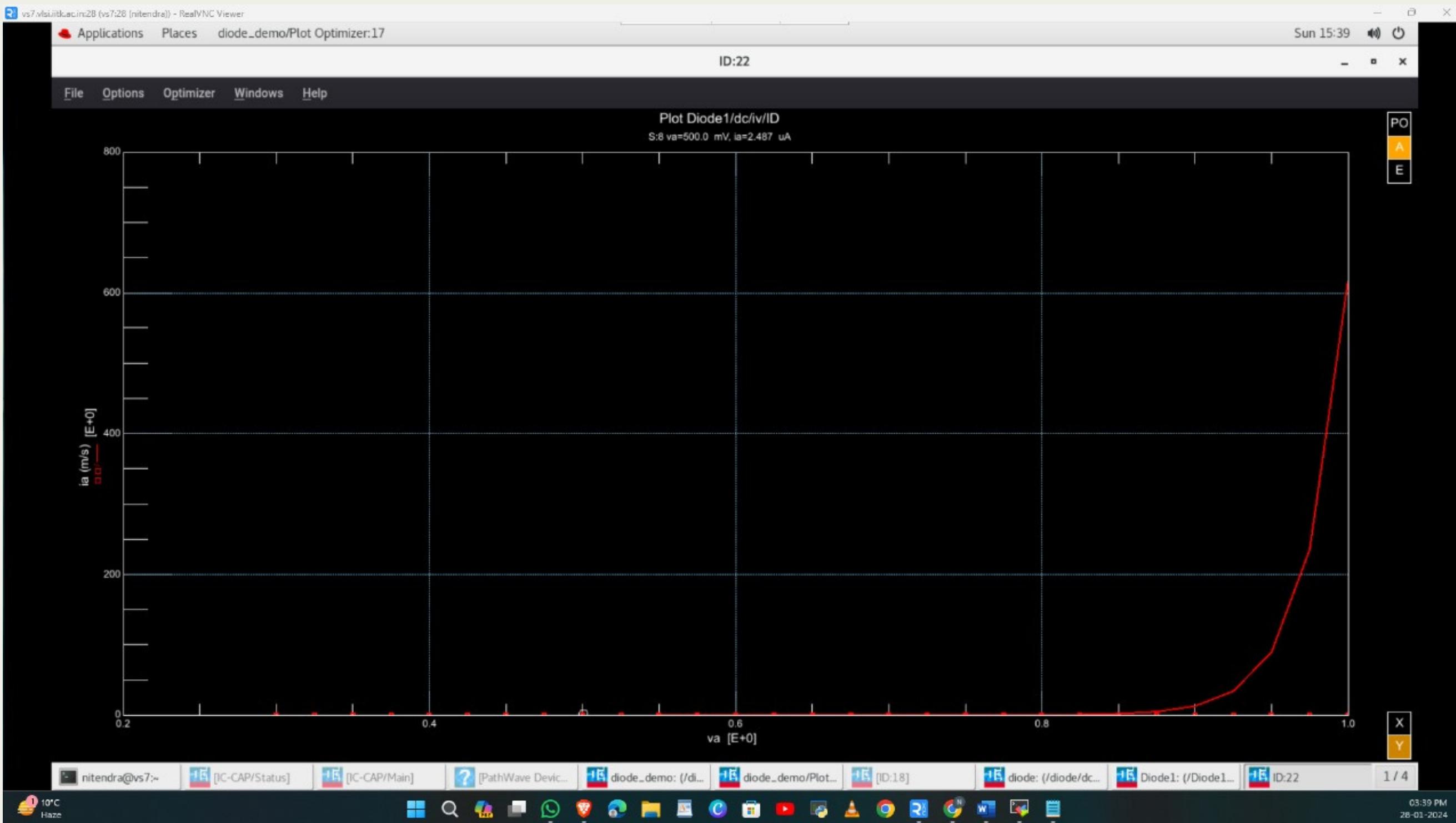
```
M16 g1 g1 a a pmos1 w=1u l=0.18u
M17 g2 g1 a a pmos1 w=1u l=0.18u
M18 g1 bl_b g3 0 nmos1 w=1u l=0.18u
M19 g2 bl_g3 0 nmos1 w=1u l=0.18u
M20 g3 se 0 0 nmos1 w=1u l=0.18u
M21 out g2 a a pmos1 w=1u l=0.18u
M22 out g2 0 0 nmos1 w=1u l=0.18u
```

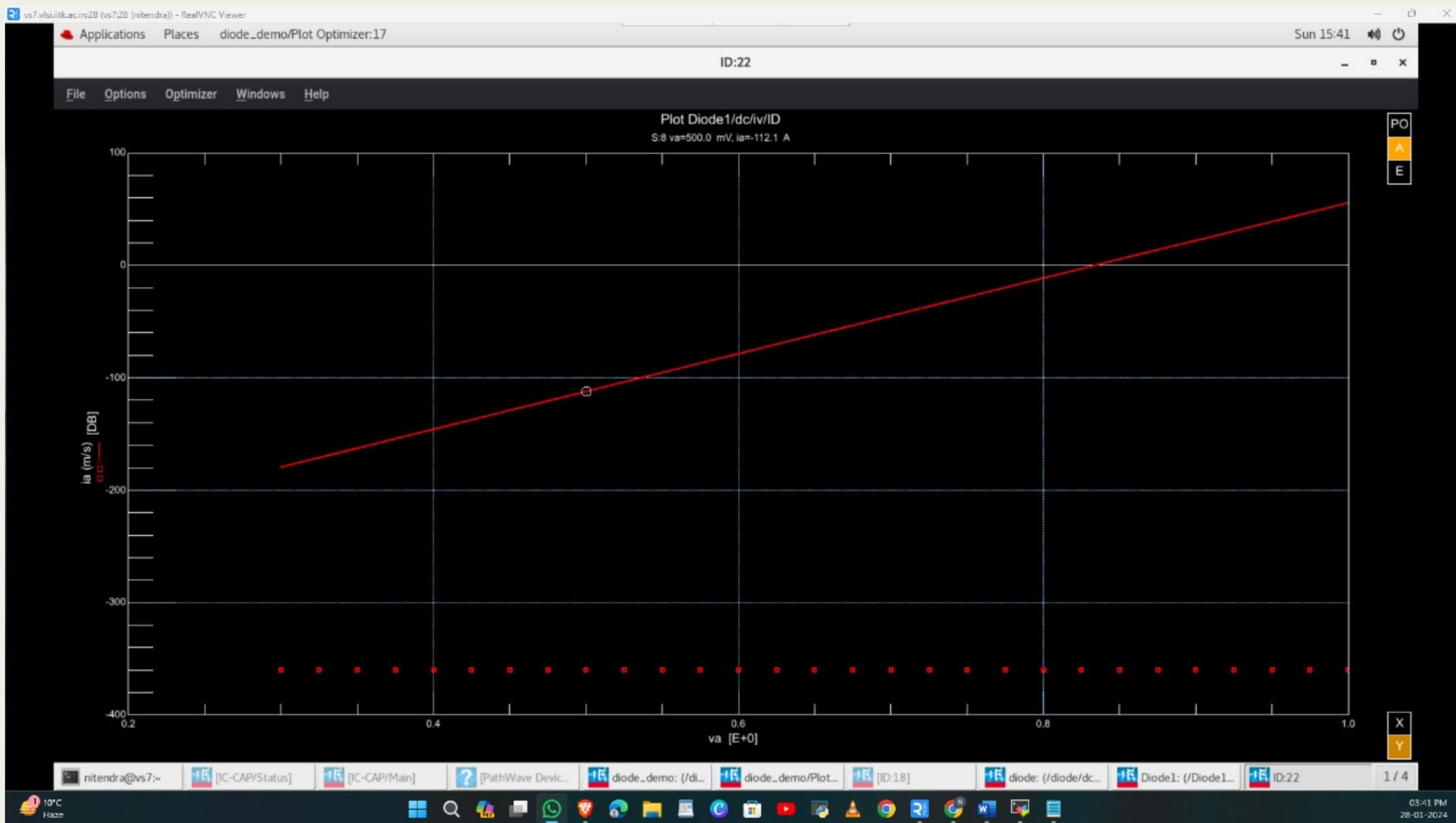
```
C1 bl_b 0 80p
C2 bl_0 80p
.tran ln 50m
.probe tran
.end
```

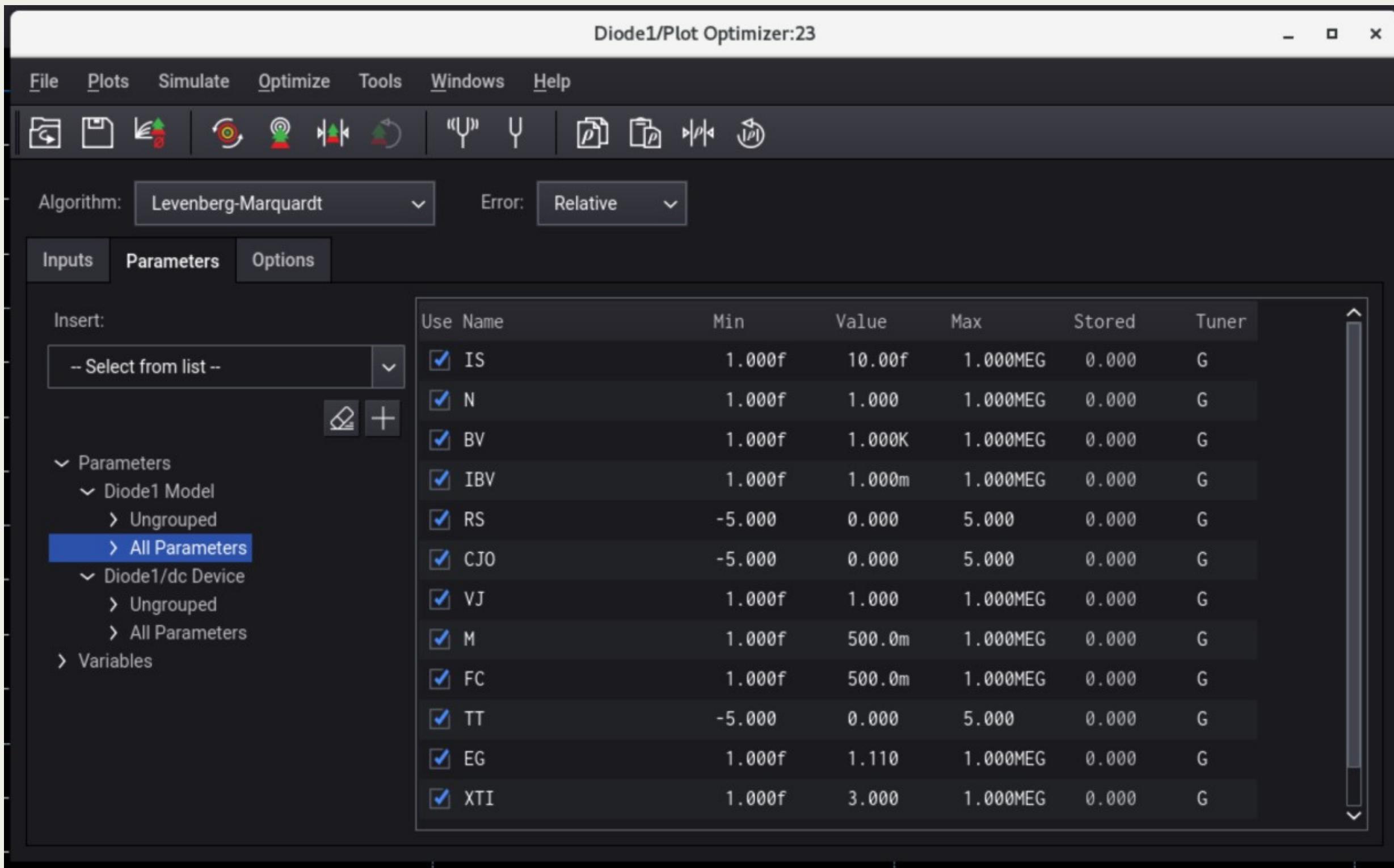
6T SRAM Cell with Differential Sense Amplifier

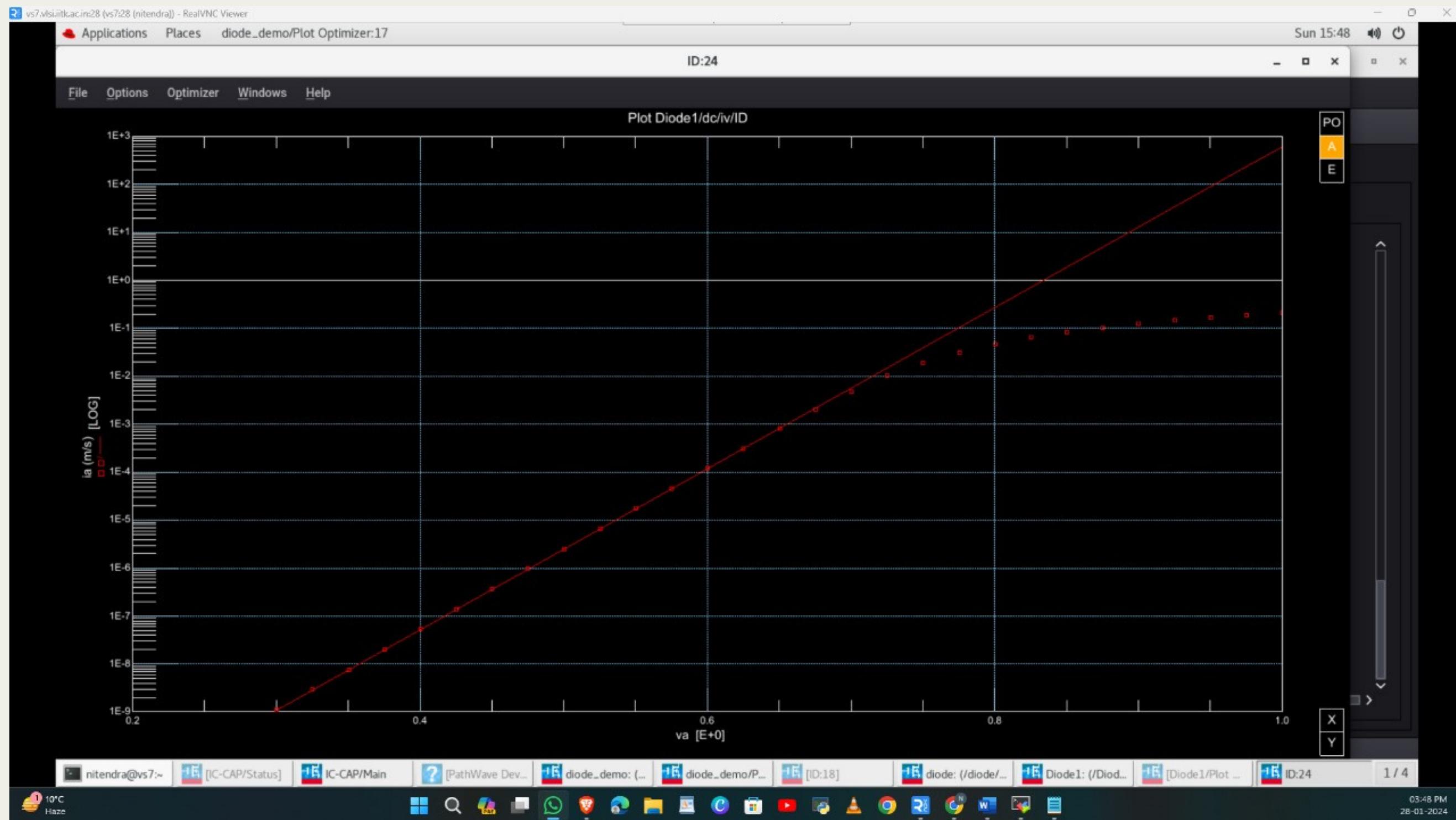


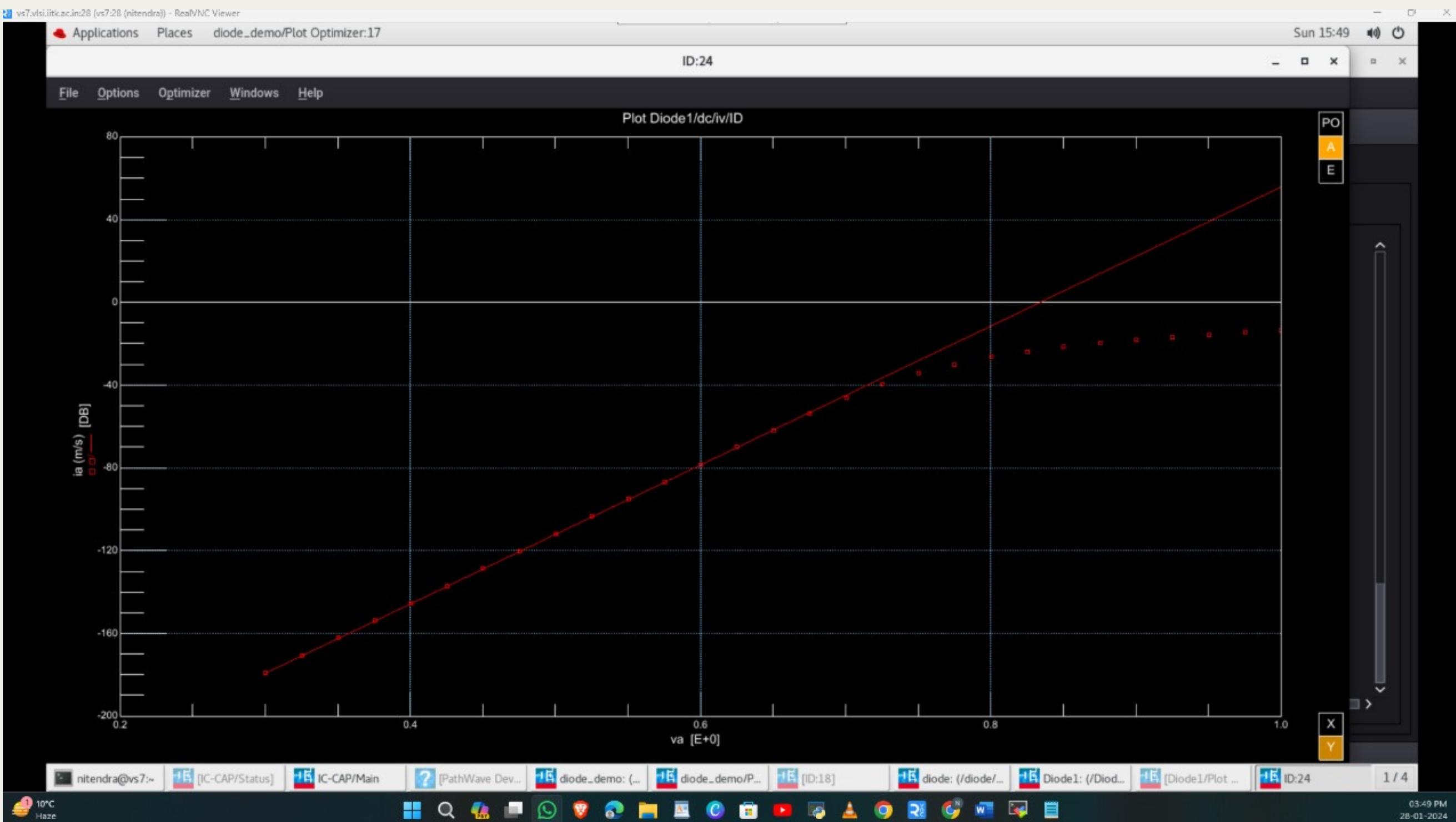


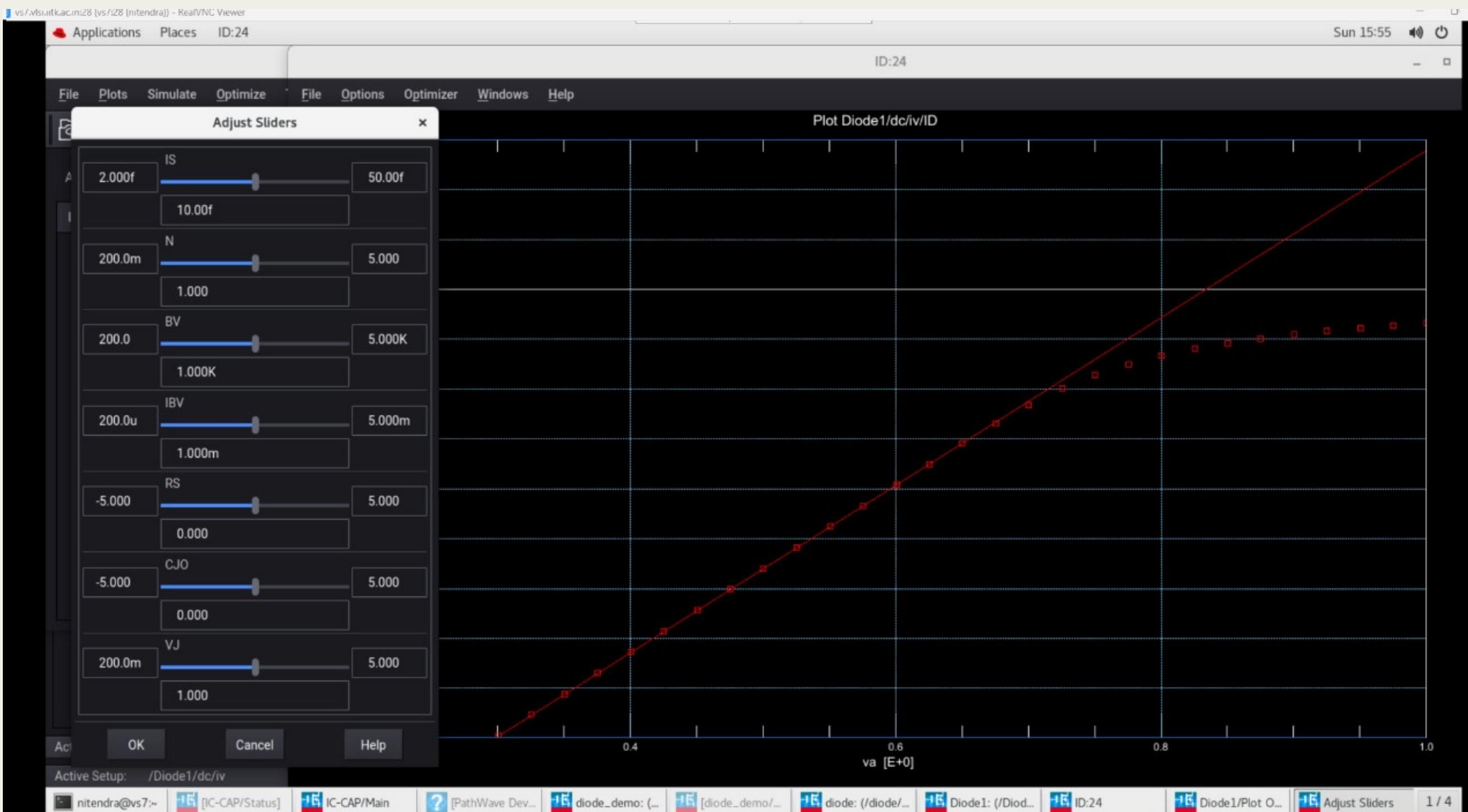


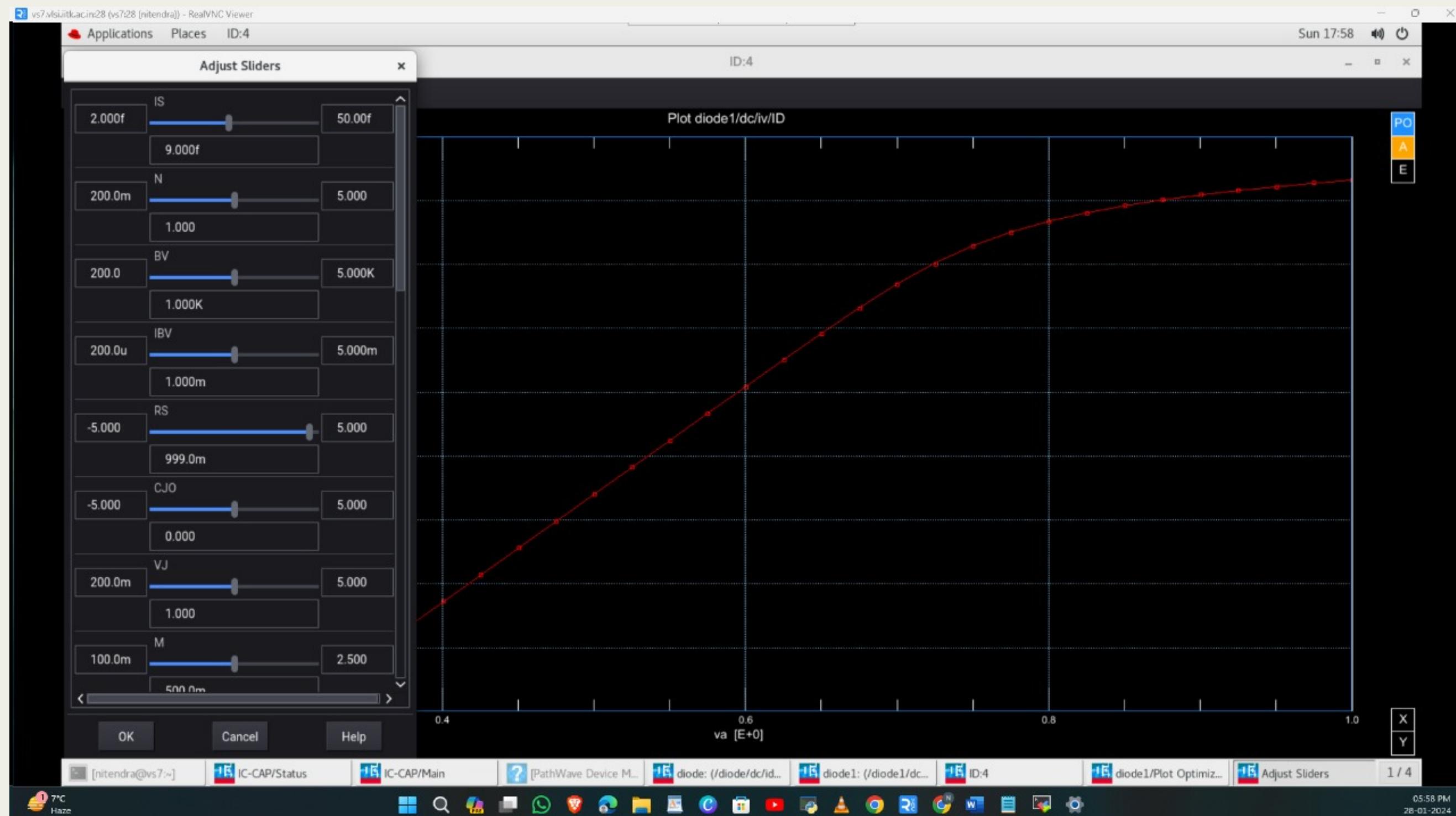


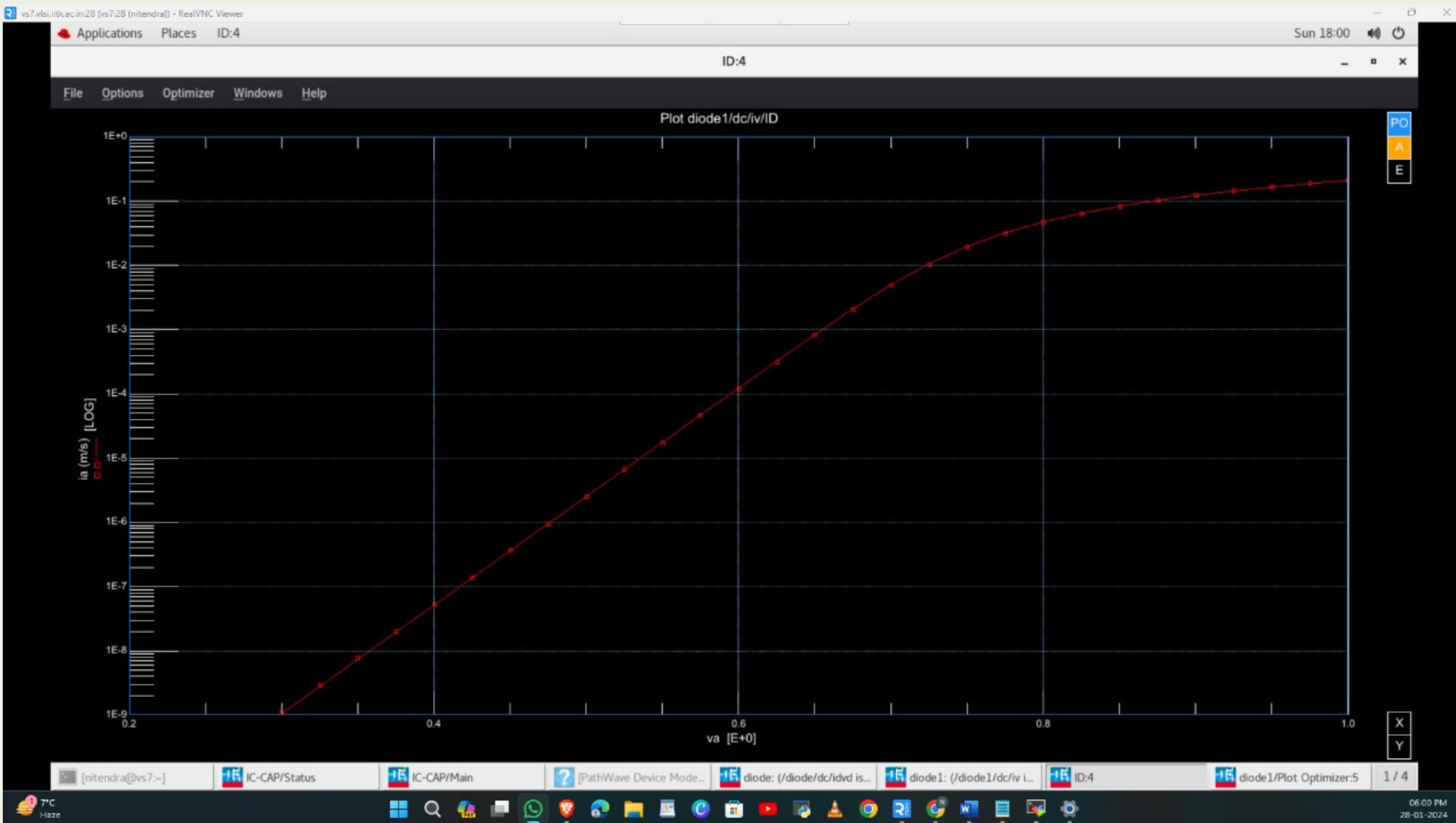


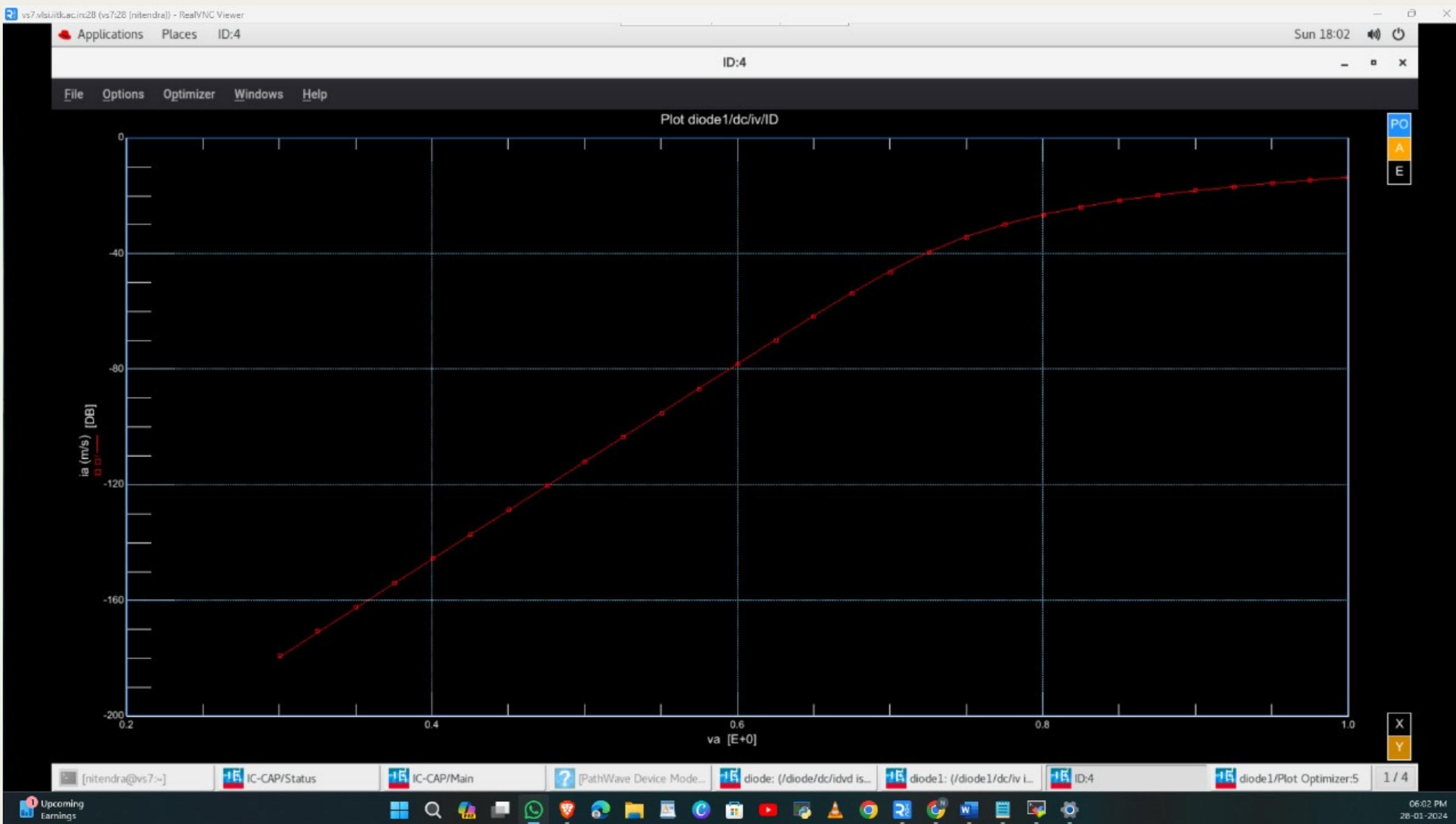


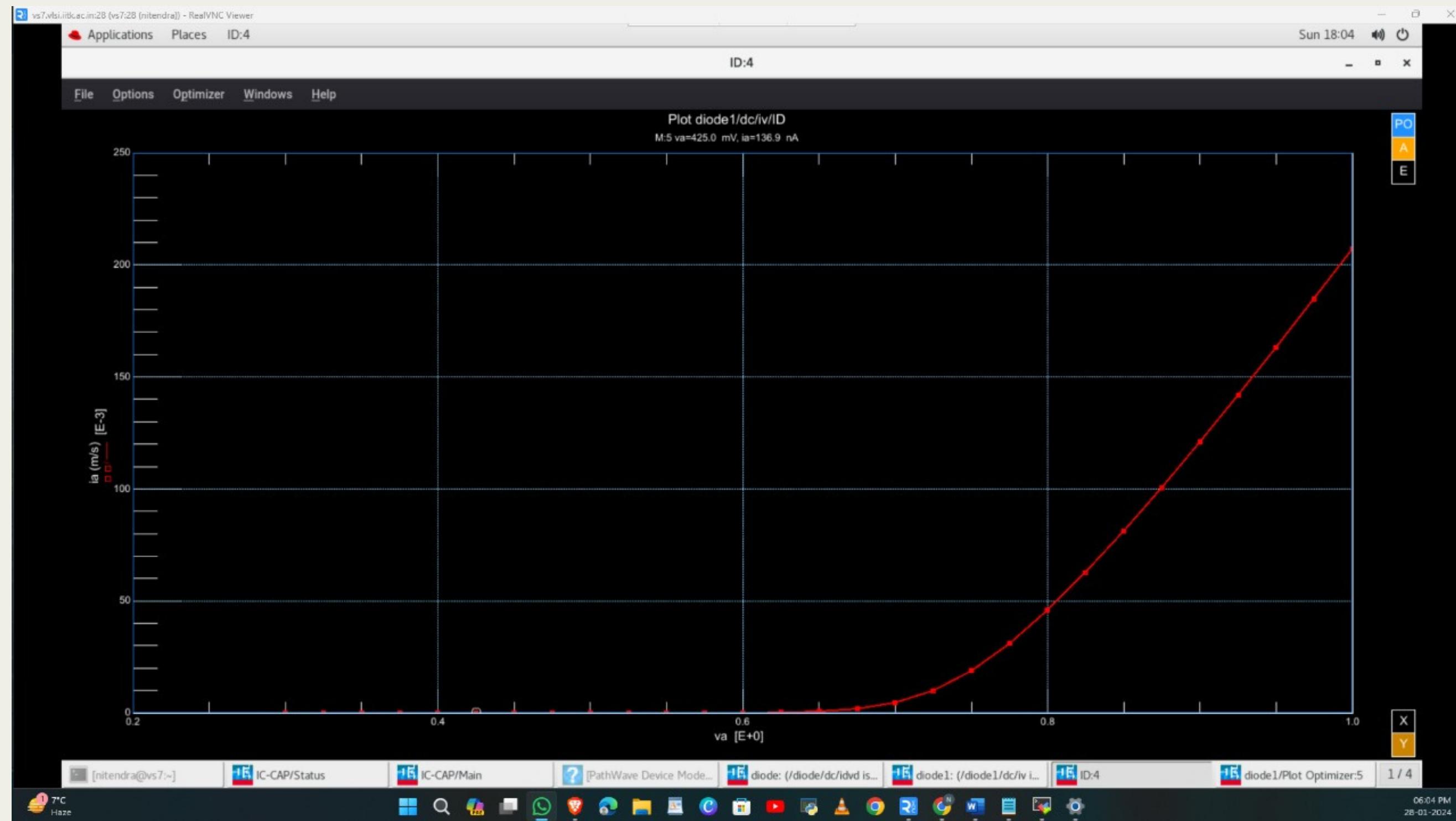












8T_ SRAM netlist

```
* 8T SRAM design
.model pmos1 pmos level=49
.model nmos1 nmos level=49
.option post
*****
M1 Q_b Q a a pmos1 w=1u l=0.18u
M3 Q_b a a pmos1 w=1u l=0.18u
M2 Q_b Q_0 0 nmos1 w=1u l=0.18u
M4 Q_b 0 0 nmos1 w=1u l=0.18u
M5 wbl wwl Q_b 0 nmos1 w=1u
l=0.18u
M6 wbl_b wwl Q 0 nmos1 w=1u
l=0.18u
M7 rbl rw1 1 0 nmos1 w=1u l=0.18u
M8 1 Q_0 0 nmos1 w=1u l=0.18u
C1 wbl 0 100p
C2 wbl_b 0 100p
C3 rbl 0 k
.param k=0
Vwwl wwl 0 pulse(0 3 1n 1p 1p 40n
64n)
Vrw1 rw1 0 pulse(0 3 0 1p 1p 16n 32n)
Vwbl wbl 0 pulse(0 3 0 1p 1p 2n 4n)
Vwbl_b wbl_b 0 pulse(0 3 0 1p 1p 4n
8n)
Vrbl rbl 0 pulse(0 3 6n 1p 1p 1n 6n)
Vdd a 0 dc 3.3
.tran 1n 128n sweep k 1p 100p 10p
.probe tran
.end
```











