2312ET054

Roll No. | | | | | | | | | | | 4 | 3 |

Course: B.Tech Computer Science and Engineering (AI/ML)
Subject: Computer Organization and Architecture,
Subject Code: ETCS-203
Semester: III

Time: 03 Hours **Max Marks: 70**

Instructions to the Students:

1. This Question paper consists of two Sections. All sections are compulsory.
2. Section A comprises 10 questions of short answer type. All questions are compulsory. Each question carries 2 marks.
3. Section B comprises 8 long answer type questions out of which students must attempt any 5. Each question carries 10 marks.
4. Do not write anything on the question paper.

Q. No.		SECTION –A (SHORT ANSWER TYPE QUESTIONS)	Marks
1.	a.	Define the Floating-point representation with its normalisation.	(2)
	b.	What is Control word and Microinstruction?	(2)
	c.	Discuss the Locality of reference principle of cache.	(2)
	d.	What do you mean by Direct Memory access?	(2)
	e.	Explain the following: Relative addressing, Index Addressing Mode	(2)
	f.	What is instruction set completeness?	(2)
	g.	What is Direct and Indirect addressing? Explain with examples.	(2)
	h.	Describe the two type of cache writing Policy.	(2)
	i.	Describe the various types of ROM and what technology is used for modifying the content of ROM.	(2)
	j.	Derive the formula for Instruction pipeline speedup.	(2)

SECTION –B (LONG ANSWER TYPE QUESTIONS)

2.		Describe the Common bus system with registers of Computer. Also, discuss the flowchart for the decoding of the Machine instruction.	(10)

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Mar 25, 2024, 13:46

3. Describe the difference between RISC and CISC Processor in detail. (10)

4. Describe the various Pipeline conflicts. Also, Explain the solution for the pipeline conflicts. (10)

5. a) What do you mean by Memory reference, Register Reference and I/O reference Instruction? (10)

   b) Describe the Associative memory match logic in detail.

6. What is Control memory? Difference between Hardwired and Microprogrammed Control memory. (10)

7. Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate the following: (10)

   a) Pipeline cycle time

   b) Non-pipeline execution time

   c) Speed up ratio

   d) Pipeline time for 1000 tasks

   e) Sequential time for 1000 tasks

8. What is Asynchronous data transfer? Also explain the Strobe control and handshaking method of data transfer? (10)

9. What do you mean by Set Associative Mapping? Explain with the example how the mapping of page in set associative cache is performed? How it is better than Direct Mapping cache? (10)

===END OF PAPER===