Input:

Ins.txt - instruction file
2 - no. of instructions that can be added to RS every cycle
2 - Add/Sub latency
3 - Mul latency
5 - Div latency
1 - Load/Store latency (Addr calculation)
3 - Entries in Add/Sub
2 - Entries in Mul
2 - Entries in Div
3 - Entries in Load/Store
128 - ROB entries
6 - Cache access latency

Output:

28

Ins.txt:

0101 0010 1011 0000 (LD R2, R11, 0000)
0101 0011 1011 0100 (LD R3, R11, 0100)
0001 0001 0010 0011 (ADD R1, R2, R3)
0010 0100 0010 0011 (SUB R4, R2, R3)
0011 0101 0001 0100 (MUL R5, R1, R4)
0100 0110 0111 1000 (DIV R6, R7, R8)
0110 0101 1011 0000 (ST R5, R11, 0000)

Note: Contents in brackets are only given for ease of understanding, they won't be given in the Ins.txt while testing your code.

Explanation:

Instruction	Issue time	Completion time
LD R2, R11, 0000	0	7 (1+6)
LD R3, R11, 0100	0	14 (1+6)
ADD R1, R2, R3	1	16 (2)
SUB R4, R2, R3	1	18 (2)
MUL R5, R1, R4	2	21 (3)
DIV R6, R7, R8	2	7 (5)
ST R5, R11, 0000	3	28 (1+6)