CS6600 Computer Architecture (Jul-Nov 2021)
Assignment-5

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Dynamic execution core

Steps followed

- We first get all the superscalar core parameters from the configuration file '*config.txt'.*
- We then enter a loop to simulate each clock cycle in the core.
- In one iteration of the loop:
  - We read instructions from the input file *'Ins.txt'* and update the dispatch buffer and the reorder buffer.
    - *'finished'* bit in ROB is initialized with *'0'*
  - We then perform register renaming by updating the busy bits of RRF, ARF and the tag of the corresponding architectural register in the ARF.
  - After this, instructions are transferred from the dispatch buffer to the reservation station of the respective functional units.
  - Instructions are then issued for execution in the functional units.
  - Once the instruction execution is finished, the corresponding RRF register is updated and the *'finished'* bit of the corresponding instruction in ROB is set to *'1'.*
  - We then write back the values to the architectural registers in ARF to complete the execution of an instruction.
  - Once written back to the ARF, the corresponding instruction is removed from the Re-Order Buffer.
- Total number of CPU clock cycles elapsed to execute all the instruction *'Ins.txt'* file is then printed on the screen.

Output

- For the above input instruction file '*Inst.txt'* the output is as follows:
  Total clock cycles elapsed: 22

Submission

Please find the relevant files for our Dynamic execution core here.