Nithin Duvvuru

408-476-0544 | nithin.duvvuru@gmail.com | linkedin.com/in/nithinduvvuru | github.com/nithinduvvuru/ | US Citizen

Education

University of California, Santa Cruz Jun. 2026

Bachelor of Science in Computer Engineering, Minor in Computer Science. *Santa Cruz, CA*

Relevant Coursework: Introduction to VLSI Digital System Design, Introduction to ASIC Systems Design, Introduction to Electronic Circuits, Logic Design, Computer Architecture.

Experience

Digital Design Engineer Jul. 2025 – Present

WaveWorks Technologies *Seattle, WA*

- Implemented Verilog RTL for a low-power WiFi backscatter chip, supporting IEEE 802.11b MAC/PHY across all data rates and reducing active RF power from milliwatts to tens of microwatts, enabling standards-compliant communication with commodity WiFi devices.
- Improved verification efficiency by 30% by developing cocotb-based testbenches and targeted simulations, ensuring correctness and robustness of MAC/PHY functionality before FPGA/ASIC synthesis.
- Collaborated with a team of engineers to accelerate design readiness for ASIC flow, synthesizing the Wi-Fi MAC/PHY on FPGA hardware and optimizing RTL with Synopsys Fusion Compiler, achieving measurable gains in area and power efficiency.

Undergraduate Research Assistant Jun. 2024 – Present

UCSC Hardware Systems Collective *Santa Cruz, CA*

- Extracted and processed temperature data from FPGA sensors, implementing statistical verification methods that increased sensor analysis accuracy by 20% for the 'Pentimento: Data Remanence in Cloud FPGAs' study.
- Debugged side-channel vulnerabilities by analyzing bias temperature instability (BTI) effects using custom verification techniques on sensor data.
- Eliminated 20% of outliers through advanced statistical analysis, resulting in more reliable FPGA system characterization and enhanced hardware security mechanisms.

Computer Science Intern Jun. 2024 – Dec. 2024

Datanomers *Freehold, NJ*

- Improved model accuracy by 15% by enhancing bias detection, imputation, and feature selection algorithms in EasyML's codebase.
- Resolved 30% of identified issues in the API-driven GUI through comprehensive testing and documentation.
- Collaborated with a cross-functional team to implement security improvements through penetration testing, reducing vulnerability points by 40%.

Projects

IBEX Processor Implementation & Optimization | *OpenLane, NGSpice, KLayout* Mar. 2025

- Implemented RISC-V IBEX processor using OpenLane for RTL-to-GDSII conversion, achieving zero DRC/LVS and zero timing violations.
- Reduced die area by 42% (from 2.71 mm^2 to 1.56 mm^2) through optimized floorplanning and macro placement.
- Decreased clock skew by 1 ns and achieved 5% power reduction while maintaining timing requirements across all corners.

Tuner | *SystemVerilog, Surfer, Verilator* Nov. 2024 – Dec. 2024

- Achieved real-time musical note detection with 99% accuracy using correlation-based algorithms in SystemVerilog.
- Reduced computational complexity by 40% through implementation of fixed-point arithmetic with configurable precision.
- Enhanced system reliability for continuous 44.1kHz audio processing through pipeline architecture with elastic buffers.

Technical Skills

HDL & Verification: SystemVerilog, Verilog, Cocotb, Verilator, Icarus Verilog, Spice, Ngspice
EDA Tools: Synopsys Design/Fusion Compiler, OpenLane, Yosys, KLayout, Vivado
Programming & Scripting: Python, TCL, C/C++, Java, Shell/Bash
VLSI & Digital Design: Static Timing Analysis (STA), placement & routing, DRC/LVS verification, power/delay/area optimization, signoff methodology