NITHISHWARAN S

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EDUCATION

Sri Eshwar College of Engineering	**B.E ECE**	**CGPA: 8.69(till 2nd semester)**	**2024-2028**
Sri Nachammal Vidyavani Senior Secondary School	**HSC**	**94%**	**2023-2024**
Sri Nachammal Vidyavani Senior Secondary School	**SSLC**	**96%**	**2021-2022**

INTERNSHIP

Digital System Prototyping using FPGAs **2025**

Currently undergoing a fully offline winter internship at NIELIT Calicut, focused on hands-on FPGA-based digital system design, Verilog HDL development, simulation, and hardware prototyping using AMD Vivado.

PROJECTS

FPGA-Based Smart Powerload Management System **2025**

A smart load-shedding management system that automatically and manually regulates electrical load using FSM-based control with real-time monitoring on FPGA

The system continuously monitors load values and uses an FSM to automatically switch between **normal**, **warning**, **shedding**, and **recovery** states to prevent **overload**.

FSM Based Smart Parking System **2025**

A smart parking management system that automates vehicle entry, exit, and slot allocation using password-based access and VIP identification.

The goal of this project is to efficiently manage **parking spaces**, ensure **security through password verification**, and automatically **release slots** after a set time.

Disaster Relief Connect: **2025**

A disaster response platform that alerts people in danger and connects them to nearby safe shelters and relief support.

The goal of this project is to provide **timely alerts** and **safe shelter** information to people during disasters. It also aims to support **NGO's** and **volunteers** in reaching and helping the mostly affected areas effectively.

CERTIFICATIONS

Hardware Modelling Using Verilog **(NPTEL)**	**2025**
Digital Logic Circuits and Design **(Udemy)**	**2025**
Git and GitHub **(LinkedIn Learning)**	**2025**
Hackathon Pathway: AIML and Data Science **(Google Developer Groups)**	**2025**
C and C++ Training **(IIT Bombay)**	**2024**

RESEARCH AND PAPER PUBLICATIONS

Analysis of Bootstrap Gate Driver Design for MOSFETs - eSim, FOSSEE, IIT BOMBAY (Link)	**2025**
Efficient High-Side N-Channel MOSFET Driver Circuit - eSim, FOSSEE, IIT BOMBAY (Link)	**2025**

SKILLS

HDL: Verilog | **Tools:** Cadence Virtuoso, ModelSim, Xilinx Vivado | **Programming** - C, Python(Basic), C++ | Digital Electronics , Network Theory | Git, Github

CODING PROFILE

HDL Bits : Solved 70 + problems | link
EW Skills : Solved 50 + problems | link
Leetcode : Solved 30 + problems | link
Skill Rack : Solved 900 + problems | link

AWARDS AND HONOURS

Received **First Prize** in the **One day Hackathon on VLSI Design Sprint** (Inter-College)	**2025**
Shortlisted in **Sri Eshwar's ICPC** to Continental Round	**2025**
Selected as a **Student Mentor** for 1st year students	**2025**