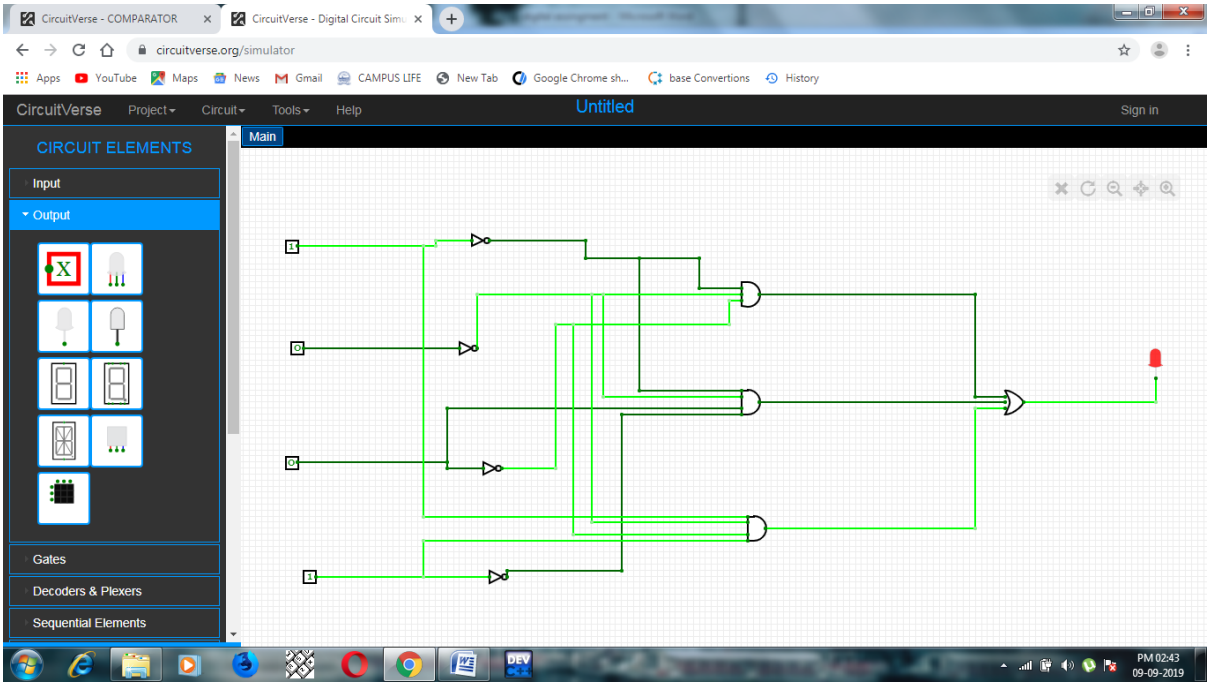
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

F=+ A’B’C’D’+A’B’C’D+A’B’CD’+AB’C’D

Simplify :

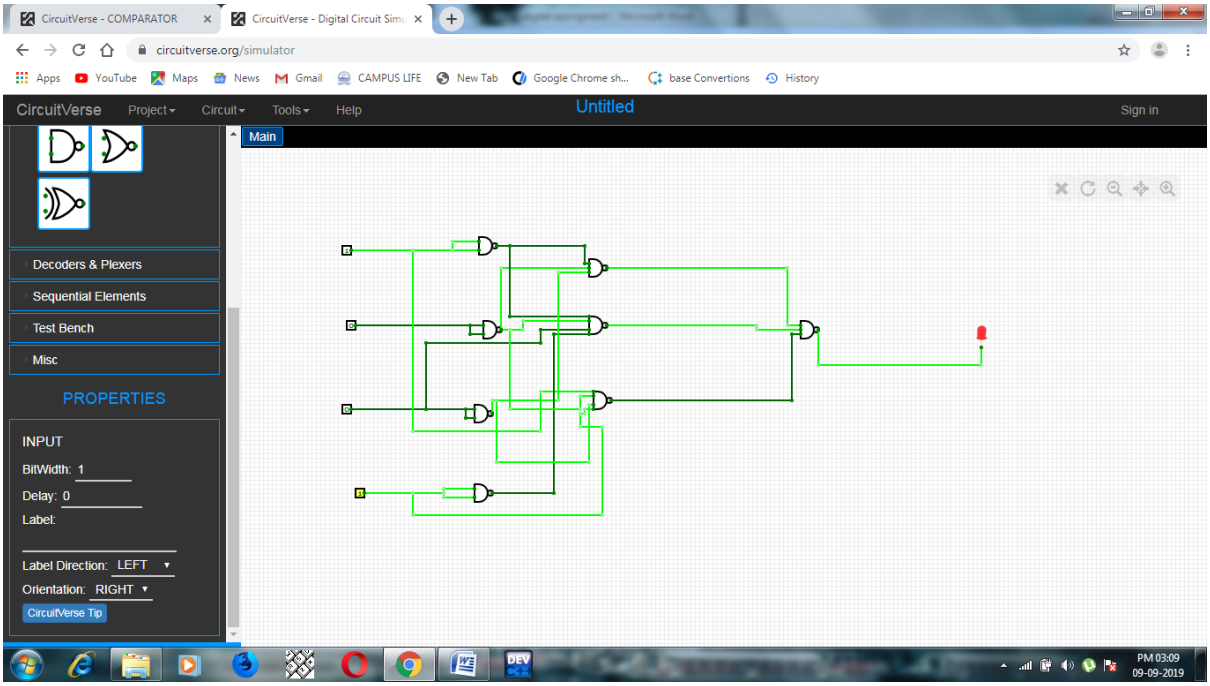
F=A’B’C’+A’B’CD’+AB’C’D

Combinational circuit



Using NAND gate:

Positive case:



Negative case: