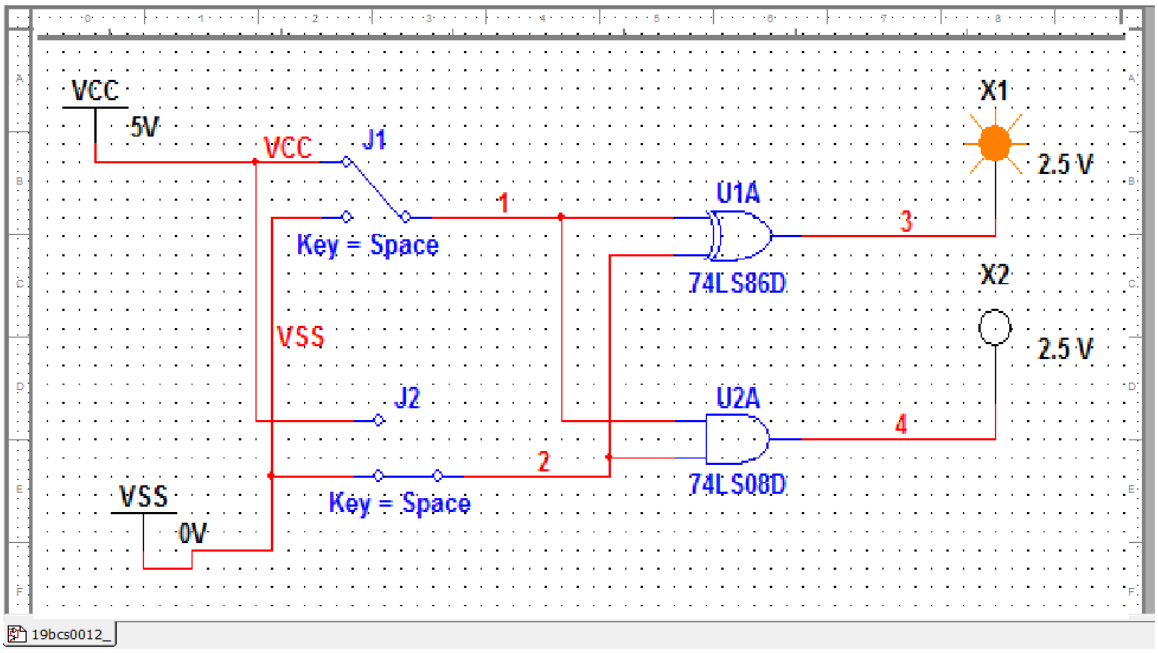
DIGITAL ASSIGNMENT (2)

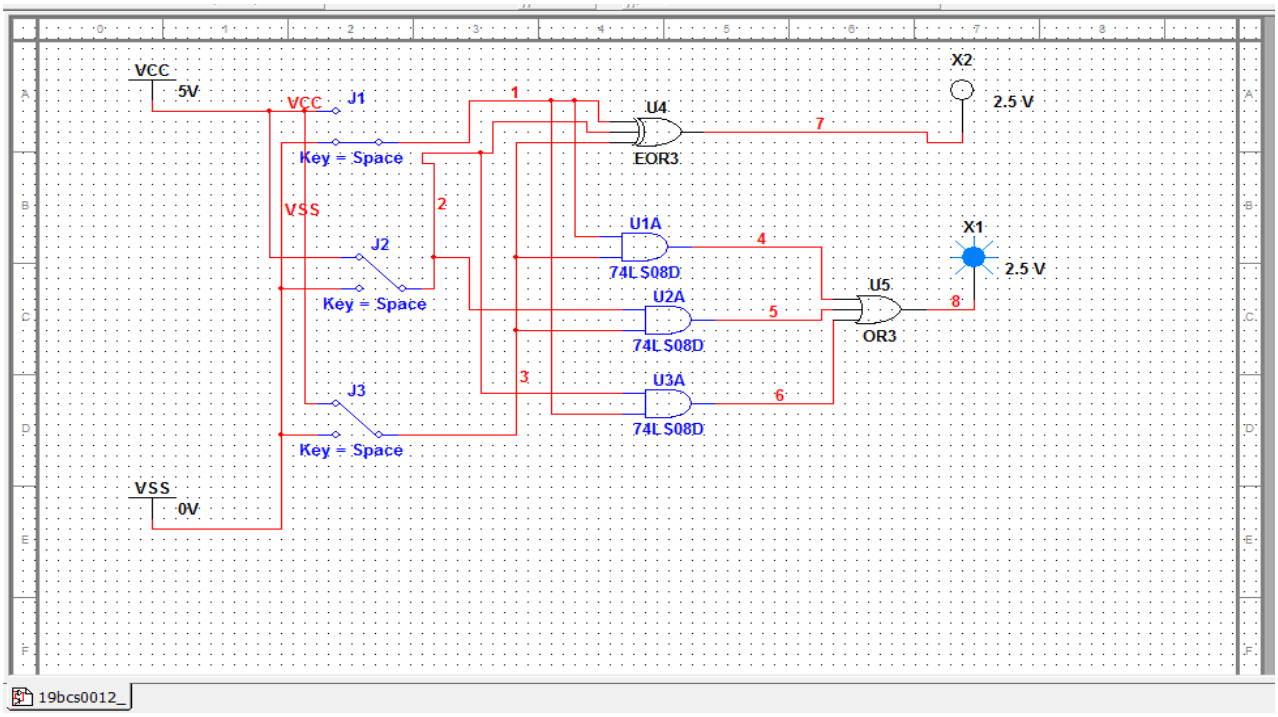
REG NO:19BCS0012

NAME:NITHISH.G

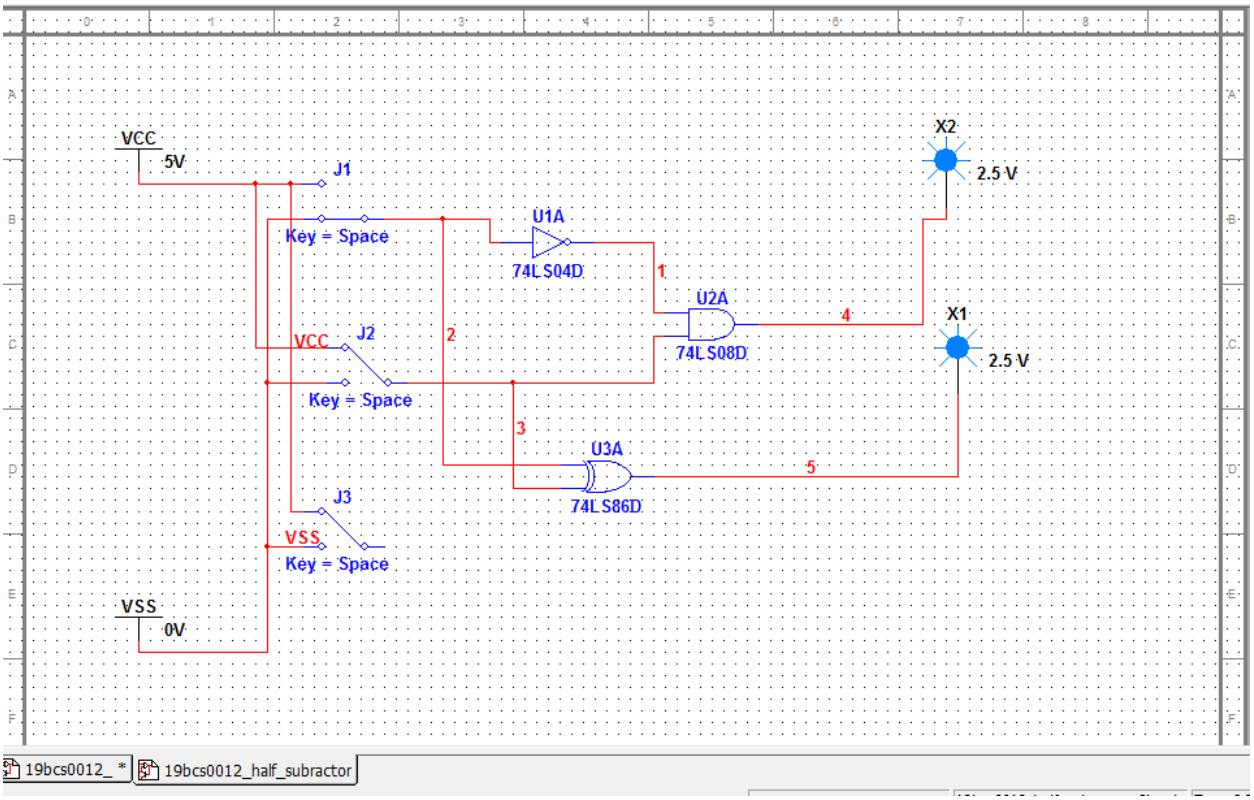
HALF ADDER



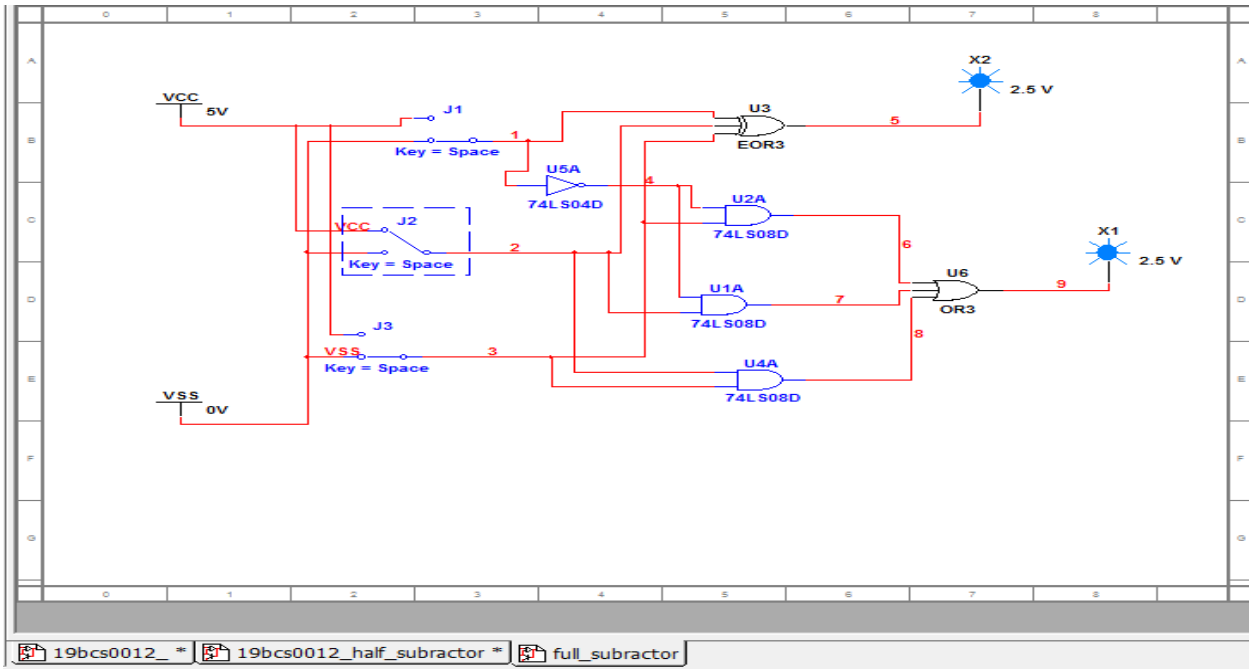
FULL ADDER



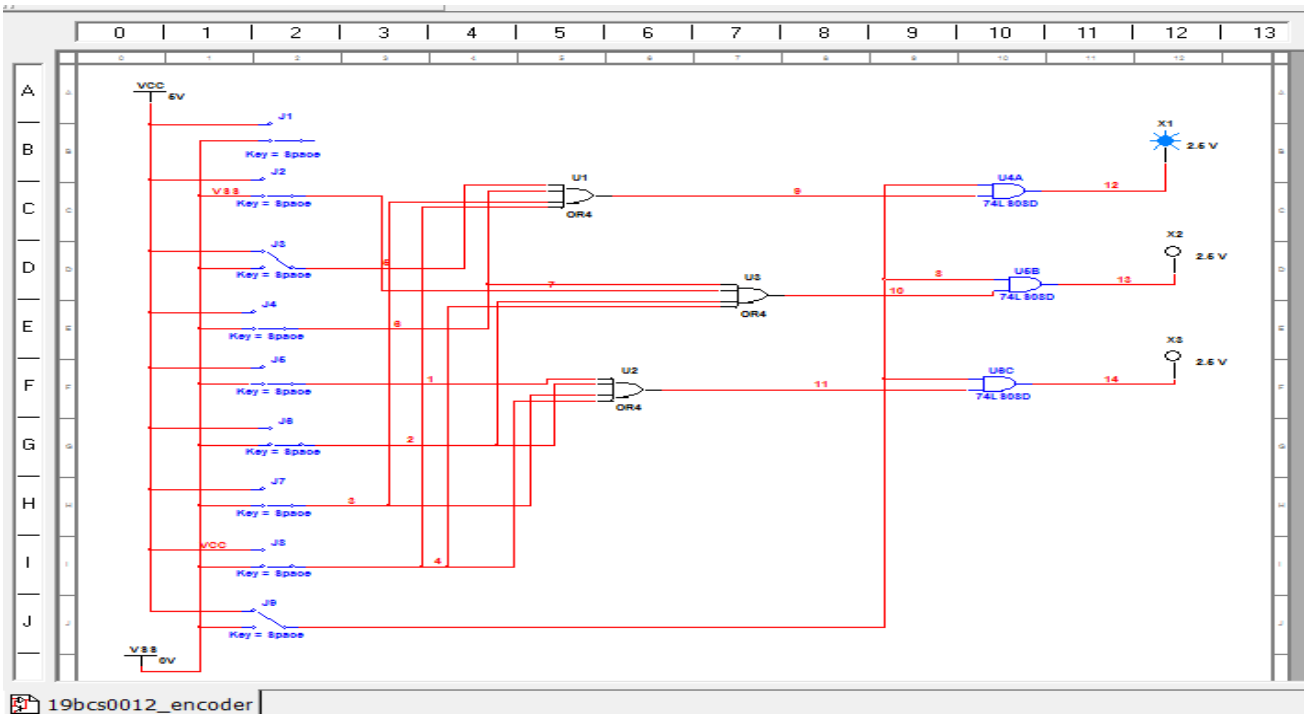
Half subractor



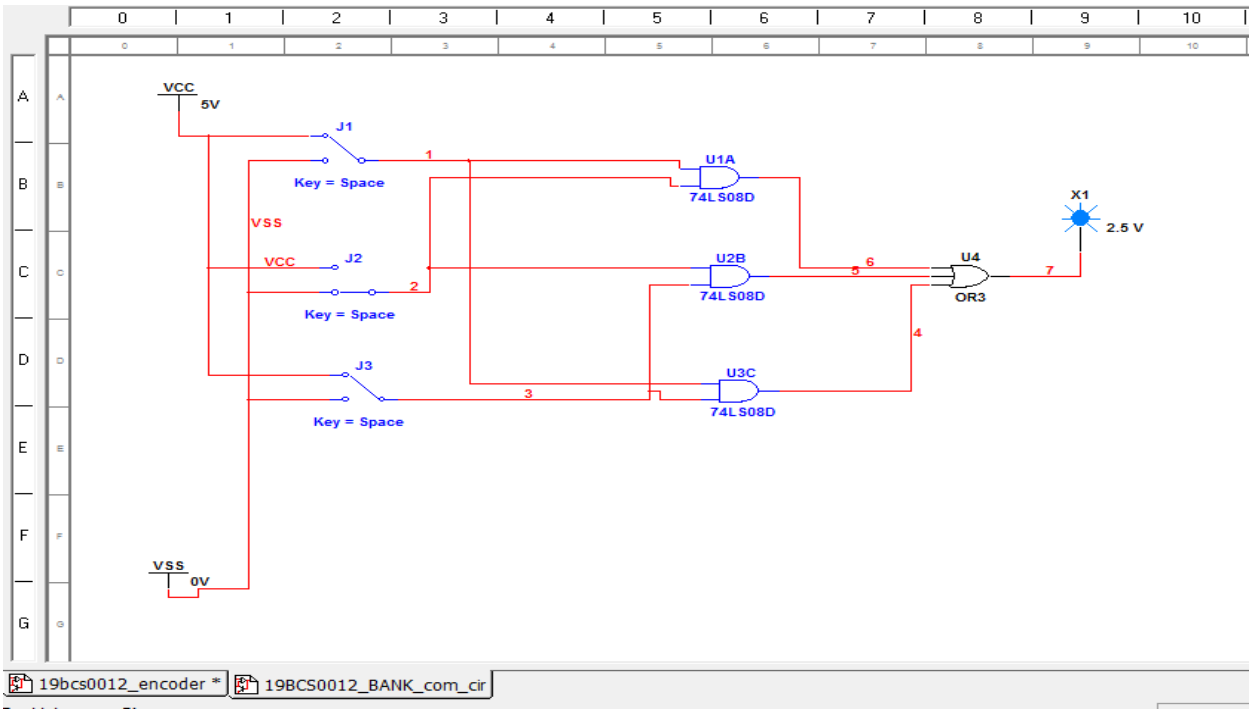
Full subractor



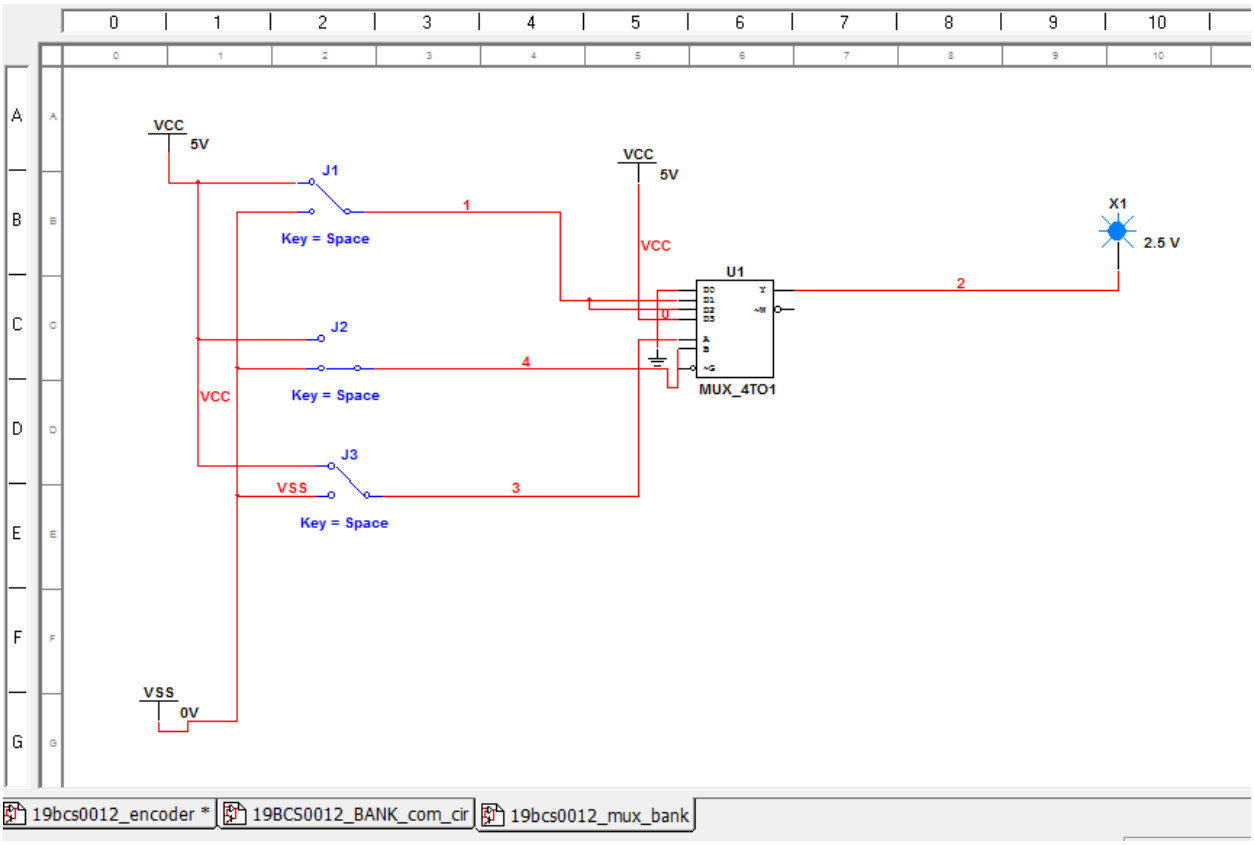
ENCODER



Bank combinational circuit


VCC
5V
J1
Key = Space
1
U1A
74LS08D
VSS
VCC
J2
2
Key = Space
U2B
74LS08D
6
5
U4
OR3
7
X1
2.5 V
4
J3
3
Key = Space
U3C
74LS08D
VSS
0V
19bcs0012_encoder *
19BCS0012_BANK_com_cir

Mux for bank


VCC
5V
J1
Key = Space
1
VCC
5V
X1
2.5 V
VCC
U1
2
0
J2
4
Key = Space
VCC
MUX_4TO1
J3
VSS
3
Key = Space
VSS
0V
19bcs0012_encoder *
19BCS0012_BANK_com_cir
19bcs0012_mux_bank