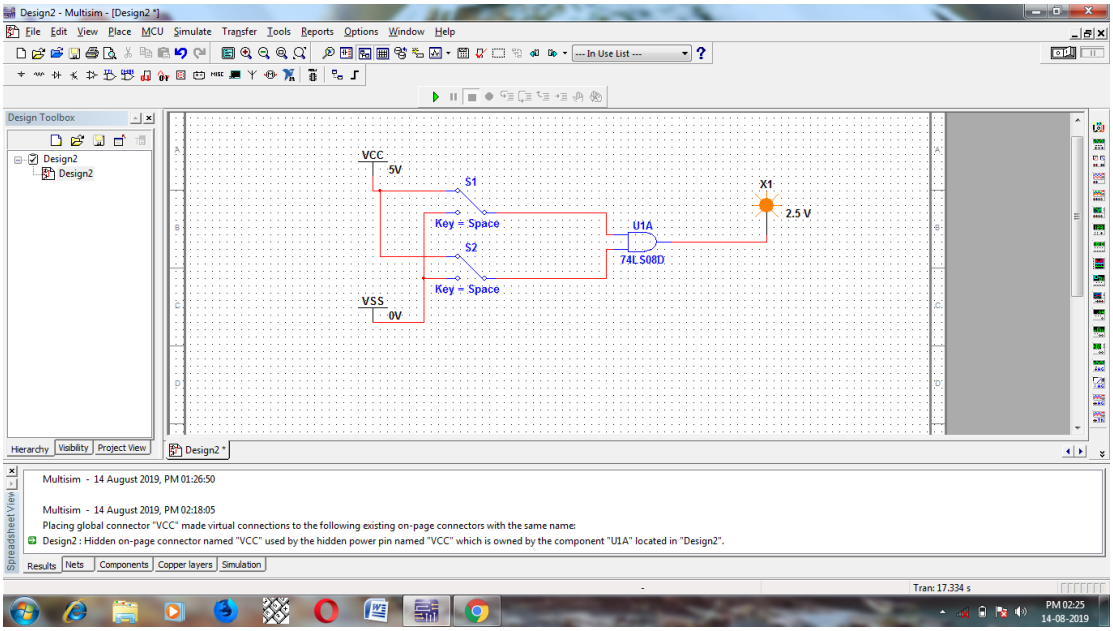
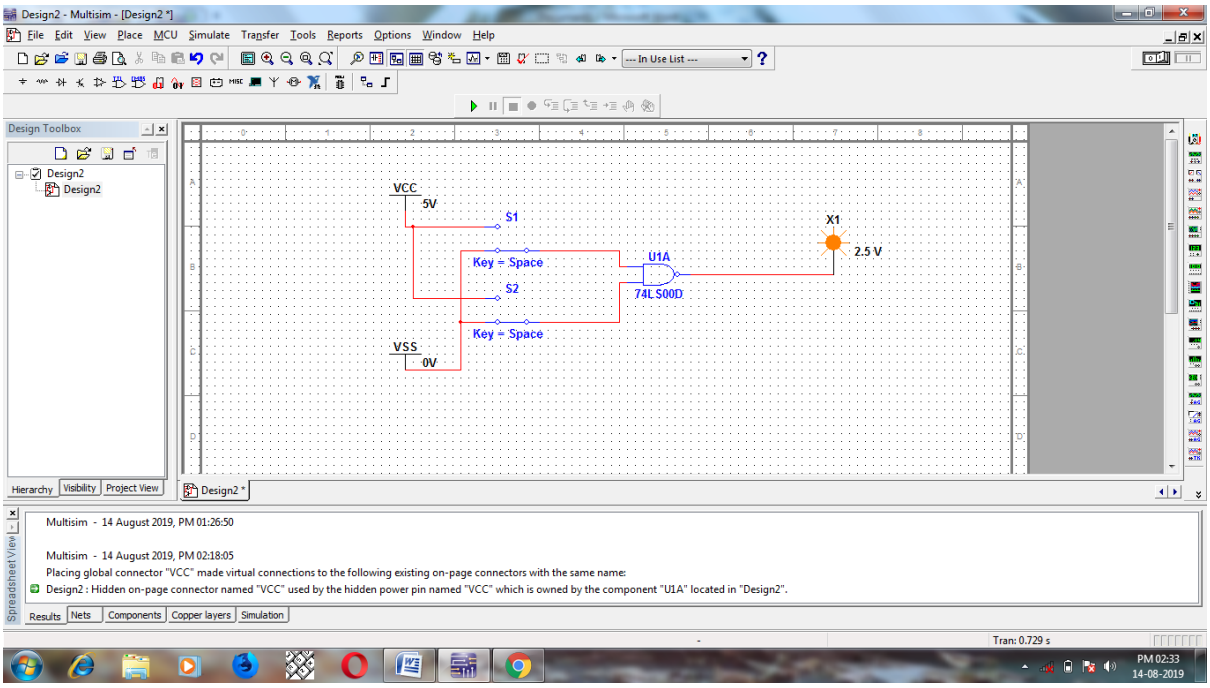
VERIFICATION OF GATES

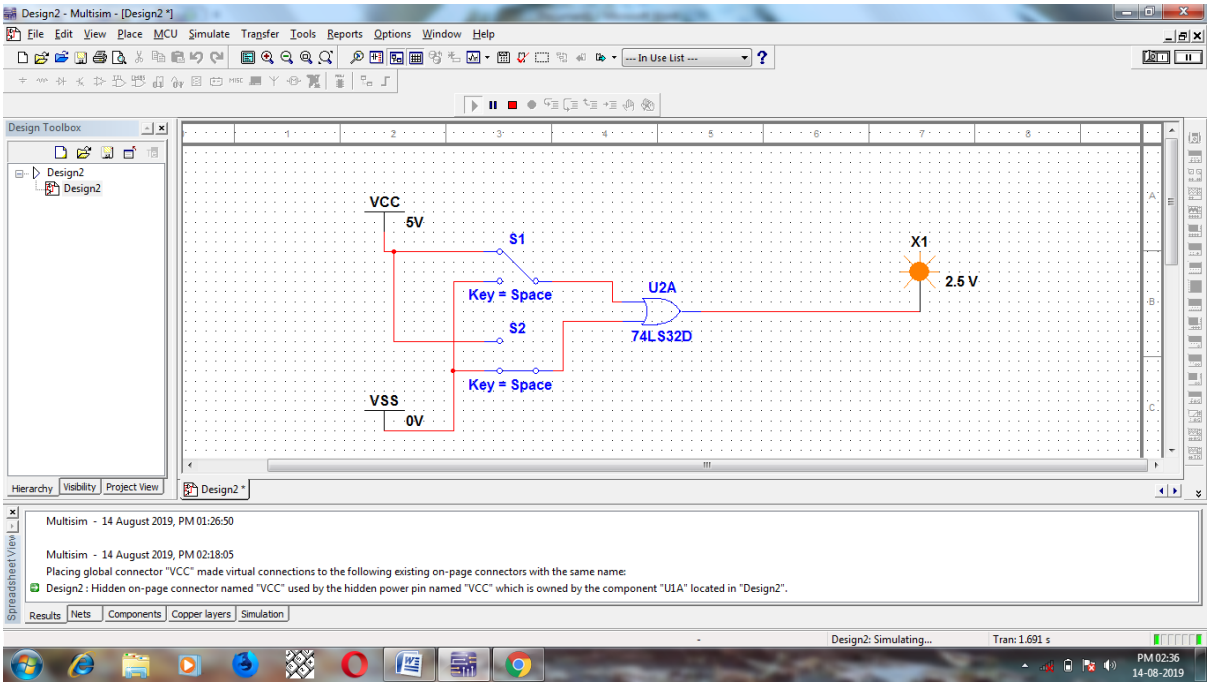
1.AND GATE



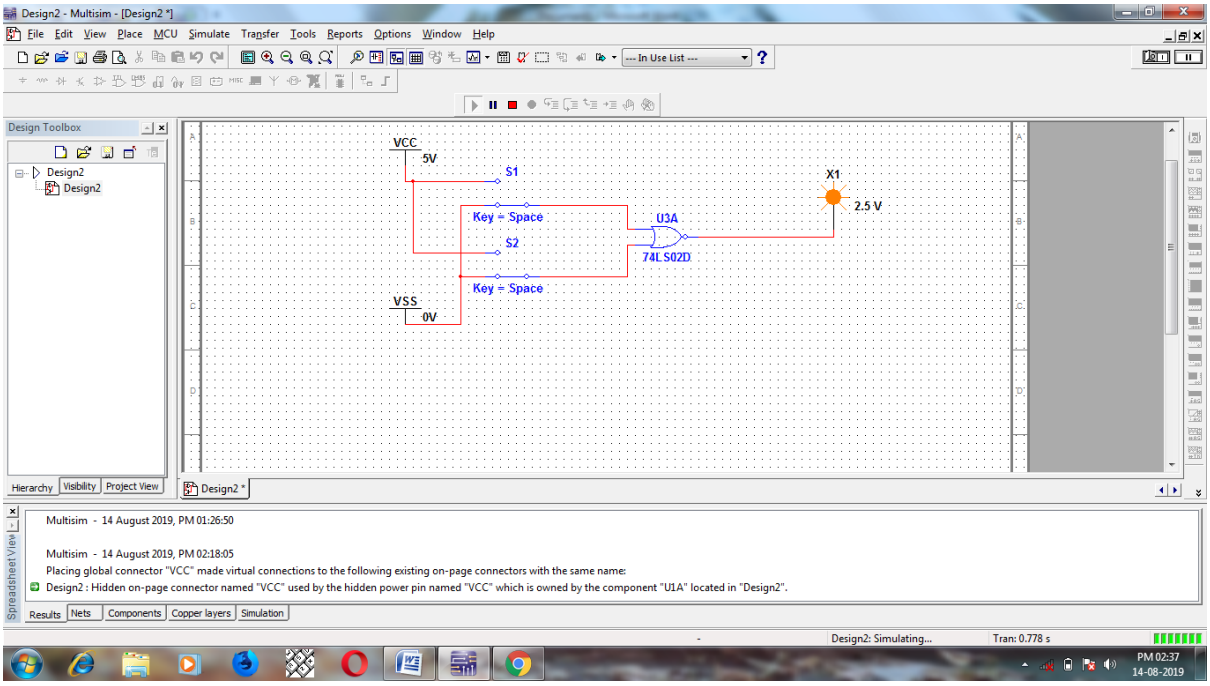
2.NAND GATE



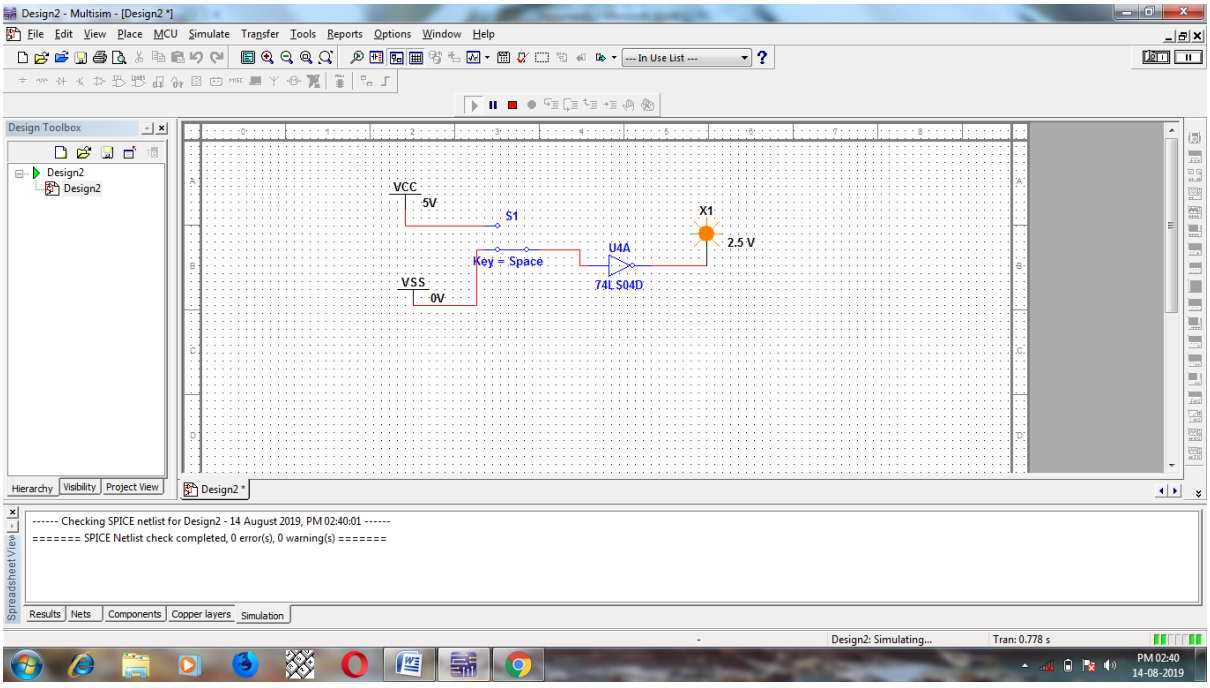
3.OR GATE



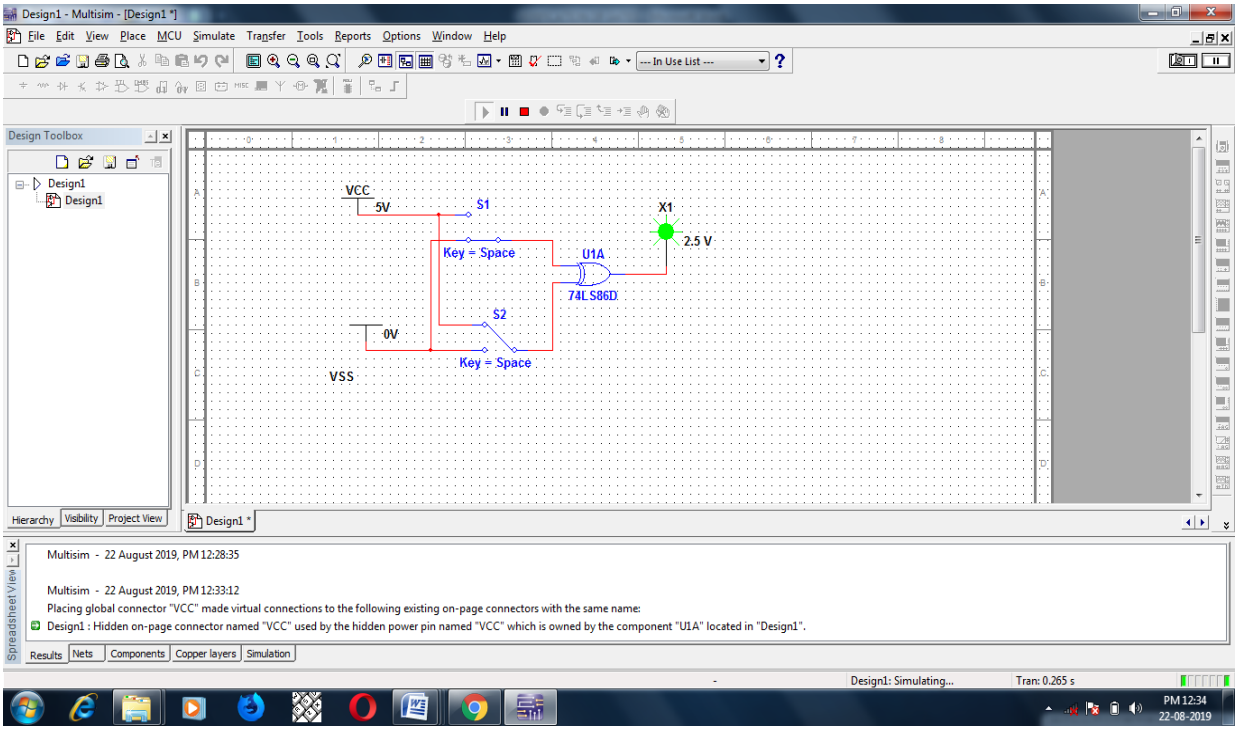
4.NOR GATE



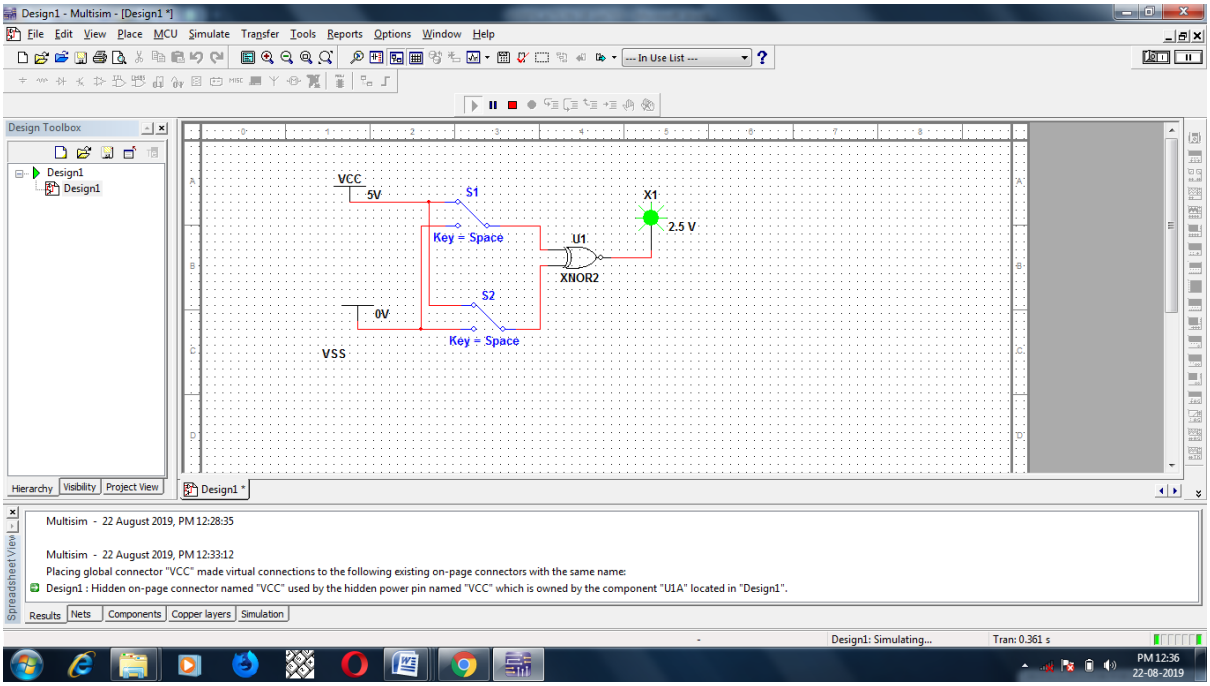
5.NOT GATE



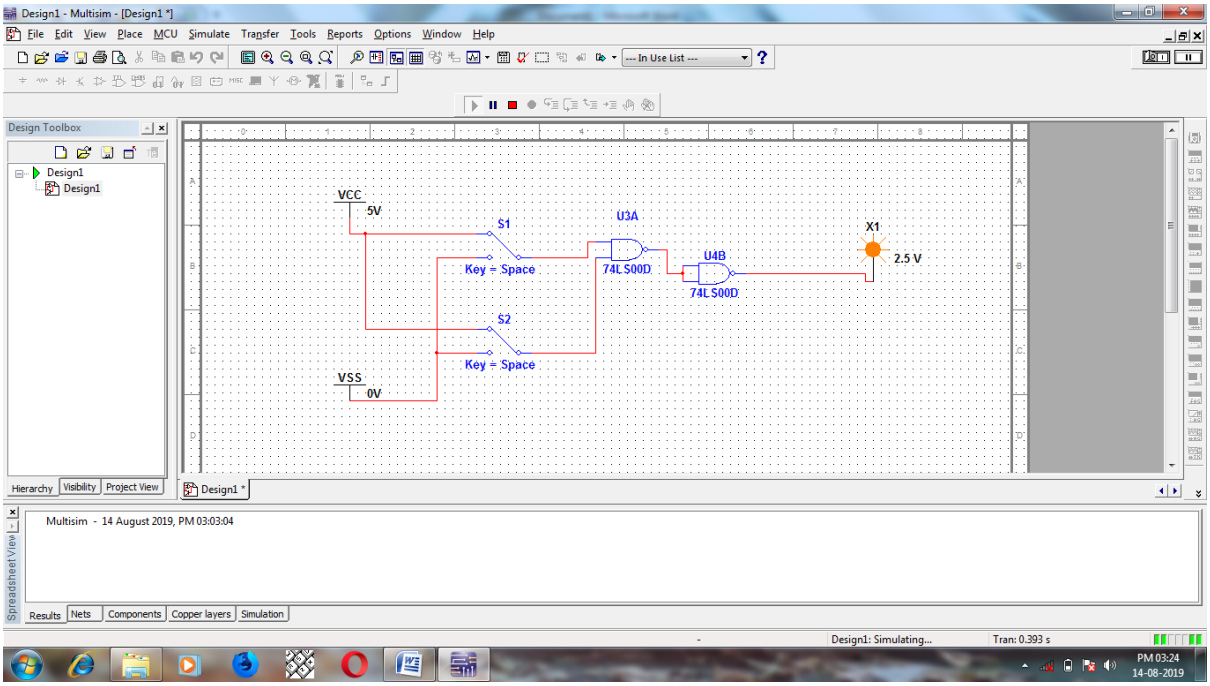
6.XOR GATE



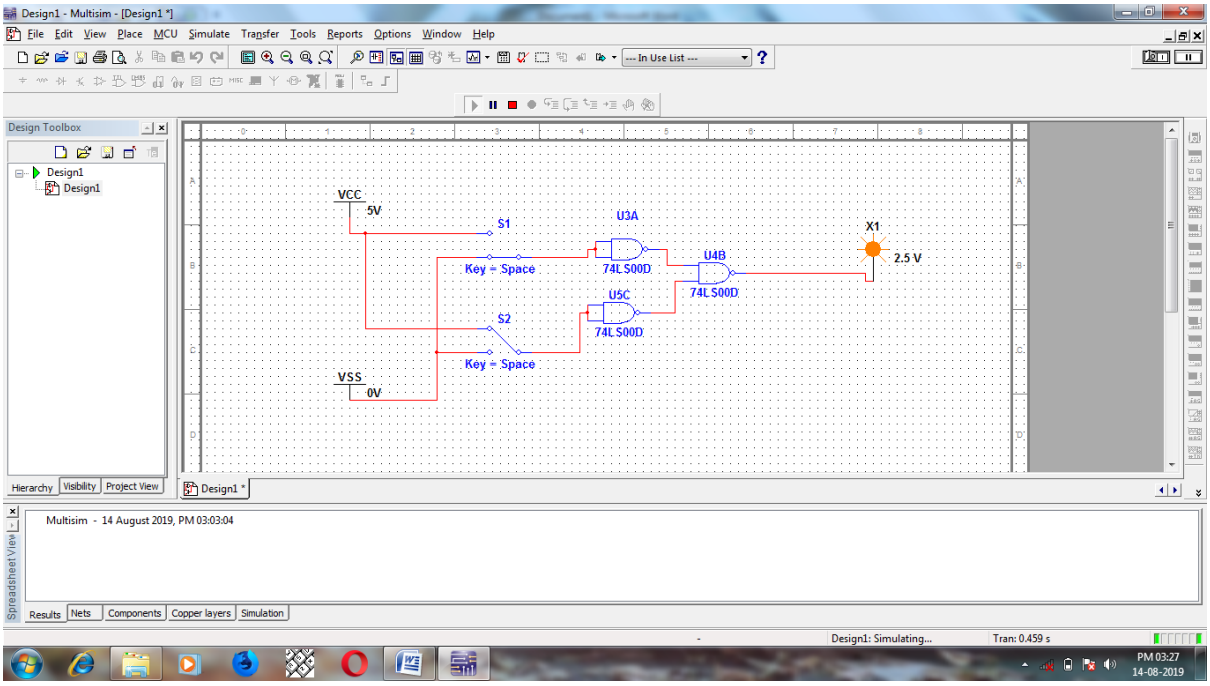
7.XNOR GATE



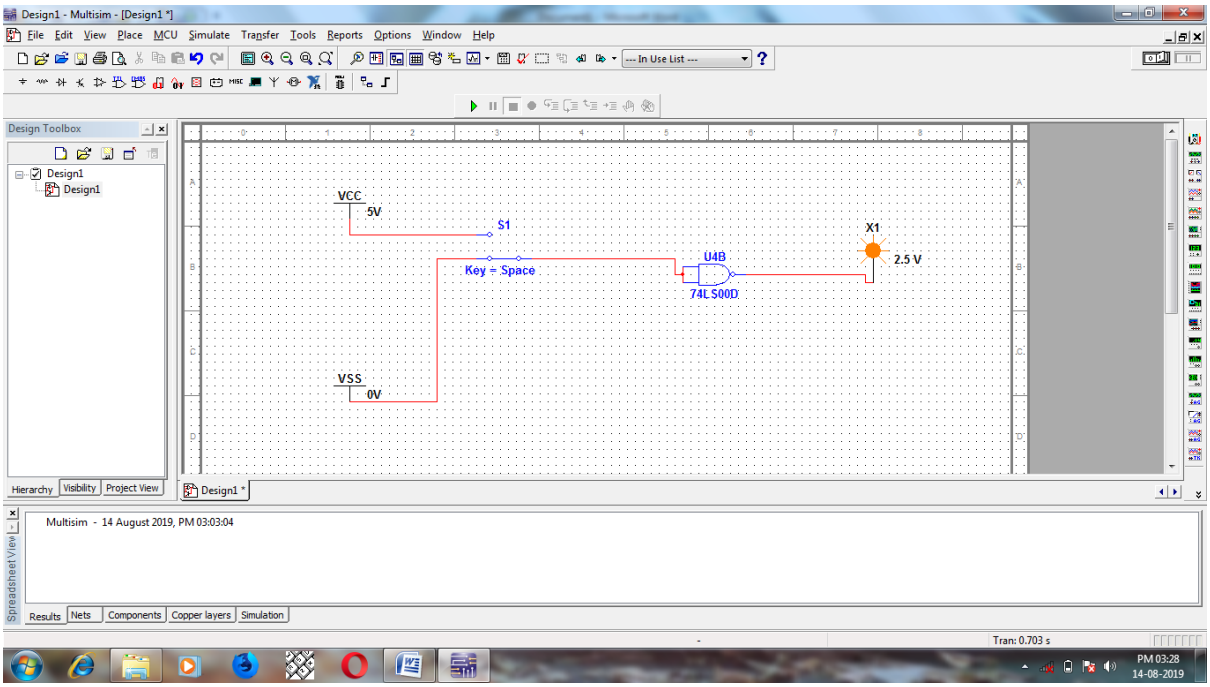
8.realizing NAND as AND gate



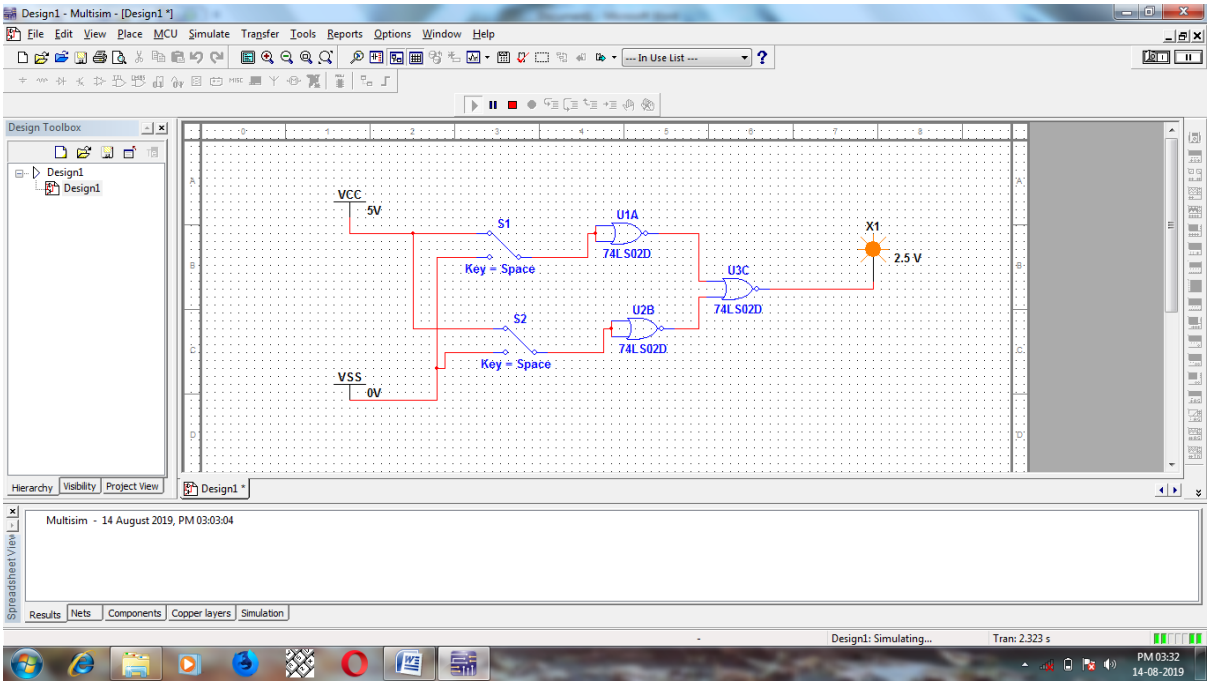
9.realizing NAND as OR gate



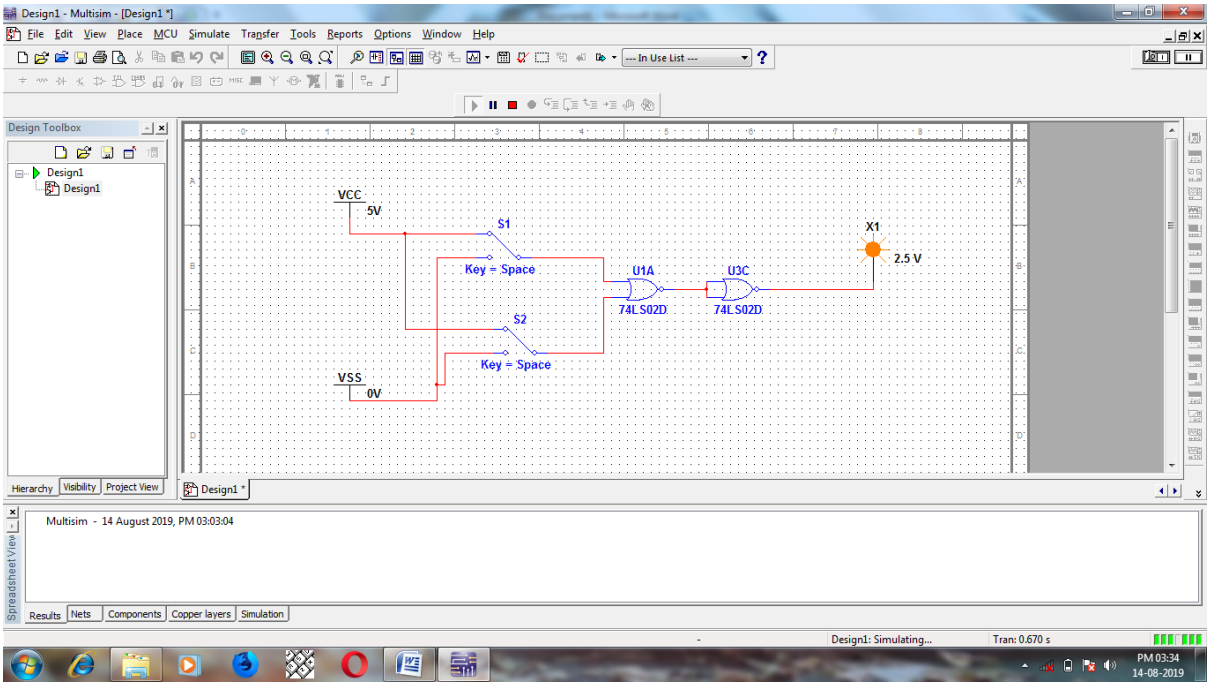
10. REALIZING NAND AS NOT



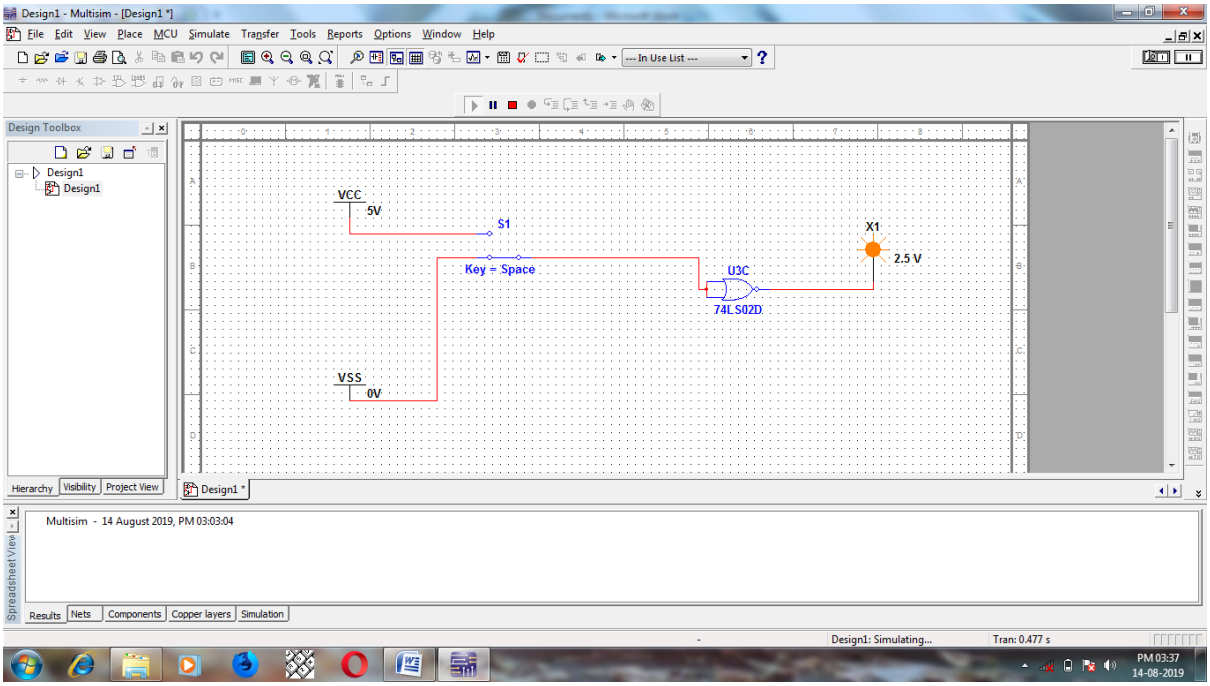
11. REALIZING NOR AS AND GATE



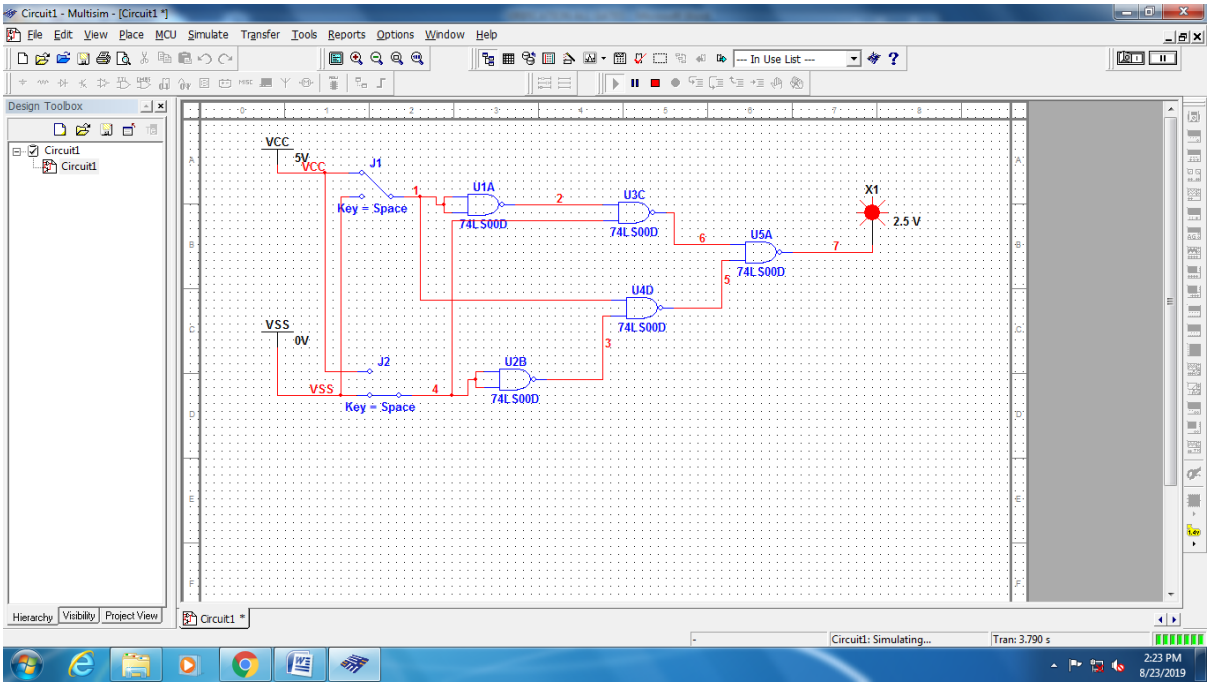
12.REALIZING NOR AS OR



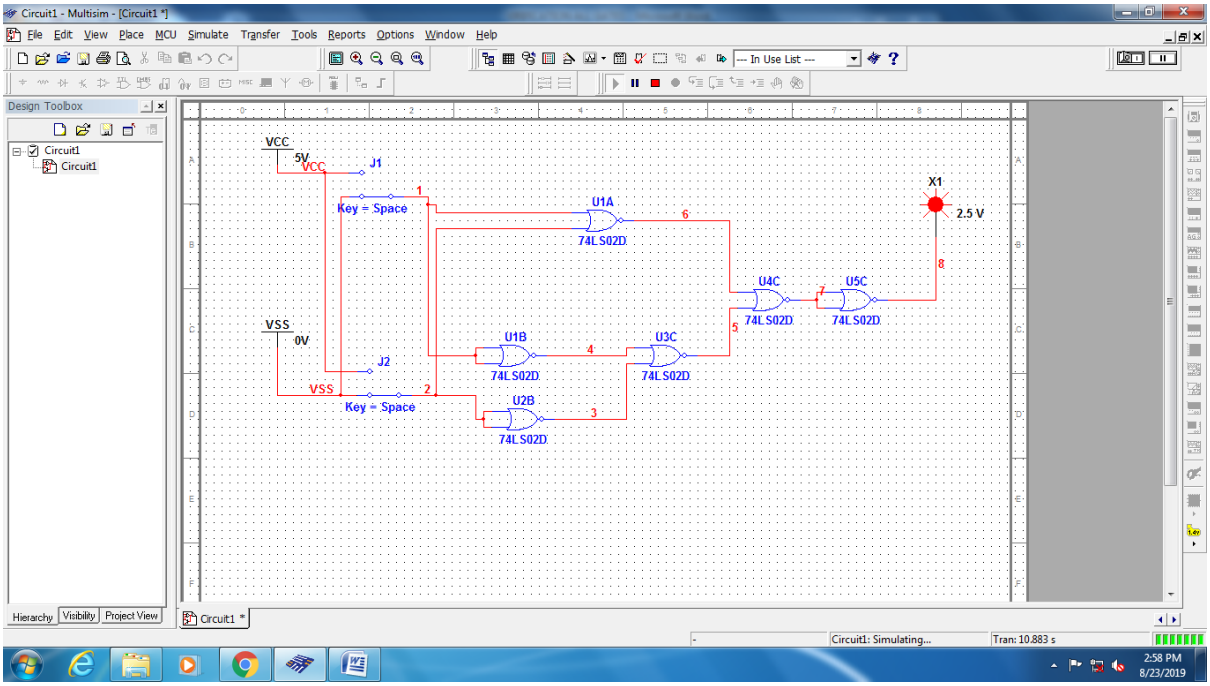
13.REALIZING NOR AS NOT



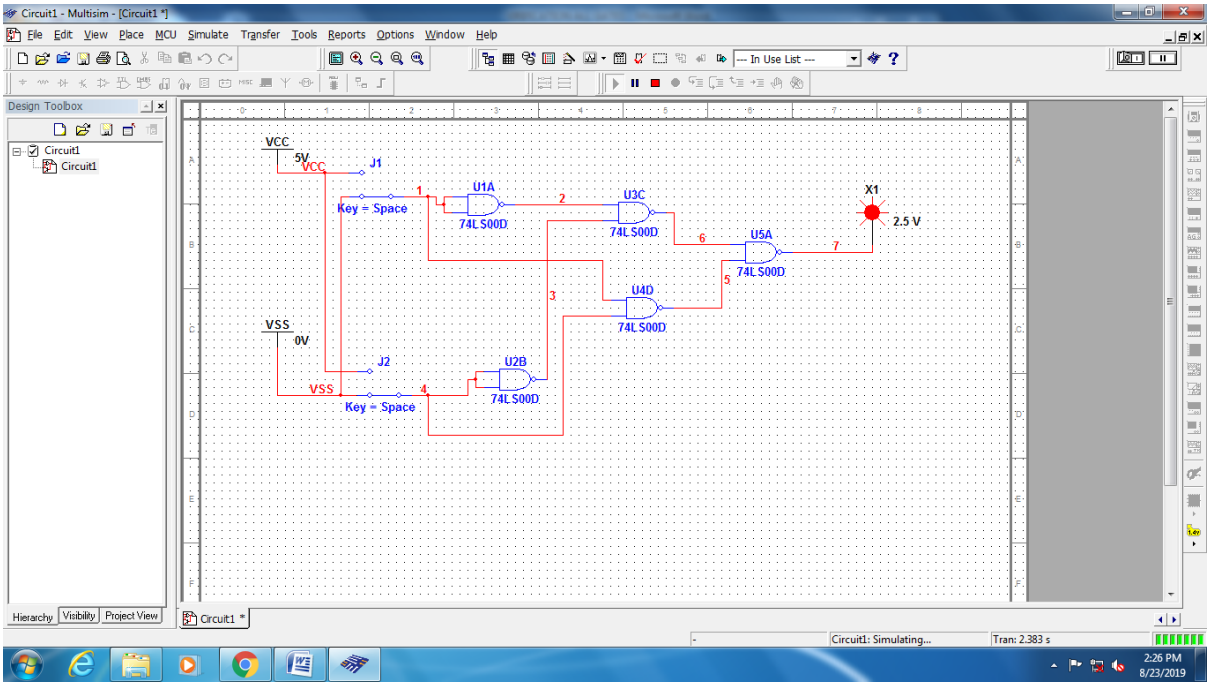
14.EX-OR Using NAND



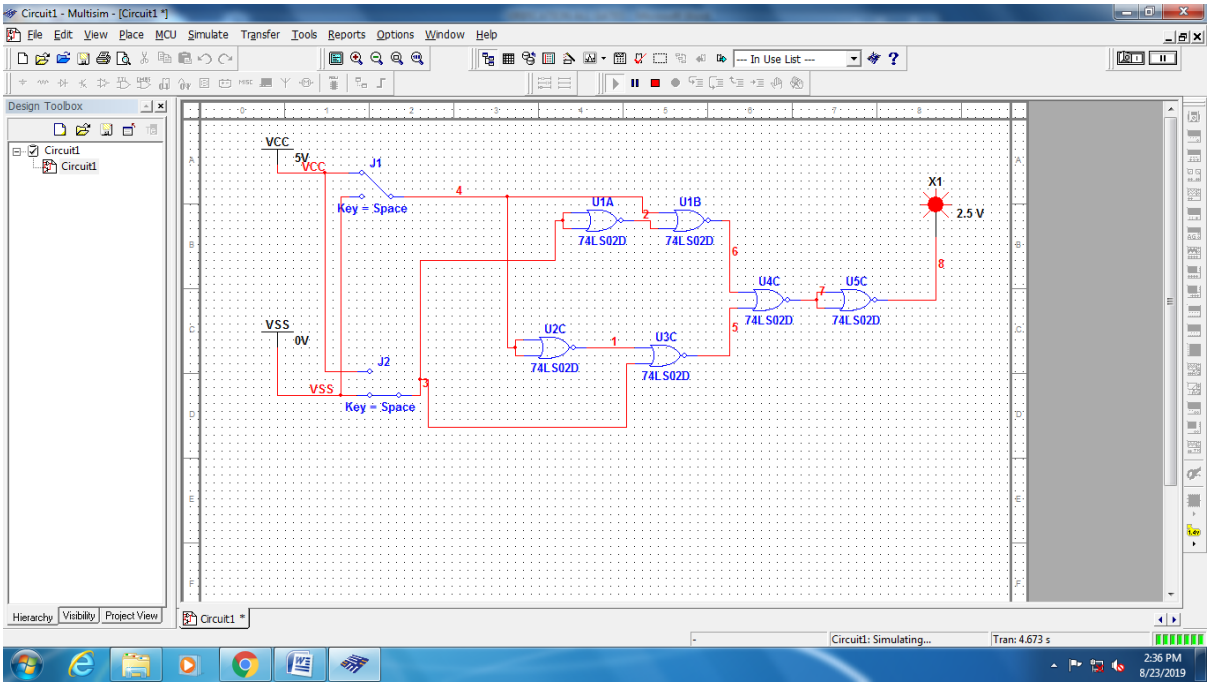
15.EX-NOR using NOR



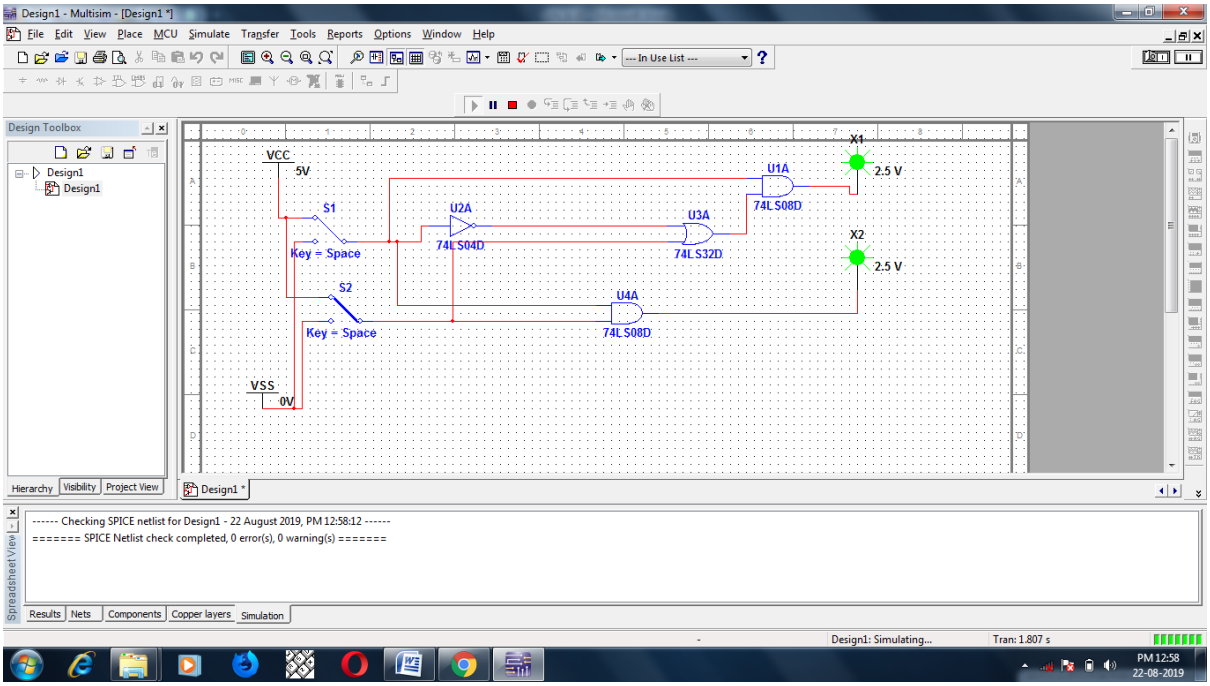
16.EX-NOR USING NAND



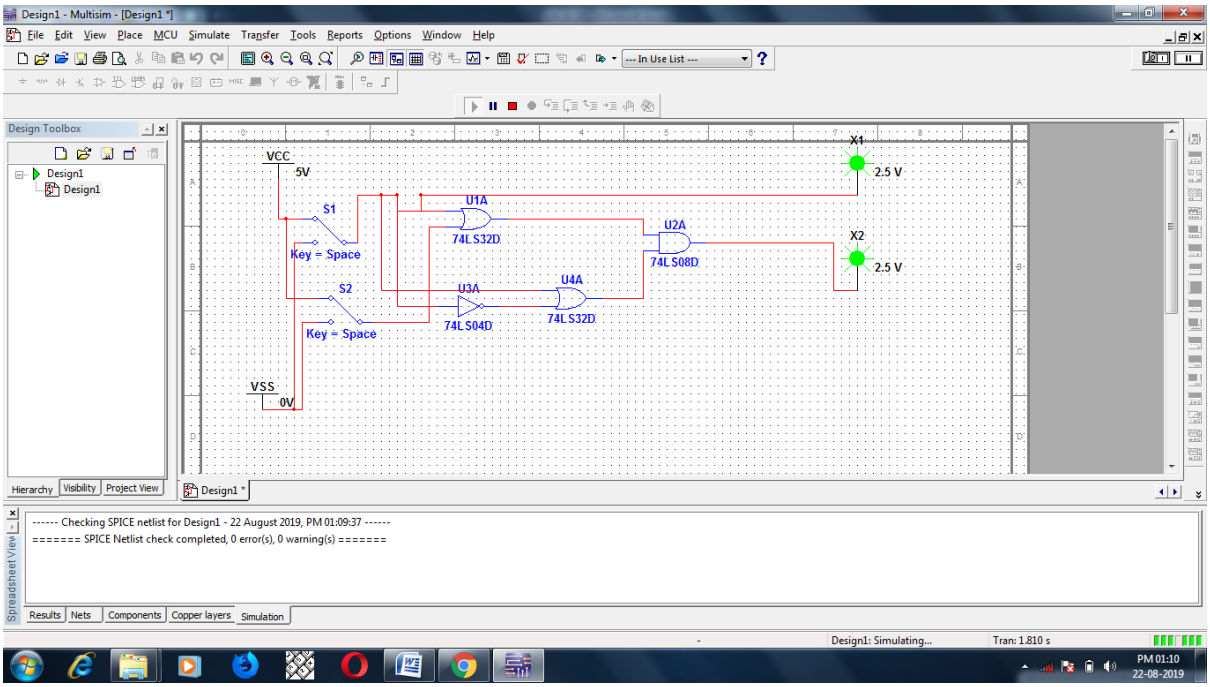
17.EX-OR using NOR



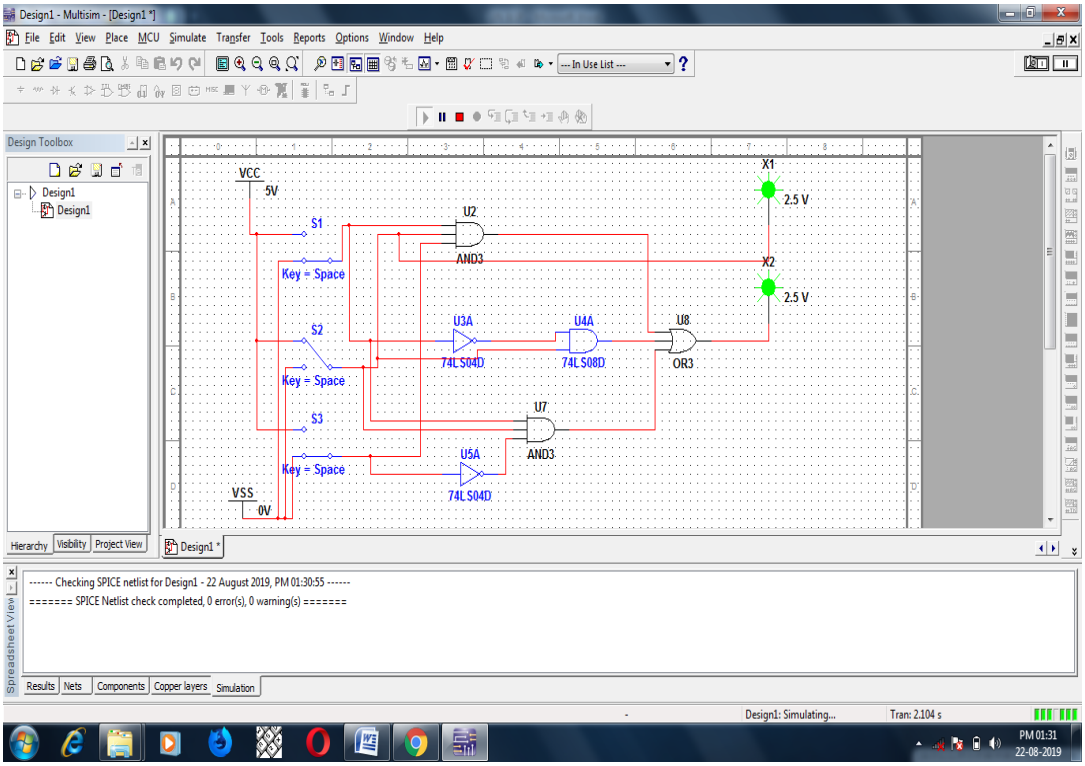
18.X(x'+y)=xy



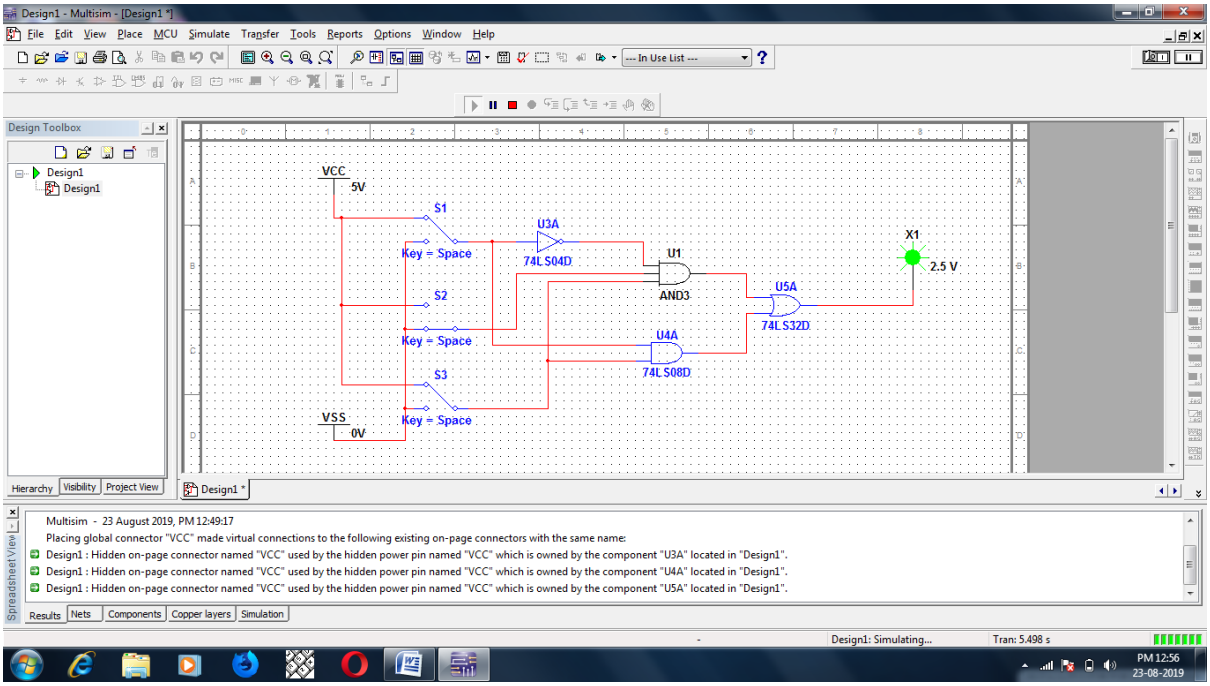
19.(x+y) (x+y')=x



20.XYZ+X'Y+XYZ'=Y



21.X’YZ+XZ


Design1 - Multisim - [Design1 *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
Design1
Design1
VCC
5V
S1
Key = Space
U3A
74LS04D
U1
AND3
X1
2.5 V
U5A
74LS32D
S2
Key = Space
U4A
74LS08D
S3
Key = Space
VSS
0V
Hierarchy Visibility Project View
Design1 *
Multisim - 23 August 2019, PM 12:49:17
Placing global connector "VCC" made virtual connections to the following existing on-page connectors with the same name:
Design1 : Hidden on-page connector named "VCC" used by the hidden power pin named "VCC" which is owned by the component "U3A" located in "Design1".
Design1 : Hidden on-page connector named "VCC" used by the hidden power pin named "VCC" which is owned by the component "U4A" located in "Design1".
Design1 : Hidden on-page connector named "VCC" used by the hidden power pin named "VCC" which is owned by the component "U5A" located in "Design1".
Spreadsheet View
Results Nets Components Copper layers Simulation
Design1: Simulating...
Tran: 5.498 s
PM 12:56
23-08-2019