

Programme : B.Sc (Computer Science)

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Course : System Software
(CSC1013)

Digital Assignment-1

1) write about the different instruction formats used in SIC and SIC/XE.

Ans:

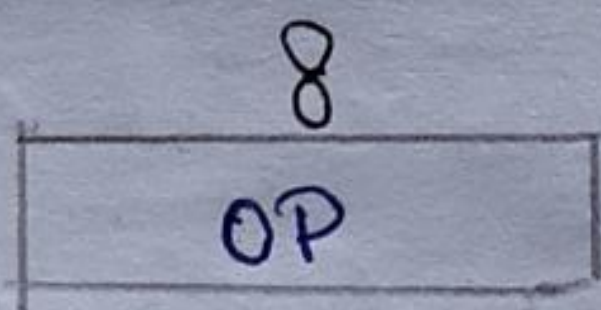
SIC Machine Architecture instruction format:

→ The Simplified instruction computer has three instruction formats.

- Format 1
- Format 2
- Format 3

Format 1:

→ Consists of 8 bits of allocated memory to instruction.

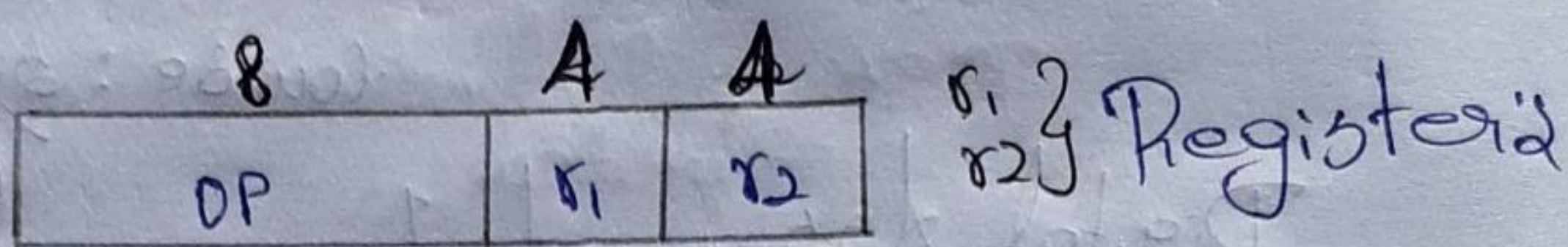


Format 1 (1 byte);

Format 2:

→ Consists of 16 bits of allocated memory to store 8-bits of instruction and two 4-bits segments to store operand

Format 2 (2 bytes):-



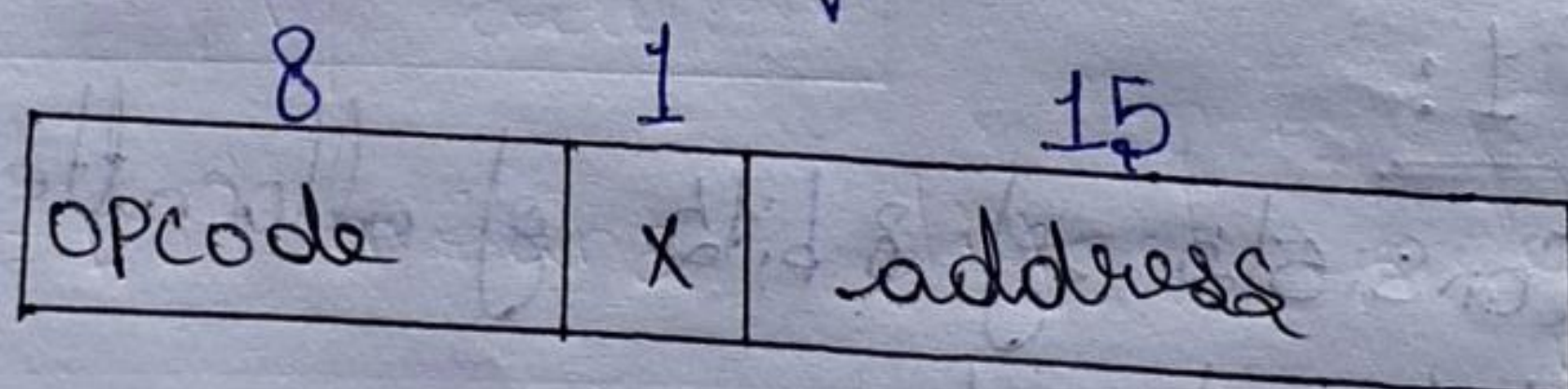
Format 3:

★ Consists of 6 bits to store an instruction, 6 bits of flag values, and 12 bits of displacement.

★ The length of the instruction format-3

24-bit format

★ The flag bit-x is used to indicate indexed-addressing mode:-



Instruction Set:-

↳ Format 3

↳ Load and store registers (LDA, LDX, STA, STX,)

↳ Integer arithmetic operation (ADD, SUB, MUL, DIV)

↳ Compare instruction (comp)

↳ Conditional jump instruction (JLT, JEQ, JGT)

↳ JSUB jumps to the subroutine, placing the return address in register 1.

↳ RSUB returns by jumping to the address contained in register 2.

SIC Instruction formats:

• SIC instruction formats has four type of instruction formats.

They are:-

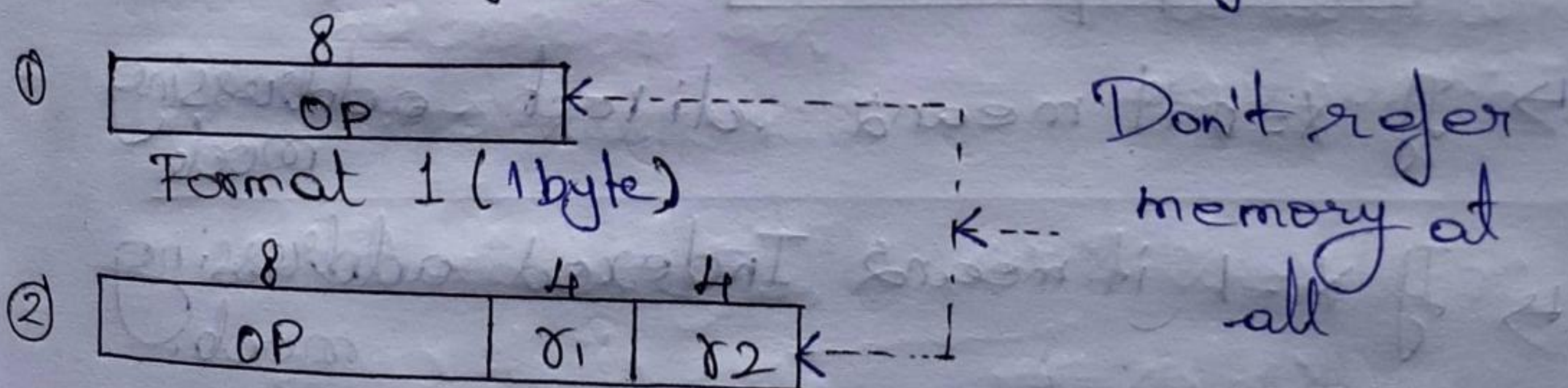
↳ Format 1 ↳ Format 2

↳ Format 3 ↳ Format 4

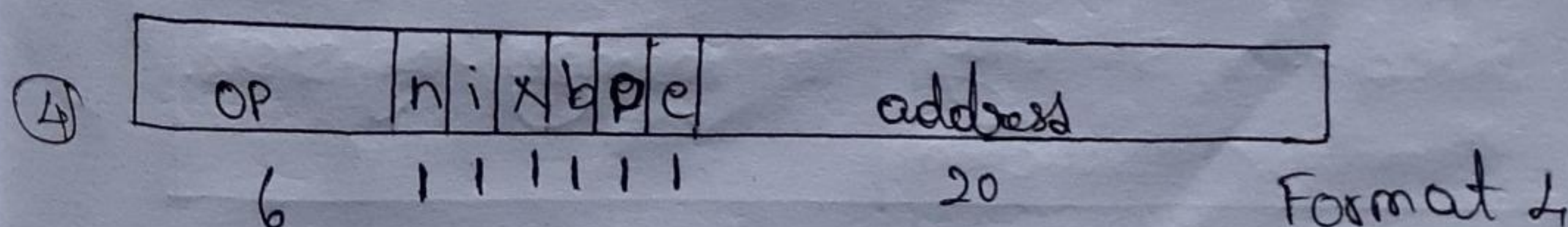
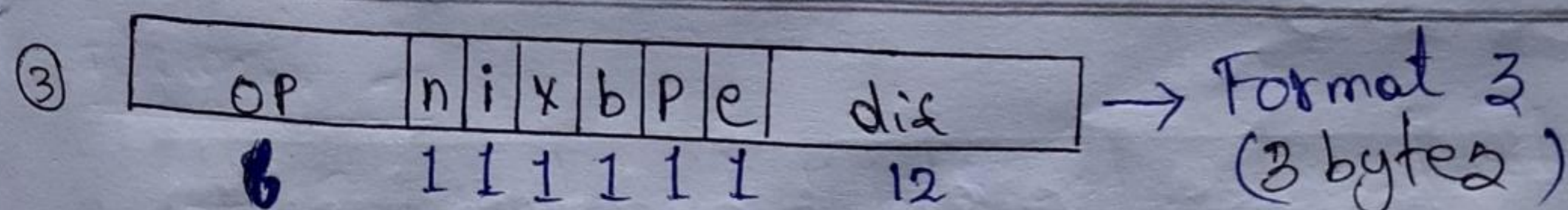
* Relative addressing format 3 ($e=0$)

* Extend the address to 20 bit 5 - format 4 ($e=1$)

* Don't refer memory at all - formats 1 and 2



Format 2 (2 bytes)



2.7 What are addressing mode? Explain the addressing modes used in SIC and SIC/XE.

SIC Addressing modes:-

* There are two addressing mode available:-

↳ Indicated by x bit in the instruction.

↳ (x) represents the contents of reg x .

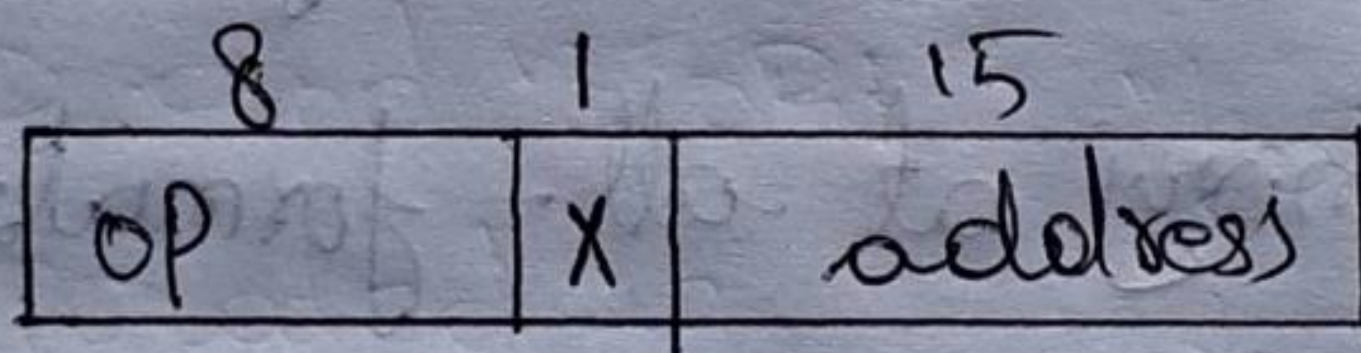
Mode Indication Target address calculation:-

Direct $x=0$ $TA = \text{address}$

Indexed $x=1$ $TA = \text{address} + (x)$

Explanation:-

* All instruction in SIC have 24 bit format



↳ If $x=0$ it means direct addressing mode

↳ If $x=1$ it means Indexed addressing mode.

SIC/XE Addressing modes:-

↳ $n i x b p e$

↳ Simple $n=0, i=0$ (SIC) or $n=1, i=1$

↳ Immediate $n=0, i=1$ $TA = \text{Value}$

↳ Indirect $n=1, i=0$ $TA = (\text{operand})$

↳ Base relative $b=1, p=0$ $TA = (B) + \text{disp}$

$$0 \leq \text{disp} \leq 4095$$

↳ PC relative $b=0, p=1$ $TA = (PC) + \text{disp}$

$$-2048 \leq \text{disp} \leq 2047$$

Explanation

↳ If $b=1, p=0$ then it is Base relative and the target address calculation $TA = (B) + \text{disp}$
($0 \leq \text{disp} \leq 4095$)

↳ If $b=0, p=1$ then it is Program counter relative and the target address $TA = (PC) + \text{disp}$
($-2048 \leq \text{disp} \leq 2047$)

↳ Direct $b=0, p=0$ $TA = \text{disp}$

↳ Index + Base relative $x=1, b=1, p=0$ $TA = (B) + \text{disp} + (x)$

↳ Indirect

⇒ Index

$X=1$

$$TA_{new} = TA_{old} + (X)$$

→ Index +

PC relative

$X=1, b=0, P=1$

$$TA = (PC) + disp + (X)$$

→ Index + Direct

$X=1, b=0, P=0$

→ Format 4

$e=1$

3.7 Compare CISC and RISC (5 Points)

	CISC	RISC
1.	Emphasis on Hardware	Emphasis on software
2.	Includes multi-clock Complex instructions	Single clock, reduced instruction only
3.	Memory to Memory "LOAD" and "STORE" incorporated in Instruction.	Register to Register "LOAD" and "STORE" are independent Instruction.
4.	Small code sizes, High cycles per second.	Large code sizes, Low clock cycles per second.
5.	Transistors are used for storing complex instruction	Spend more transistors on memory registers.