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COURSE : COMPUTER ARCHITECTURE

CODE : CSC2004

Digital Assignment - 3

17 (a) How many 512X8 RAM Chips are needed to Provide a memory capacity of 2048X8?

Soln:

Available memory chip size $M_{N,W}$:

$N \times W : 512 \times 8$

Required memory size : $N' \times W'$

$N' \times W' : 2048 \times 8$

Here

Condition : $N' > N$ & $W' = W$

Increase number of words by the factor "P"

$$P = \left[\frac{N'}{N}\right]$$

$N' = 2048$

$N = 512$ $\quad P = \left[\frac{N'}{N}\right] \Rightarrow \left[\frac{2048}{512}\right]$

$$\boxed{P = 4 //}$$

∴ The no. of chips need to Provide a memory capacity of 2048×8 is "4" //

(b) How many 128×4 RAM chips are needed to provide a memory capacity of 1024×8?

Soln

Available memory chip Size:

$$N \times W = 128 \times 4$$

Required memory Size:

$$N' \times W' = 1024 \times 8$$

Here condition:

$N' > N$ & $W' > W$

Increase number of words by the factor of P &

* Increase the word size of a memory by a factor of 9.

$$P = \left[\frac{N'}{N}\right] \Rightarrow \left[\frac{1024}{128}\right]$$

$$P \Rightarrow 8 //$$

$$q = \left[\frac{W'}{W}\right] \Rightarrow \left[\frac{8}{4}\right]$$

$$q = 2 //$$

$$P * q \Rightarrow 8 \times 2$$

$$\Rightarrow 16 //$$

$$\therefore P * q = 16$$

∴ The no. of chips needed to Provide a memory capacity of 1024×8 is 16 //

(2) Design 256 x 16 - bit ROM using 128 x 8 - bit ROM

Soln

Available memory N x W = 128 x 8

Required memory N' x W' = 256 x 16

$P = \left[\frac{N'}{N}\right]$ $q = \left[\frac{W'}{W}\right]$

P = 2 q = 2

Condition:

$N' > N$ & $W' > W$

Increasing word size and
Increasing no. of words

∴ P * Q = 2 x 2 = 4 memory chips of 128 x 8. are required to construct 256 x 16 bit ROM

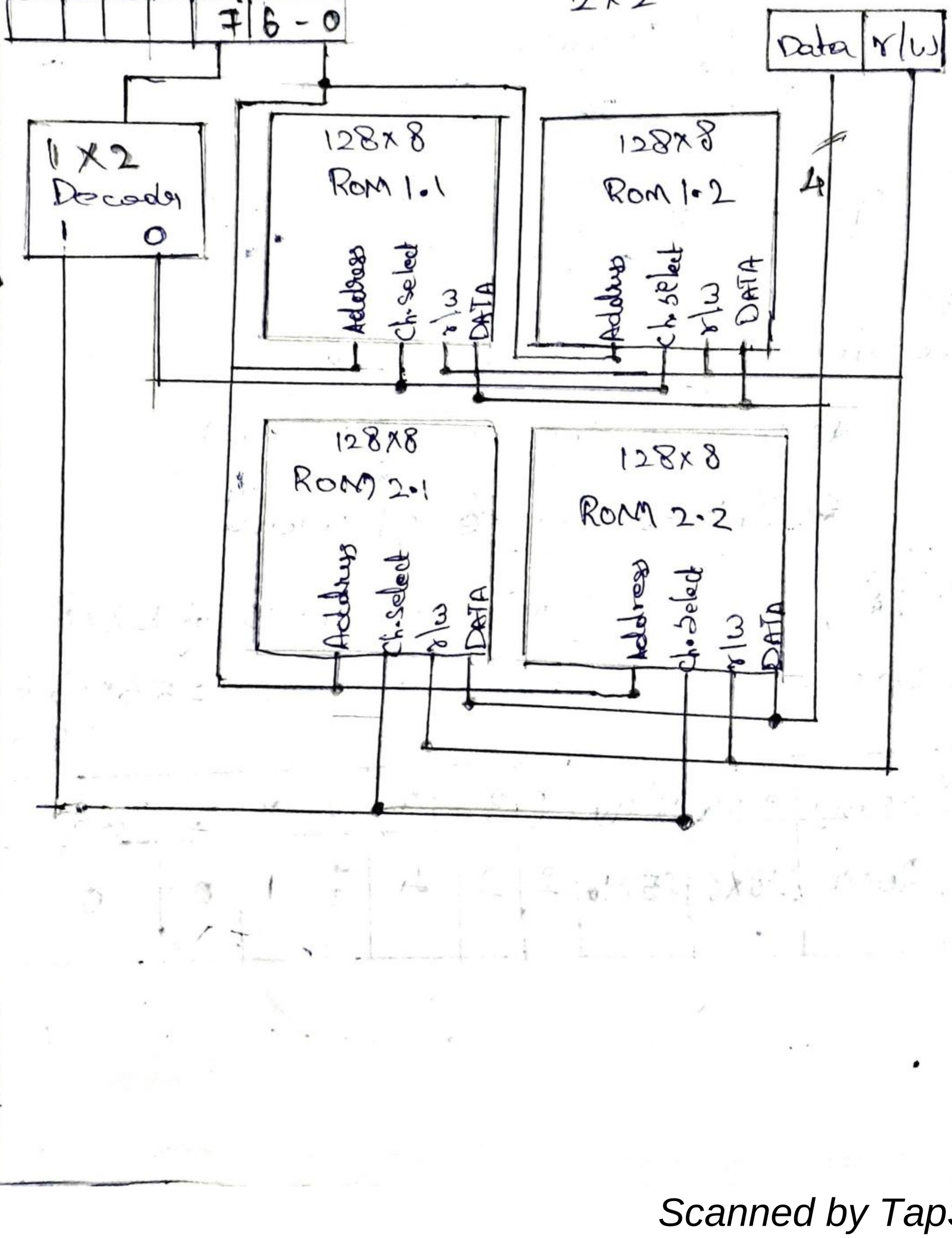
Memory	N x W	N' x W'	P	Q	P * Q	X	Y	Z	Total
ROM	128 x 8	256 x 16	2	2	4	1	1	0	8

memory address mapping:-

Component	Hexadecimal add.		Address Bus										
	From	To	10	9	8	7	6	5	4	3	2	1	0
ROM 1.1	0000	7F				0	x	x	x	x	x	x	x
ROM 1.2	0000	7F				0	x	x	x	x	x	x	x
ROM 2.1	80	FF				1	x	x	x	x	x	x	x
ROM 2.2	80	FF				1	x	x	x	x	x	x	x

Memory Design

matrix Expression
2 x 2



(3) Design 2024 x 4-bit RAM using 1024 x 4-bit RAM.

Soln

Available memory N x W = 1024 x 4

N = no. of words; W = Word Size

$$P = \left[\frac{N'}{N}\right] \qquad q = \left[\frac{W'}{W}\right]$$

Required memory N' x W' = 2024 x 4

Condition:

$$N' > N \text{ \& } W' = W$$

So, it is Vertical Expansion

∴ Increasing the number of words.

$$P = \left[\frac{N'}{N}\right] \Rightarrow \left[\frac{2024}{1024}\right] \Rightarrow 2$$

$$q = \left[\frac{W'}{W}\right] = \left[\frac{4}{4}\right] \Rightarrow 1$$

∴ P * q = 2 x 1 ⇒ 2 memory chips of size 1024 x 4 are required to construct 2024 x 4 bit RAM.

S.No	Memory	N x W	N' x W'	P	q	P*q	x	y	z	Total
1.	RAM	1024 x 4	2024 x 4	2	1	2	10	1	0	11

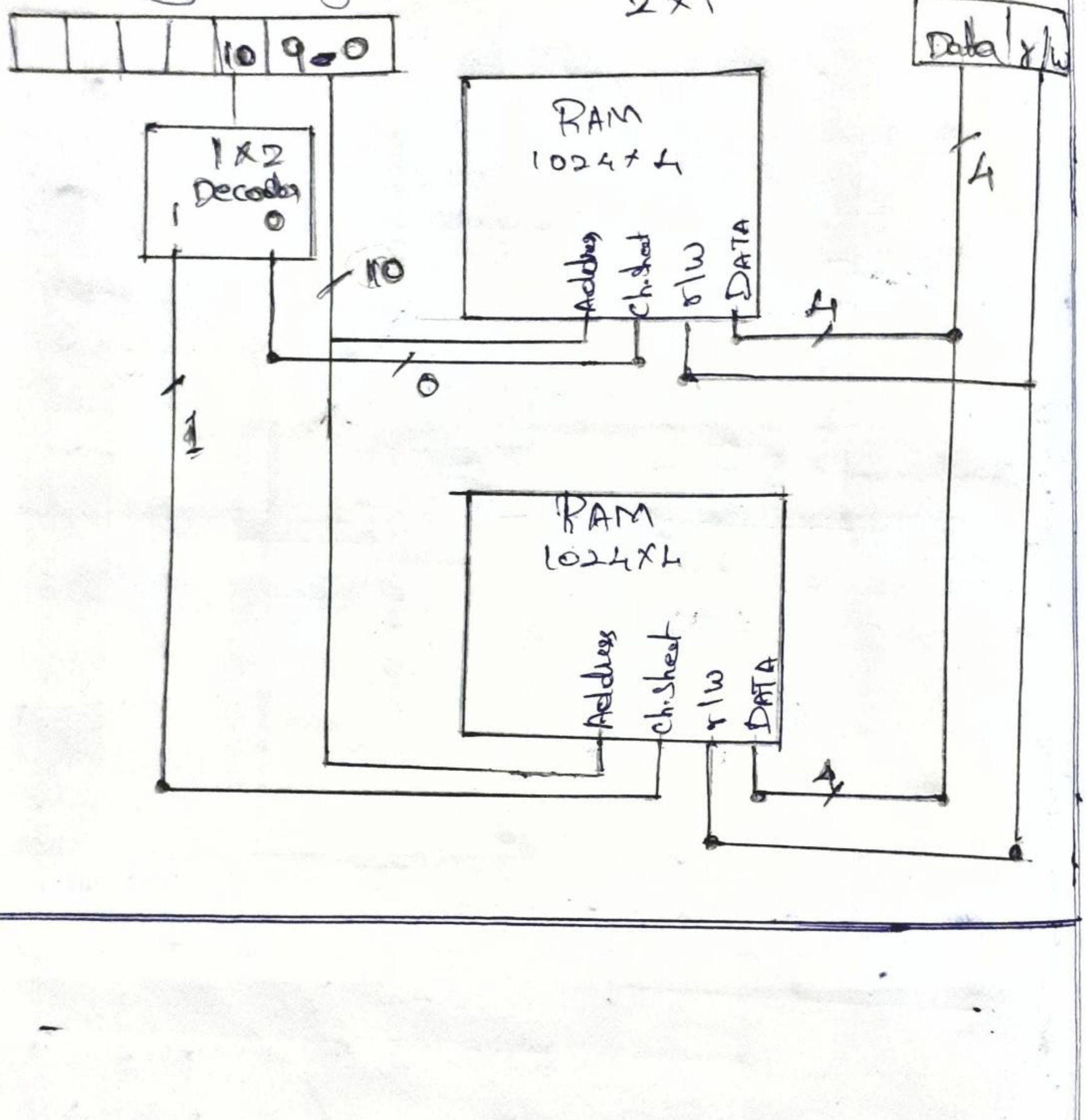
memory address map:-

component	Hexadecimal address	
	From	To
RAM 1	0000	0FFF
RAM 2	0400	07FF

Address Bus																			
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								0	0	x	x	x	x	x	x	x	x	x	x
								0	1	x	x	x	x	x	x	x	x	x	x

memory Design:-

matrix Expression
2 x 1



4) Design 256×16-bit ROM using 128×8-bit ROM chips.

Soln

Available memory $N \times W = 128 \times 8$

Required memory $N' \times W' = 256 \times 16$

N = no. of words W = word size

$$P = \left[\frac{N'}{N}\right] = \left[\frac{256}{128}\right] = 2$$

$$q = \left[\frac{W'}{W}\right] = \left[\frac{16}{8}\right] = 2$$

Condition: $N' > N$ & $W' > W$

* Increasing no. of words
* Increasing size of word

∴ $P * Q = 2 \times 2 \Rightarrow 4$ memory chips of 128×8 are required to construct 256×16 bit ROM

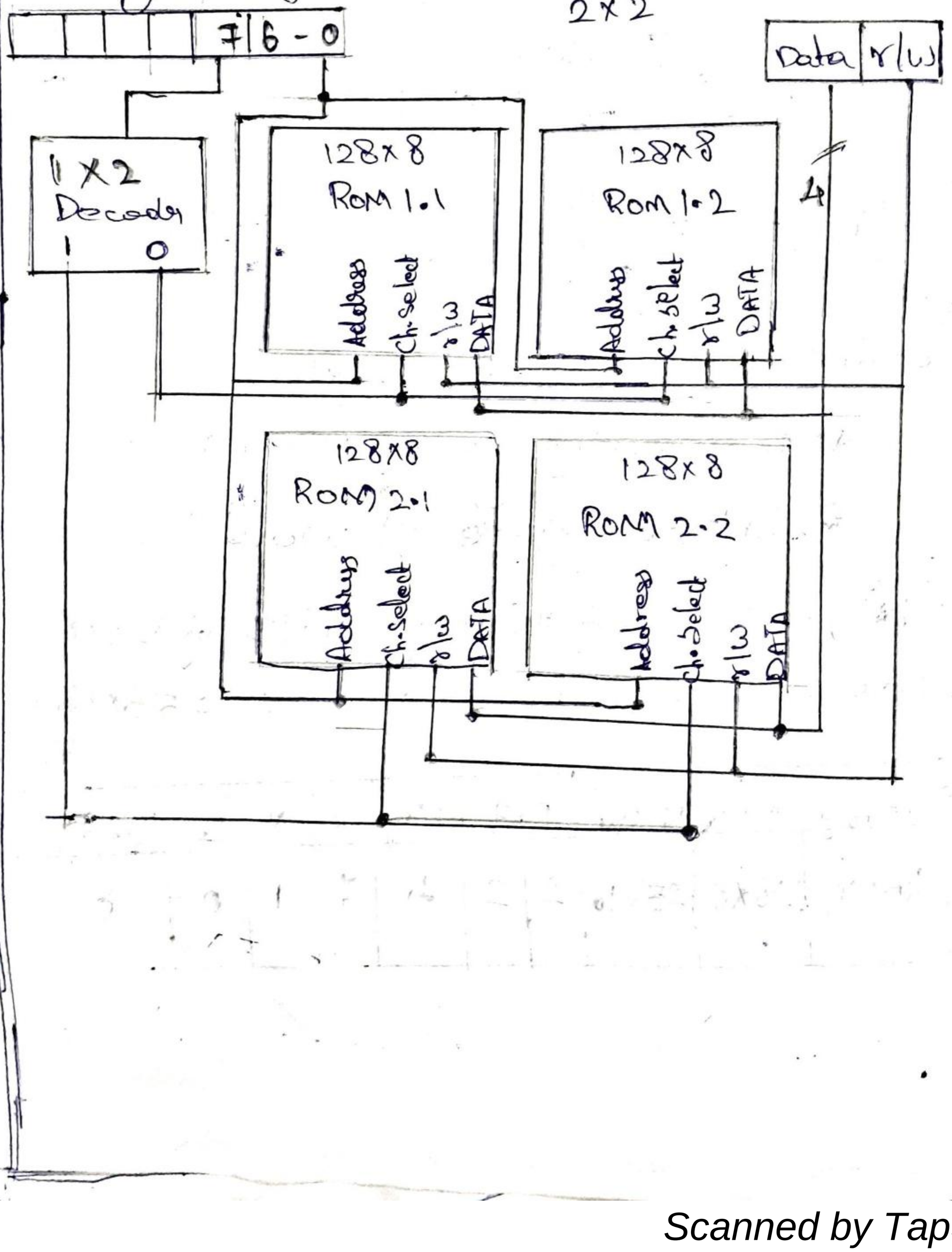
Sno	Memory	N×W	N'×W'	P	Q	P*Q	X	Y	Z	Total
	ROM	128×8	256×16	2	2	4	7	1	0	8

memory address mapping :-

Component	Hexadecimal add.		Address Bus										
	From	TO	10	9	8	7	6	5	4	3	2	1	0
ROM 1.1	0000	7F				0	x	x	x	x	x	x	x
ROM 1.2	0000	7F				0	x	x	x	x	x	x	x
ROM 2.1	80	FF				1	x	x	x	x	x	x	x
ROM 2.2	80	FF				1	x	x	x	x	x	x	x

Memory Design

matrix Expression
2 x 2



5) A computer employs RAM chips of 128*8 and ROM chips of 512*8. The computer system needs 265 bytes of RAM, 1024*16 of ROM. A memory mapped I/O configuration is used. The two higher order bits of the address bus are assigned 00 for RAM, 01 for ROM.

a) Compute the total number of decoders needed for the above Memory system design.

b) Given the memory-address map for each of the memory chips.

c) Show the chip layout for the above memory design.

Soln

RAM

Available memory for RAM N x W = 128 x 8

Required memory N' x W' = 256 x 8

ROM

Available memory N x W = 512 x 8

Required memory N' x W' = 1024 x 16

memory address mapping:- (B)

S.No	Memory	N x W	N' x W'	P	Q	P+Q	X	Y	Z	Total
1	RAM	128x8	256x8	2	1	2	7	1	2	10
2	Rom	512x8	1024x16	2	2	4	9	1	2	12
3	Interface	256x8	512x8	2	1	2	8	1	2	11

(B)

Component	Hexadecimal Address		Address Bus													
	From	To	15-12	11	10	9	8	7	6	5	4	3	2	1	0
RAM1	0000	007F		0	0	0			x	x	x	x	x	x	x
RAM2	0200	027F		0	0	1			x	x	x	x	x	x	x
ROM 1.1	0400	05FF		0	1	0	x	x	x	x	x	x	x	x	x
ROM 1.2	0400	05FF		0	1	0	x	x	x	x	x	x	x	x	x
Rom 2.1	0600	07FF		0	1	1	x	x	x	x	x	x	x	x	x
ROM 2.2	0600	07FF		0	1	1	x	x	x	x	x	x	x	x	x
Interface 1	0800	08FF		1	0	0		x	x	x	x	x	x	x	x
Interface 2	0A00	0AFF		1	0	1		x	x	x	x	x	x	x	x