Gate Questions on Multiplexers (MUX)

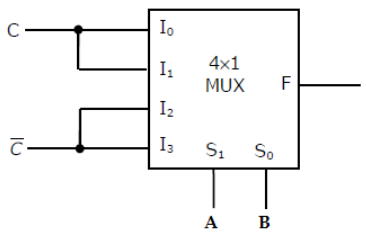
October 20, 2017 2 comments

Gate Questions on Multiplexers (MUX)

1992

Question 1: GATE | GATE-EC-1992

The logic realized by the circuit shown in figure is -



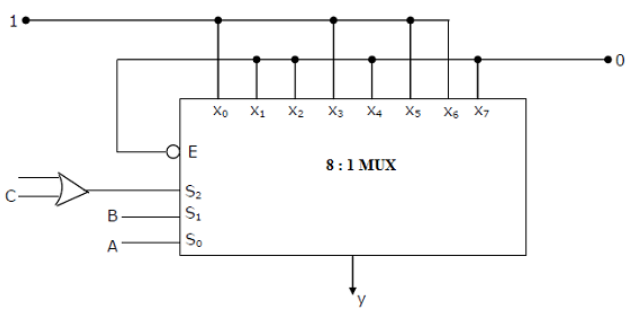
(A) F = A ⊙ C
(B) F = A ⊗ C
(C) F = B ⊙ C
(D) F = B ⊗ C

Answer: (B)
Explanation:

2001

Question 1: GATE | GATE-EC-2001

In the TTL circuit in the figure, S_2 to S_0 are select lines and X_7 and X_0 are input lines. S_0 and X_0 are LSBs. The output Y is -



(A) indeterminate
(B) $\overline{A \otimes B}$
(C) $\overline{A \otimes B}$
(D) $\overline{C}.\overline{(A \otimes B)} + C.(A \otimes B)$

Answer: (D)
Explanation:

2003

Question 1: GATE | GATE-EC-2003 (ISRO-EC-2017)

Without any additional circuitry, an 8:1 MUX can be used to obtain -

(A) some but not all Boolean functions of 3 variables
(B) all function of 3 variables but none of 4 variables
(C) all functions of 3 variables and some but not all of 4 variables
(D) all functions of 4 variables

Answer: (C)
Explanation:

2004

Question 1: GATE | GATE-EC-2004

The minimum number of 2 to 1 multiplexers required to realize a 4 to 1 mutliplexer is -

(A) 1
(B) 2

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(C) 3
(D) 4

Answer: (C)

Explanation:

Question 2: GATE | GATE-CS-2004

Consider a multiplexer with X and Y as data inputs and Z as control input. Z = 0 selects input X, and Z = 1 selects input Y. What are the connections required to realize the 2-variable Boolean function f = T + R, without using any additional hardware ?

(A) R to X, 1 to Y, T to Z
(B) T to X, R to Y, T to Z
(C) T to X, R to Y, 0 to Z
(D) R to X, 0 to Y, T to Z

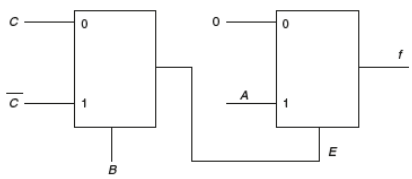
Answer: (A)

Explanation:

2005

Question 1: GATE | GATE-EC-2005

The Boolean function f implemented in figure using two input multiplexers is -



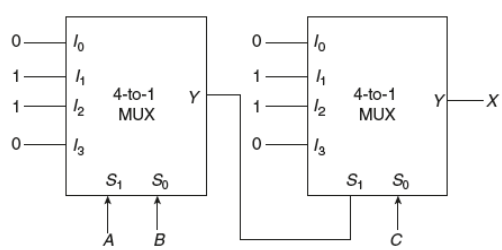
(A) $A\bar{B}C + AB\bar{C}$
(B) $ABC + A\bar{B}\bar{C}$
(C) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$
(D) $\bar{A}\bar{B}C + \bar{A}B\bar{C}$

Answer: (A)
Explanation:

2007

Question 1: GATE | GATE-EC-2007

In the following circuit, X is given by -



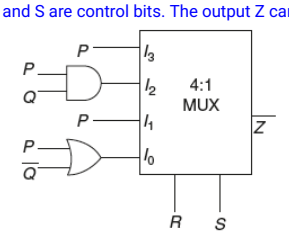
(A) $X = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$
(B) $X = \bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$
(C) $X = AB + BC + AC$
(D) $X = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

Answer: (A)
Explanation:

2008

Question 1: GATE | GATE-EC-2008

For the circuit shown in the following figure I_0-I_3 are inputs to the 4:1 multiplexer R(MSB) and S are control bits. The output Z can be represented by -



(A) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$
(B) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
(C) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
(D) $PQ\bar{R} + PQR\bar{S} + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$

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Answer: (A)
Explanation:

2009

Question 1: GATE | GATE-EC-2009

What are the minimum number of 2 to 1 multiplexers required to generate a 2-input AND gate and a 2-input Ex-OR gate?

(A) 1 and 2
(B) 1 and 3
(C) 1 and 1
(D) 2 and 2

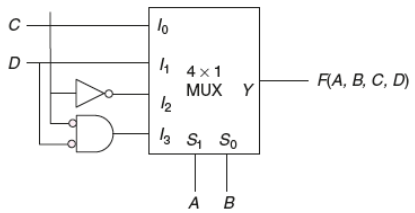
Answer: (A)

Explanation:

2010

Question 1: GATE | GATE-EC-2010

The Boolean function realized by the logic circuit shown is -



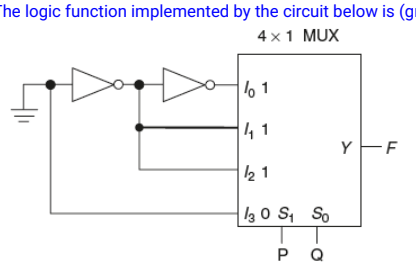
(A) F=Σm(0,1,3,5,9,10,14)
(B) F=Σm(2,3,5,7,8,12,13)
(C) F=Σm(1,2,4,5,11,14,15)
(D) F=Σm(2,3,5,7,8,9,12)

Answer: (D)
Explanation:

2011

Question 1: GATE | GATE-EC-2011

The logic function implemented by the circuit below is (ground implies logic 0)-



(A) F = AND(P,Q)
(B) F = OR (P,Q)
(C) F = XNOR (P,Q)
(D) F = XOR (P,Q)

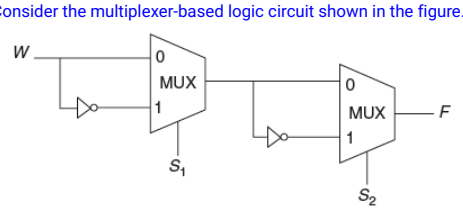
Answer: (D)

Explanation:

2014

Question 1: GATE | GATE-EC-2014

Consider the multiplexer-based logic circuit shown in the figure.



Which one of the following Boolean functions is realized by the circuit?

(A) F = W $\overline{S_1}$ $\overline{S_2}$
(B) F = $WS_1 + WS_2 + S_1S_2$
(C) F = $\overline{W} + S_1 + S_2$

Theory Format
The photonic nature of light
Direct and Indirect Band Gap
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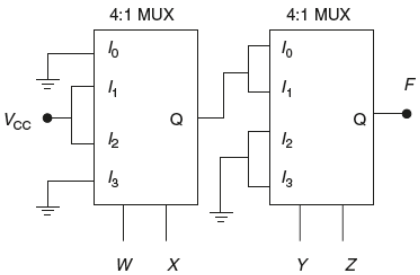
(D) F = W ⊕ S_1 ⊕ S_2

Answer: (D)

Explanation:

Question 2: GATE | GATE-EC-2014

In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by -



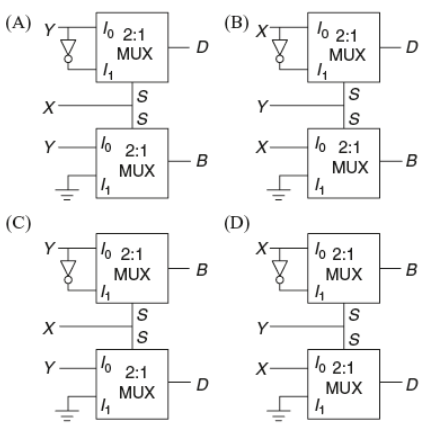
(A) F = W $\overline{X}$ + $\overline{W}$ X + $\overline{Y}$ $\overline{Z}$
(B) F = W $\overline{X}$ + $\overline{W}$ X + $\overline{Y}$ Z
(C) F = W $\overline{X}$ $\overline{Y}$ + $\overline{W}$ X $\overline{Y}$
(D) F = ($\overline{W}$ + $\overline{X}$) $\overline{Y}$ $\overline{Z}$

Answer: (C)

Explanation:

Question 3: GATE | GATE-EC-2014

If X and Y are inputs and the difference (D = X − Y) and the borrow (B) are the outputs, which one of the following diagrams implements a half subtractor?

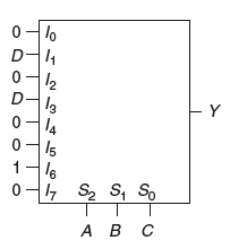


Answer: (A)

Explanation:

Question 4: GATE | GATE-EC-2014

An 8-to-1 multiplexer is used to implement a logical function Y, as shown in the figure. The output Y is given by -



(A) Y = A $\overline{B}$ C + A $\overline{C}$ D
(B) Y = A B $\overline{C}$ + A B D
(C) Y = A B $\overline{C}$ + $\overline{A}$ C D
(D) Y = $\overline{A}$ $\overline{B}$ D + A $\overline{B}$ C

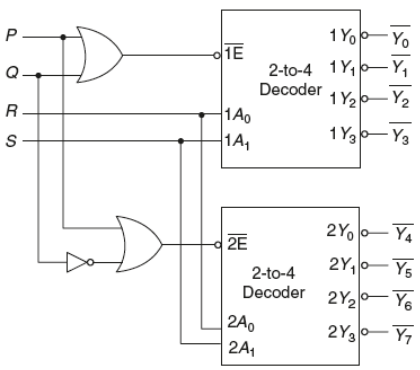
Answer: (C)

Explaination:

2015

Question 1: GATE | GATE-EC-2015

A 1-to-8 demultiplexer with data input D_{in}, address inputs S_0, S_1, S_2 (with S_0 as the LSB) and $\overline{Y_0}$ to $\overline{Y_7}$ as the eight demultiplexed outputs, is to be designed using two 2-to-4 decoders (with enable input $\overline{E}$ and address inputs A_0 and A_1) as shown in the figure. D_{in}, S_0, S_1 and S_2 are to be connected to P, Q, R, and S, but not necessarily in this order. The respective input connections to P, Q, R, and S terminals should be -



(A) S_2, D_{in}, S_0, S_1
(B) S_1, D_{in}, S_0, S_2
(C) D_{in}, S_0, S_1, S_2
(D) D_{in}, S_2, S_0, S_1

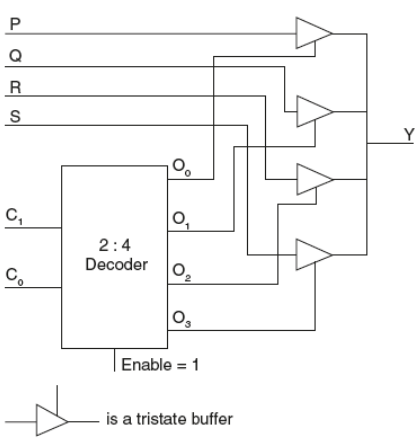
Answer: (D)

Explaination:

2016

Question 1: GATE | GATE-EC-2016

The functionality implemented by the circuit below is -



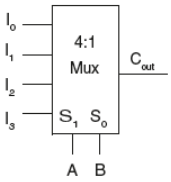
(A) 2 to 1 multiplexer
(B) 4 to 1 multiplexer
(C) 7 to 1 multiplexer
(D) 6 to 1 multiplexer

Answer: (B)

Explaination:

Question 2: GATE | GATE-EC-2016

A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry and C_{out} is the output carry. A and B are to be used as the select bits with A being the more significant select bit.



Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0, I_1, I_2, and I_3 so that the output is C_{out}?

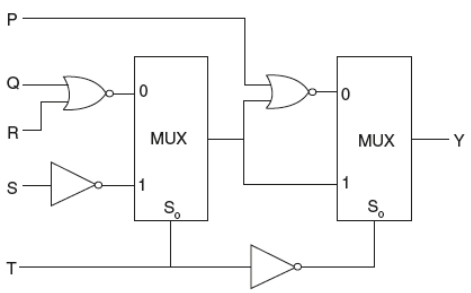
(A) $I_0 = 0$, $I_1 = C_{in}$, $I_2 = C_{in}$ and $I_3 = 1$
(B) $I_0 = 1$, $I_1 = C_{in}$, $I_2 = C_{in}$ and $I_3 = 1$
(C) $I_0 = C_{in}$, $I_1 = 0$, $I_2 = 1$ and $I_3 = C_{in}$
(D) $I_0 = 0$, $I_1 = C_{in}$, $I_2 = 1$ and $I_3 = C_{in}$

Answer: (A)

Explaination:

Question 3: GATE | GATE-EC-2016

For the circuit shown in the figure, the delays of NOR gates, multiplexers and inverters are 2ns, 1.5ns and 1ns respectively. If all the inputs P, Q, R, S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.



Answer: 6 ns

Explaination:

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Unknown February 4, 2019 at 9:30 AM
Its very good .Please provide the explanation which helps us to check wheather our analization is true are false
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Sams February 10, 2019 at 3:53 AM
thank you for appreciating our work. We are working on it to provide the explanation and theory, so that you can easily crack the examination.

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