Low-Power High-Speed Sense-Amplifier

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INTRODUCTION

- A sense amplifier is a circuit that is used to amplify and detect small signals in electronic systems.
- Single-ended communications set ups are meant to be used only for short runs or to provide communication between devices on the same Printed Circuit Board (PCB).
- With the employment of a new sense-amplifier stage as well as a new single-ended latch stage, the power and delay of the flipflop is greatly reduced.
- The proposed SAFF can provide low voltage operation by adopting MTCMOS (Multi-threshold CMOS) optimization.

CIRCUIT DAIGRAM OF SA AND PROPOSED LATCH TYPE SENSE AMPLIFIER

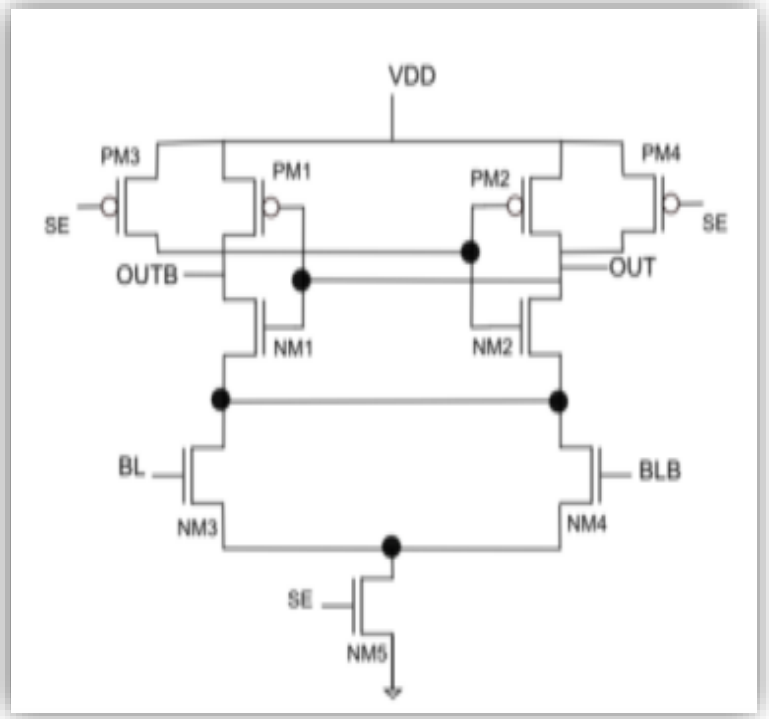

Figure 1

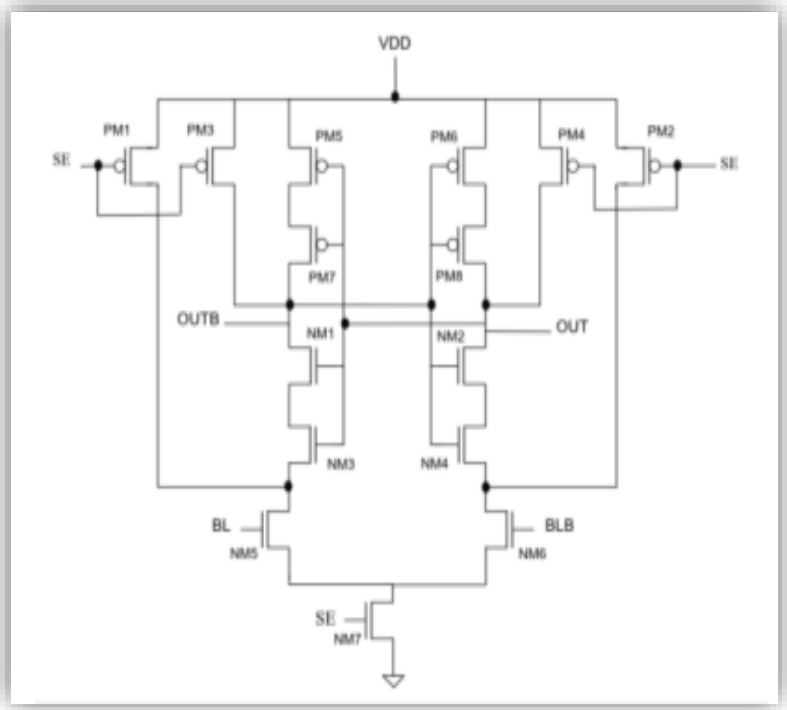

Figure 2

REASON FOR PURSUING :

- Energy Efficiency - Low-power sense amplifiers are essential for applications where energy efficiency is a critical concern, such as battery-powered devices, IoT (Internet of Things) devices, and portable electronics.
- Mobile Devices - In mobile devices like smartphones and tablets, where power constraints are significant, low-power sense amplifiers contribute to extended battery life.
- Memory Access Time - High-speed sense amplifiers contribute to minimizing latency in memory access, which is essential for various computing tasks.

Role of Sense Amplifier:

- Sense amplifier is a crucial component in modern computer memory chips.
- It is part of the read circuitry responsible for sensing and amplifying low-power signals from a bitline representing data bits stored in memory cells.
- Its primary function is to amplify the small voltage swings to recognizable logic levels for proper interpretation of data by external logic.

Placement and Quantity:

- Each column of memory cells typically contains one sense amplifier.
- Modern memory chips may have hundreds or thousands of identical sense amplifiers.

Design Overview:

- Sense amplifier is designed to read by sensing a differential voltage on the bitlines.
- It reads the value without requiring rail-to-rail voltage swing on BL/BLB (bitlines).
- The sense amplifier consists of cross-coupled inverters.
- The junctions between NMOS and PMOS transistors are connected to the drain terminals of pull-up PMOS transistors.
- The gates of these pull-up PMOS transistors are controlled by an enable signal.
- The source terminals of NMOS transistors within the inverters are connected to the drain terminals of NMOS transistors, with their gates connected to the two bitlines (BL and BLB).
- These NMOS transistors have their sources connected to the drain of an NMOS transistor, with the gate controlled by the enable signal.

PROPOSED SYSTEM:

Introduction to Latch Type Sense Amplifier:

- Current Controlled Latched Sense Amplifier (CC-Latch Sense Amplifier) is a type of voltage sense amplifier commonly used in integrated circuits for reading and amplifying signals from memory cells, such as in SRAM.

Design Overview:

- This amplifier utilizes a latch-based design similar to traditional latch-based amplifiers.
- However, the bitlines are attached to the gates of transistors N3 and N4, resulting in a high impedance at the input and decoupling of the bitlines from the output.
- The two inverters are constructed from MOSFET pairs NM1, PM1, NM2, and PM2.

Operation:

- When the amplifier is off (SE signal at logic low), reset transistors PM3 and PM4 are turned on, clearing the previous latched value and holding the latch at its metastable point.
- The bitline inputs are connected to the gates of MOSFETs NM3 and NM4.
- When the sense amplifier is enabled (SE signal at logic high), reset transistors turn off, and current source NM5 turns on, causing an even current to flow through each half of the amplifier.
- Discharging of one bitline causes the gate voltage to drop, reducing the current through that side of the amplifier and causing the voltage to rise. This triggers the amplifier to latch, stopping the static flow of current and displaying a valid value at the output.

Circuit Diagram:

- Figure 1 depicts the circuit diagram of a latch type sense amplifier.

Signal Sensing:

- When the sensing signal SE is at logic low (GND), the output node is isolated to GND, and precharge transistors PM2 and PM4 charge the output nodes to VDD.
- When SE signal is enabled (logical high, VDD), NM5 is turned on, pulling the node down to GND level. Under this condition, NM3 and NM4 work as a common-source differential amplifier.

Designs, waveforms and output screenshots

- Schematic of the proposed Sense Amplifier is shown.
- Transient response of the proposed Sense Amplifier.
- Layout of the proposed Sense Amplifier.

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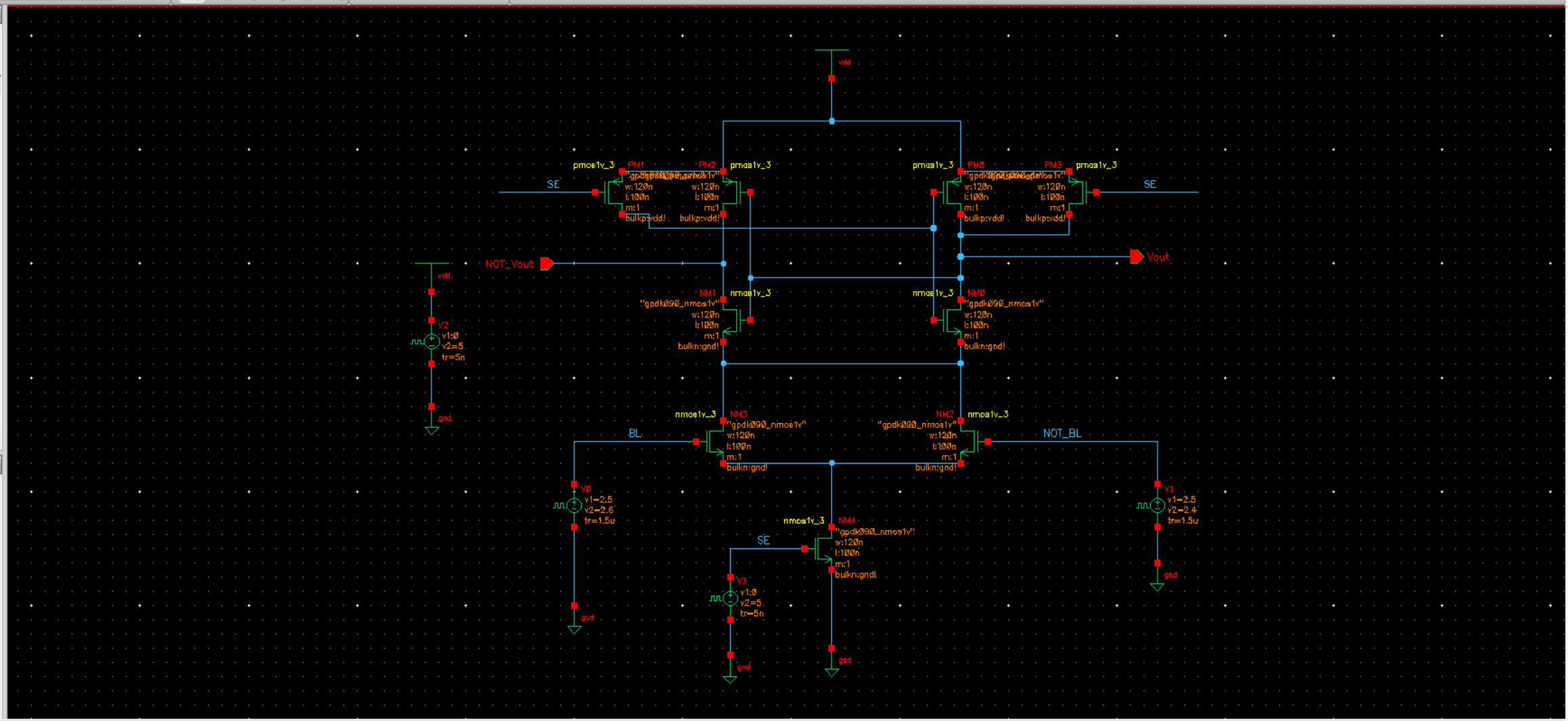

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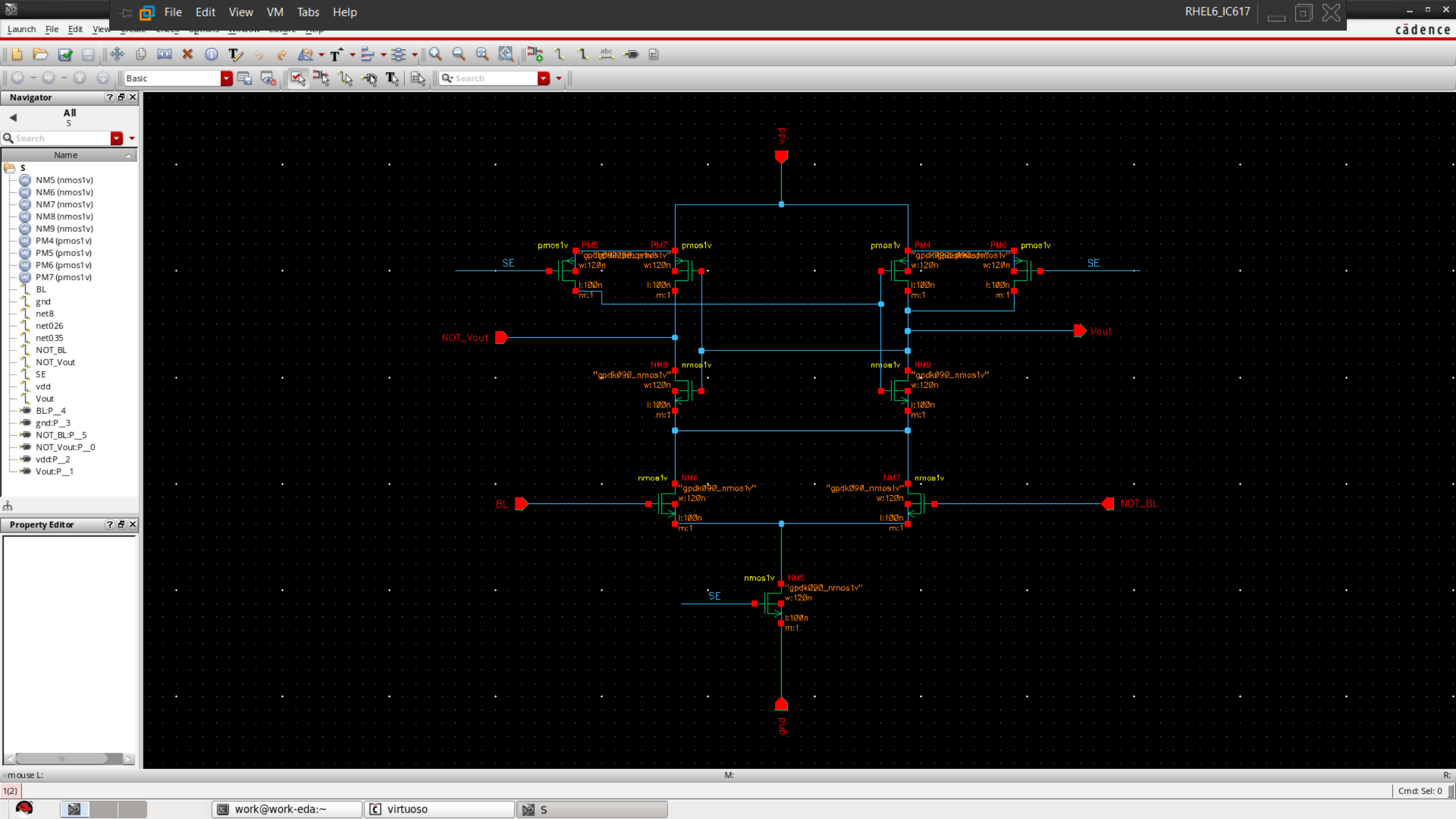
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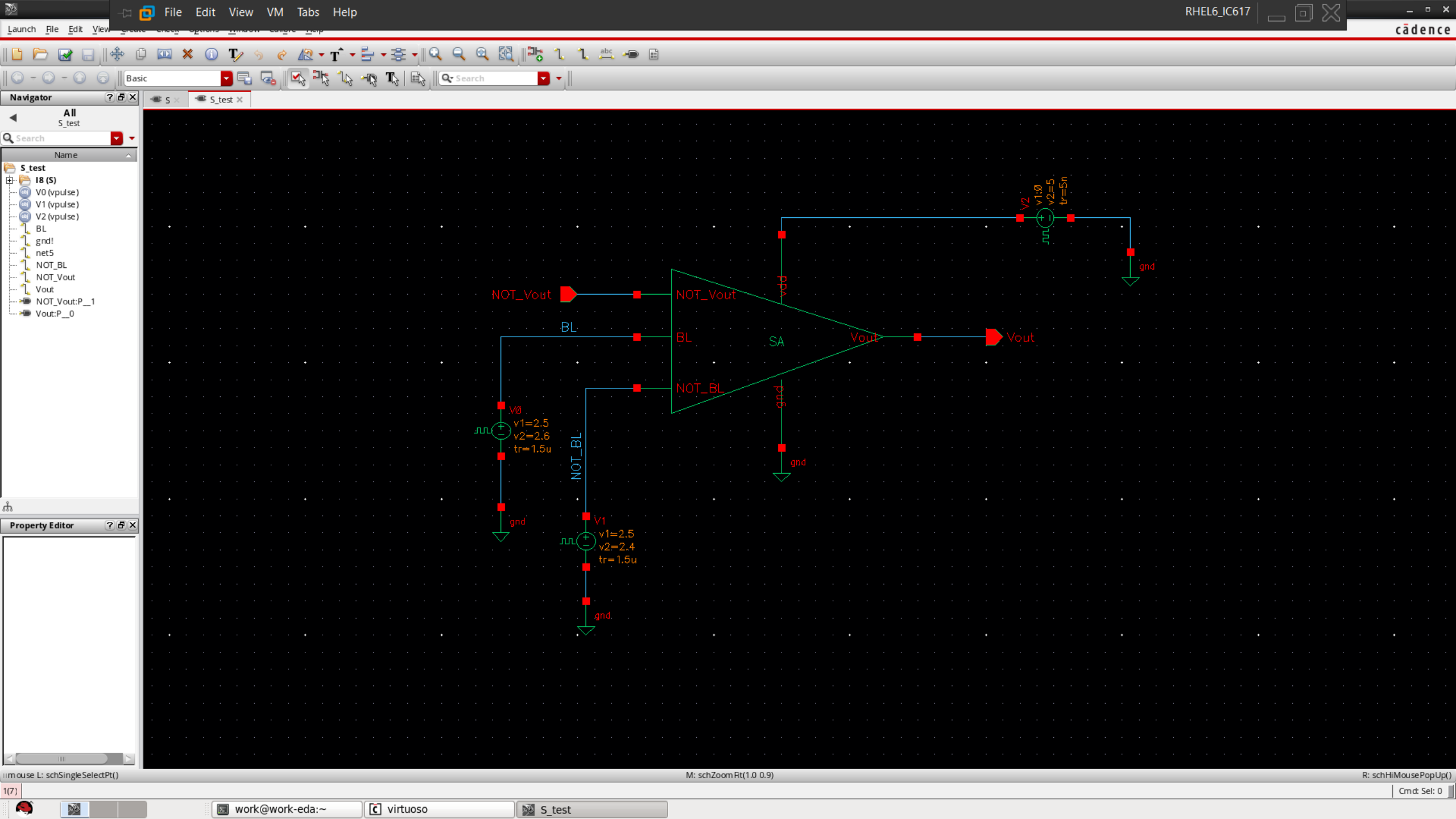
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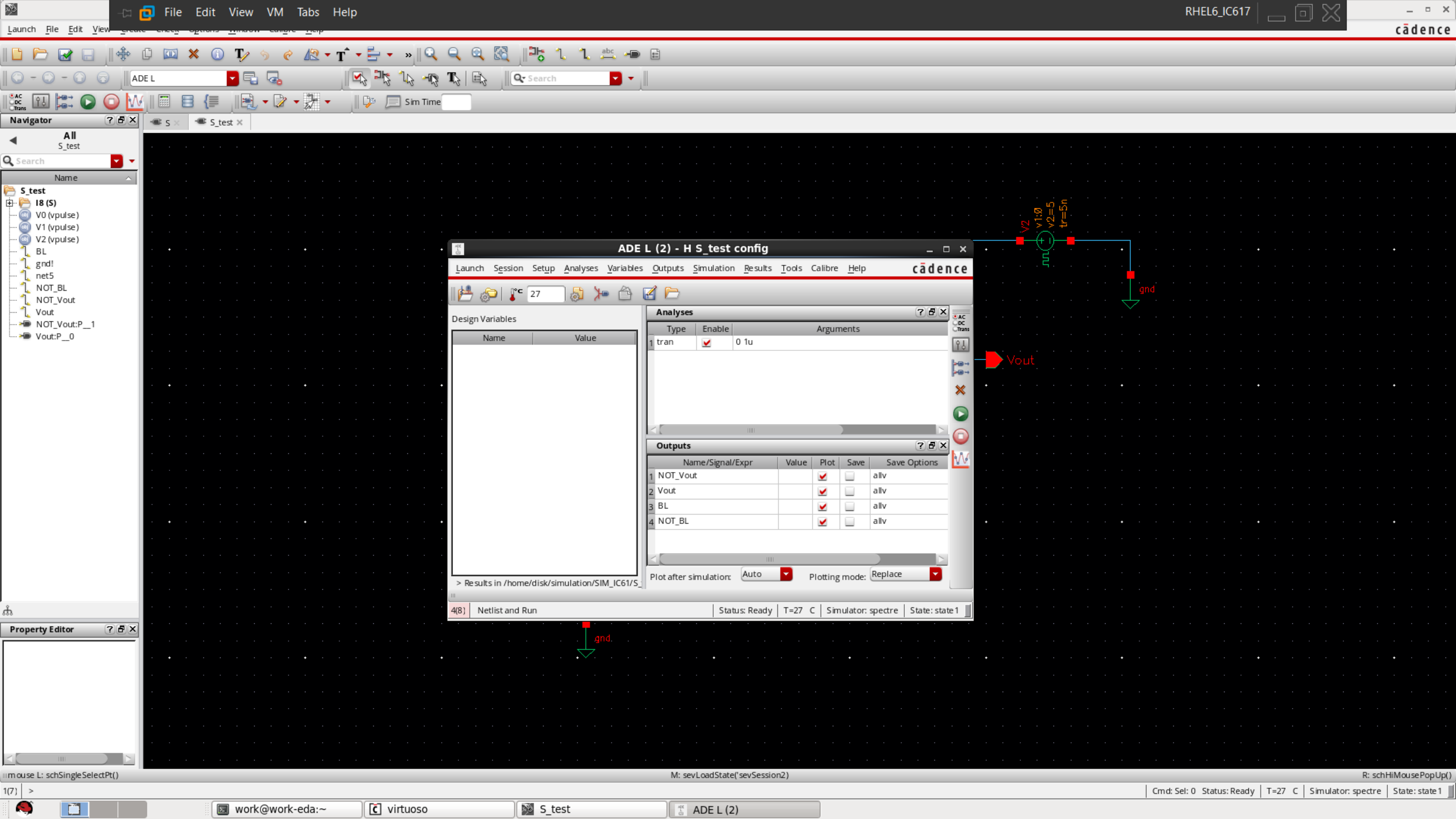
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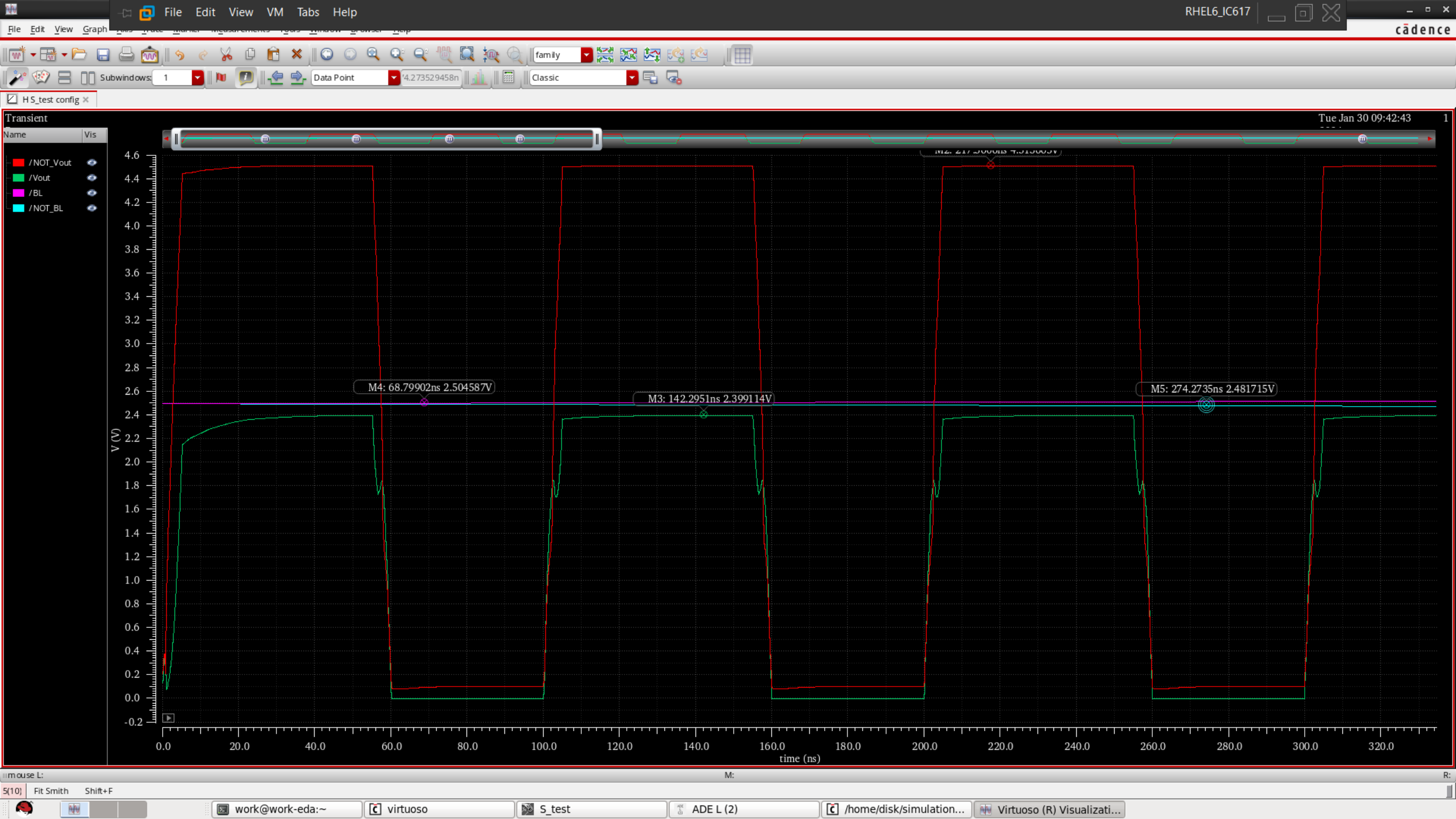
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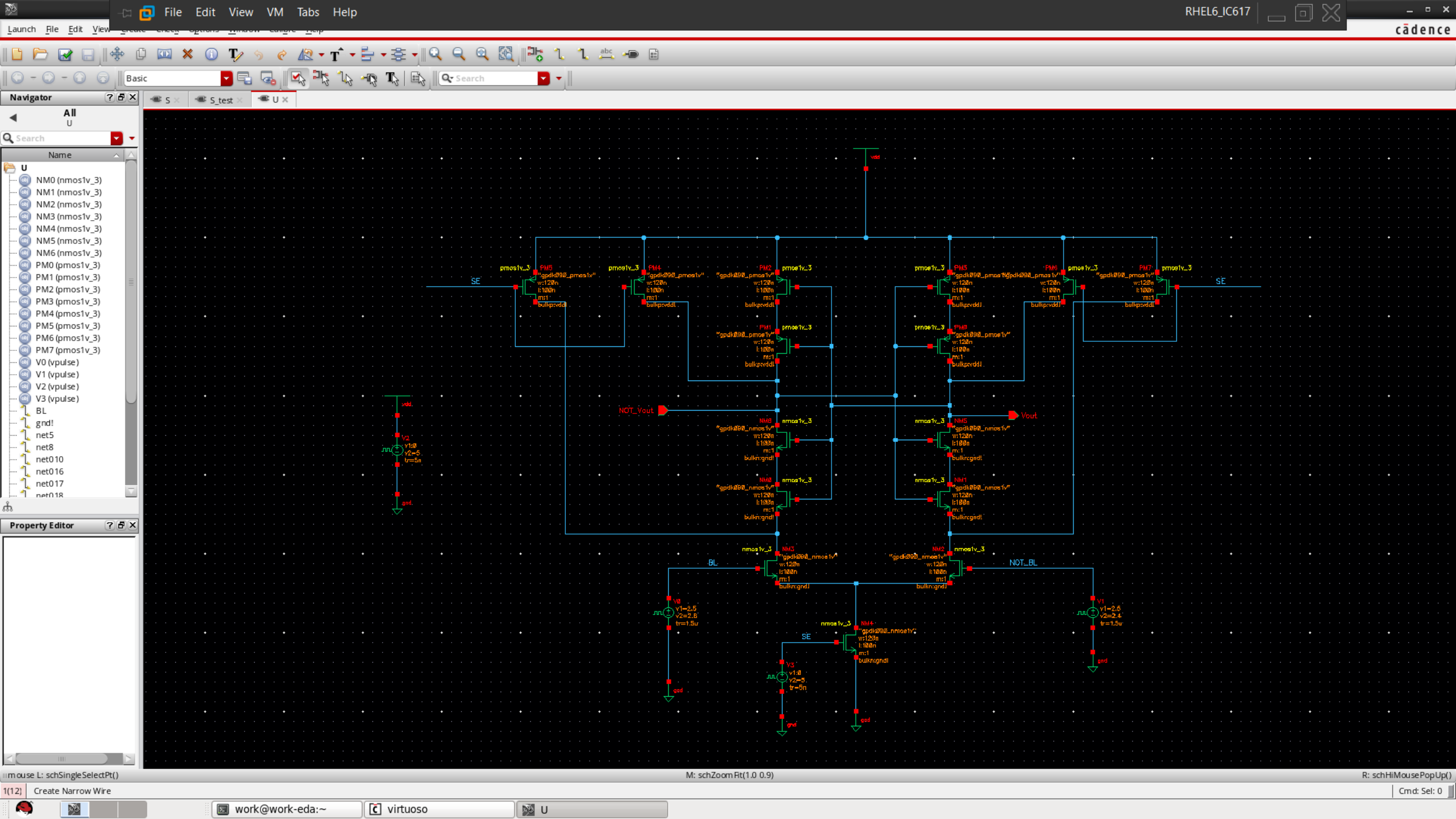
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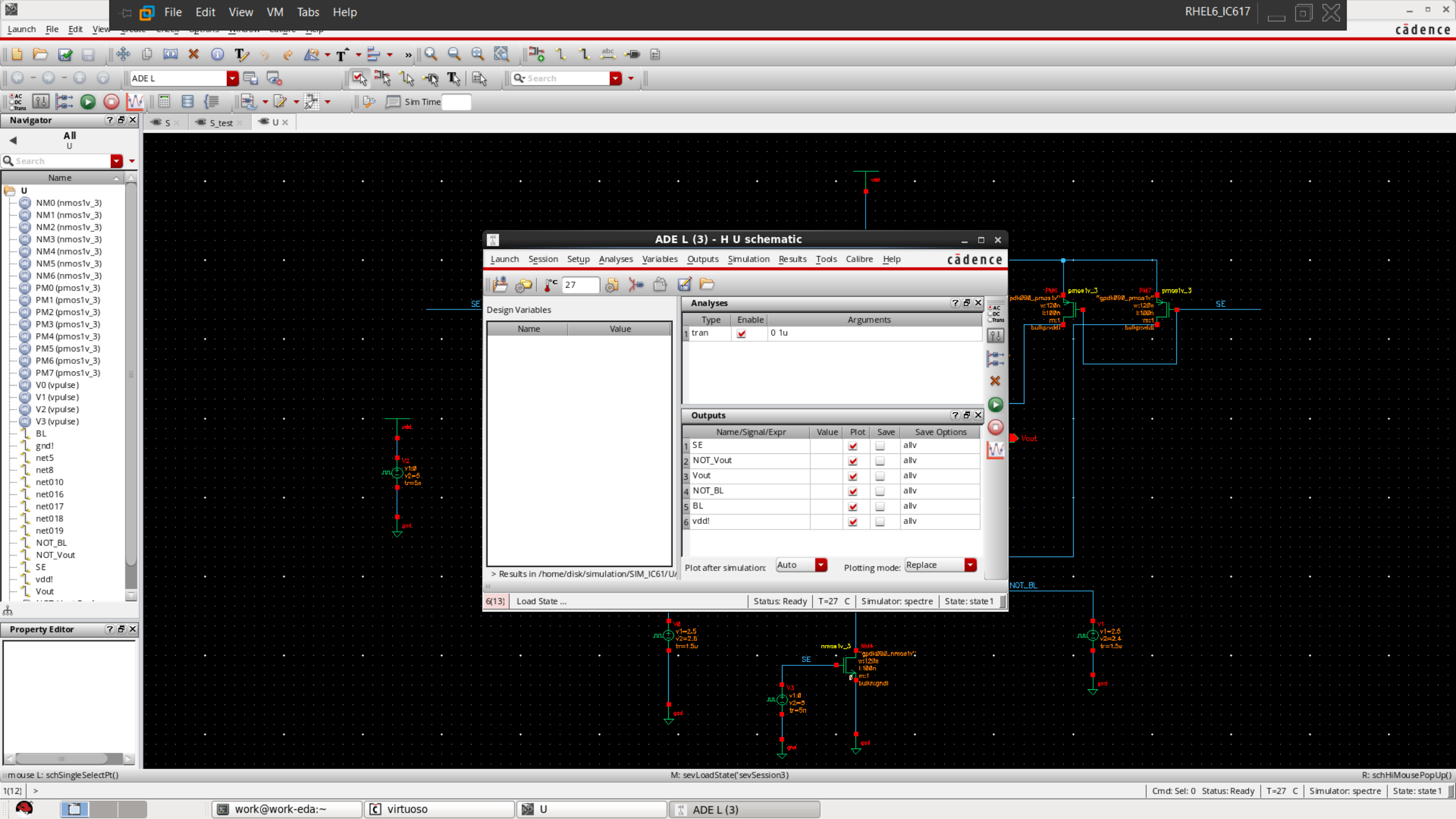
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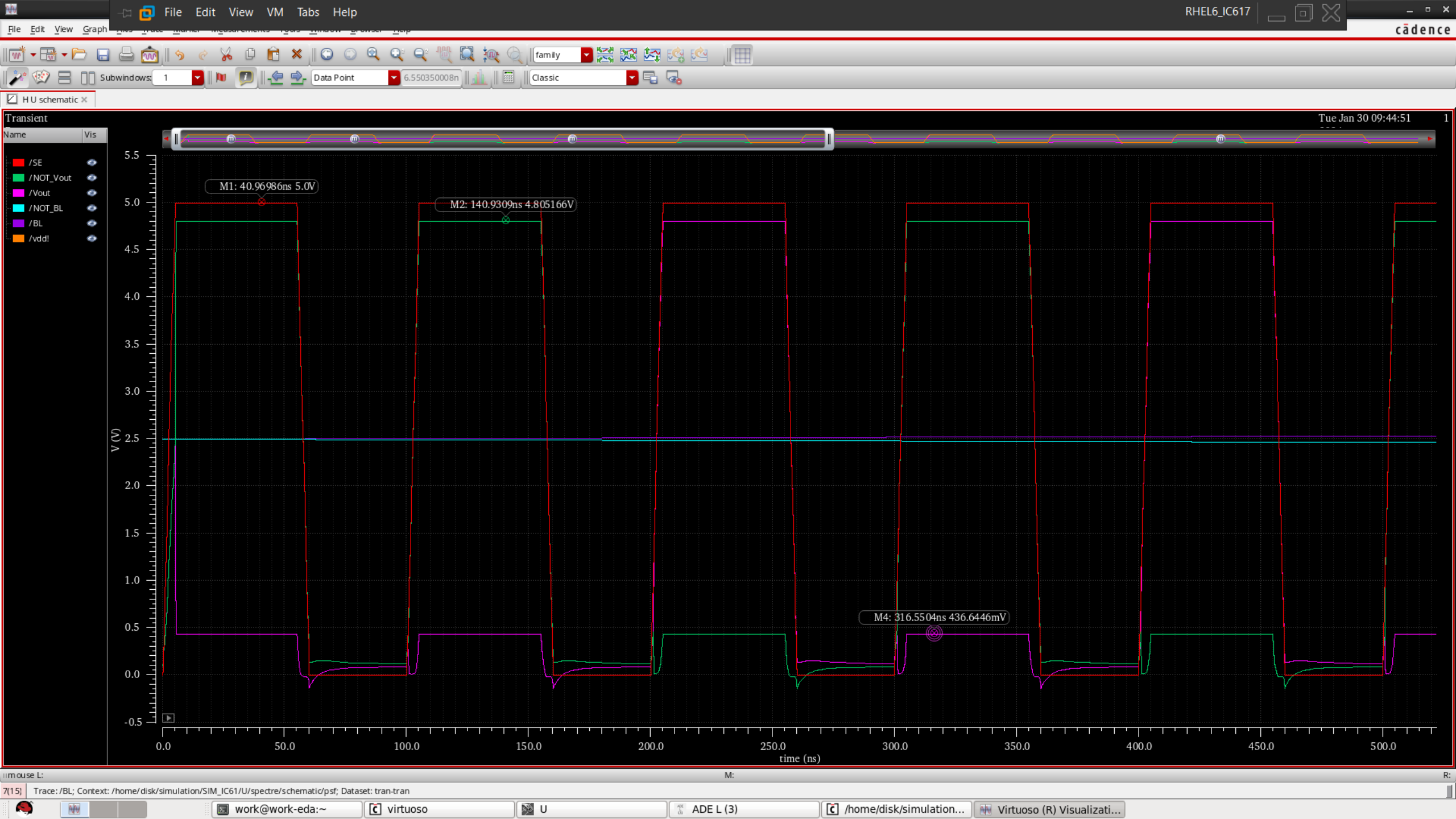
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POWER AND DELAY COMPARISON OF EXISTING AND PROPOSED SA

	Latch type SA	Proposed SA
Technology used	180nm	180nm
Supply voltage	1V	910mV
Static power	591nW	46.9pW
Dynamic power	98nW	180nW
Total power	689nW	180nW
Delay	7nS	4.5nS

CONCLUSION - The emergence of VLSI technology has led to the miniaturization of memory devices, significantly reducing their footprint and enhancing performance. However, this advancement poses challenges for memory designers, particularly in the realm of sense amplifiers. As technology continues to shrink, the demand for more efficient and faster sense amplifiers intensifies, while simultaneously grappling with increased power consumption.

To combat this, innovative techniques are being employed to refine conventional latch-type sense amplifiers. In a recent endeavor, a new latch-type sense amplifier design has been introduced, integrating stacking and supply voltage scaling. This novel approach demonstrates superior results, offering reduced power consumption and latency compared to traditional designs. With a static power of 46.2pW and dynamic power of 180nW, totaling 180nW, the proposed design showcases its potential as a peripheral circuit in memory applications, effectively addressing the challenges associated with technology shrinkage.

References:

1) T.Vaishubiah, M.Durgadevi, Dr.K.Ramasamy ,“REDUCTION OF COUPLING SIGNALS USING LATCH TYPE SENSE AMPLIFIER IN SRAM,” International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. 4, Special Issue 23, December 2017.
2) International Journal for Research in Engineering Application & Management (IJREAM) - ISSN : 2454-9150

   Vol-05, Issue-03, June 2019

TOOL OF IMPLEMENTATION : Cadence Virtuoso Tool

- It is used to verify the functionality and performance of the designed sense amplifier.
- Analysis of simulation results to ensure the amplifier meets specified criteria (speed, power, accuracy).
- Used to generate the Verilog code and the generated code is handled by the fabrication team to manufacture the chip.
- Cadence virtuoso is a EDA (Electronic Design Automation) tool for learning about IC design/analysis and PCB design/analysis. Virtuoso is majorly used for custom design and analysis of circuits based on MOS technologies, especially in the CMOS.