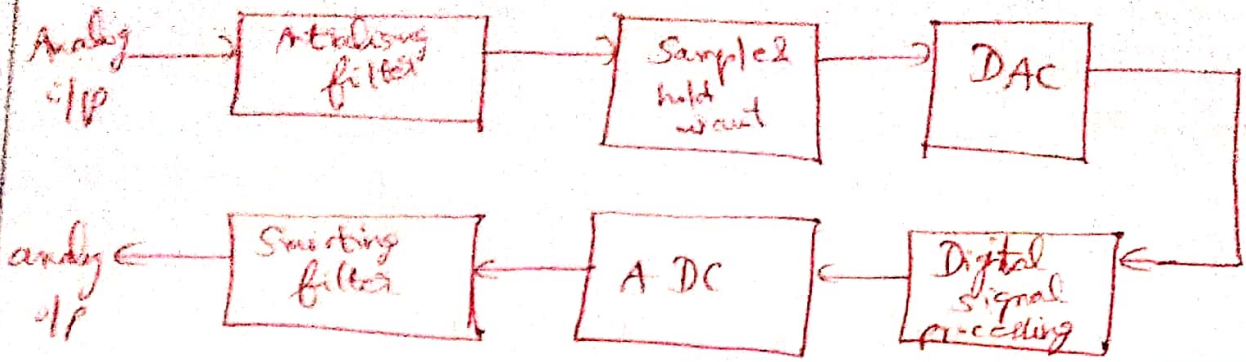
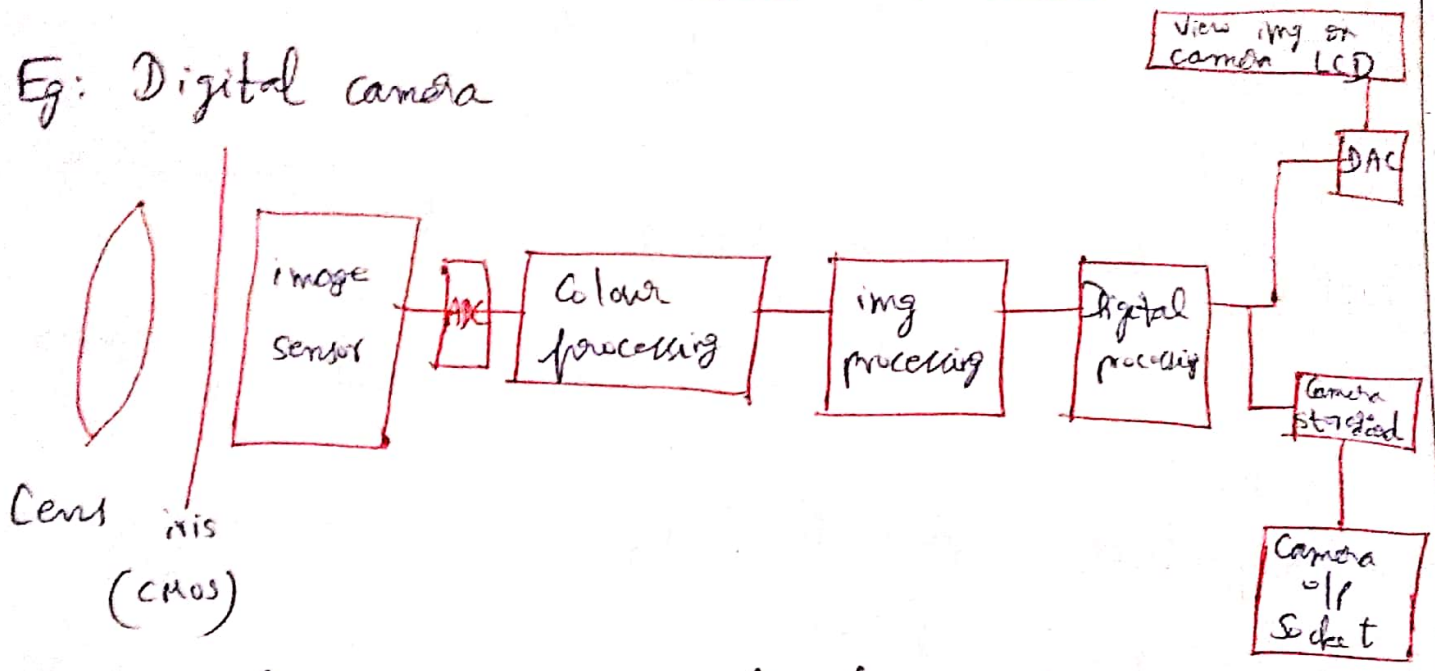
→ A/D and D/A conversion appⁿ:



Eg: Digital camera



→ Lens → focused on img to be capture.

→ Light on lens → image sensor → convert light → electrical signals (analog) → digital (ADC).

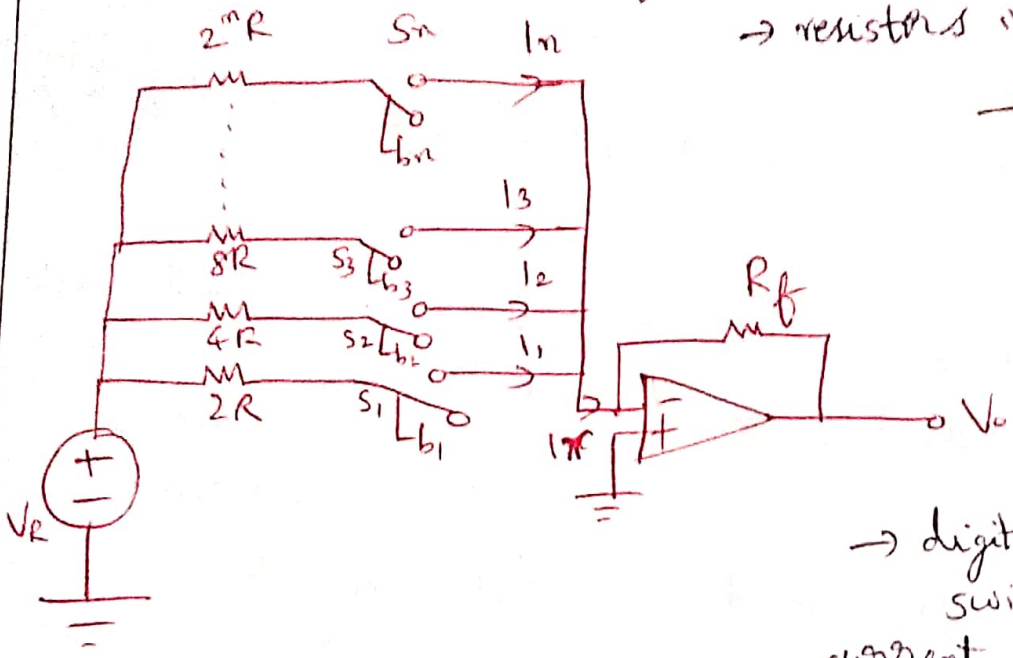
→ After digital processing → digital data to analog & light signal to view img on camera LCD.

↳ Analog → digital. once digital processing ✓ ⇒ convert dig. back to analog.

Types of DAC (D/A Converters)

- n-bit binary weighted resistor
- Inverted R/2R ladder

n-bit binary weighted Resistor :



→ resistors in parallel.

→ op-amp as inverting voltage summer

→ digital logic = 1 → switch is open → current flows.

→ digital logic = 0 → switch closed → current ✗

→ Assuming $+V_{cc} = -V_{EE} = 0$ (gnd), $I_{b1} = I_{b2} = 0$,

$$I_n = \left(\frac{V_R}{2^n R}\right) \times b_n$$ → current in a branch.

$$I_1 = \frac{V_R}{2R} \times b_1, \quad I_2 = \frac{V_R}{4R} \times b_2, \quad \ldots \quad I_n = \frac{V_R}{2^n R} \times b_n$$

$$I_{net} = I_1 + I_2 + \ldots + I_n \quad \text{(KCL)}$$

$$I_n = \frac{V_R}{2R} \times b_1 + \frac{V_R}{4R} \times b_2 + \frac{V_R}{8R} \times b_3 + \ldots + \frac{V_R}{2^n R} \times b_n$$

$I_n = \frac{-V_o}{R_f}$ (inverting)

$\frac{-V_o}{R_f} = \frac{V_R}{R}(b_1 \times 2^{-1} + b_2 \times 2^{-2} + b_3 \times 2^{-3} + \dots + b_n \times 2^{-n})$

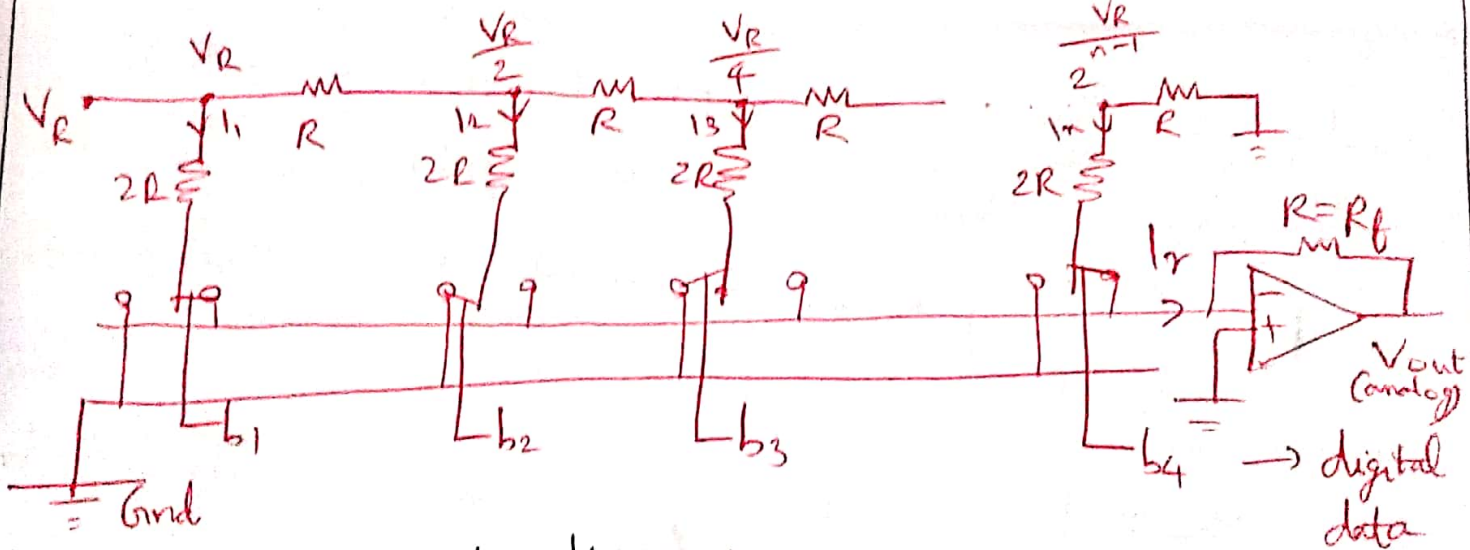
$\therefore V_o = \frac{-V_R}{R}(R_f)(b_1 \times 2^{-1} + b_2 \times 2^{-2} + b_3 \times 2^{-3} + \dots + b_n \times 2^{-n})$

$R_f = R$

$\rightarrow \boxed{V_o = -V_R (b_1 \times 2^{-1} + b_2 \times 2^{-2} + b_3 \times 2^{-3} + \dots + b_n \times 2^{-n})}$

→ disadv:
- → Wide range of resistors → hard to construct circuit practically, calculations hard]
- → loading effect → switch → both sides.

Inverted R/2R ladder D/A convertor:



Assumptions → $I_{b_1} = I_{b_2} = 0$

→ $+V_{cc} = -V_{EE} = 0$ (grided)

Current in any branch → $I_n = \frac{V_R}{2R} \times b_n$

Only 2 resistor values → R and 2R are used.

$b_n = 0 \rightarrow$ no current as switch is open

$\hookrightarrow b_n = 1 \rightarrow$ current ✓ $\rightarrow$ switch closed.

op-amp as voltage summer (inverting)

KCL $\Rightarrow \quad I_R = \frac{-V_o}{R_f}$

$\Downarrow$

$I_R = I_1 + I_2 + I_3 + \ldots + I_n$

$I_1 = \frac{V_R}{2R} \times b_1, \quad I_2 = \frac{V_R}{\frac{2}{2R}} \times b_2 = \frac{V_R}{4R} \times b_2,$

$I_3 = \frac{V_R/4}{2R} \times b_3 = \frac{V_R}{8R} \times b_3, \quad I_n = \frac{V_R/2^{n-1}}{2R} = \frac{V_R}{2^n R}$

$\therefore \quad \frac{-V_o}{R_f} = \frac{V_R}{2R} \times b_1 + \frac{V_R}{4R} \times b_2 + \frac{V_R}{8R} \times b_3 + \ldots + \frac{V_R}{2^n R} b_n$

$V_o = \frac{-V_R}{R}(R_f)\left(b_1 \times 2^{-1} + b_2 \times 2^{-2} + b_3 \times 2^{-3} + \ldots + b_n \times 2^{-n} \right)$

$R_f = R$

$\Rightarrow \boxed{V_o = -V_R \left(b_1 \times 2^{-1} + b_2 \times 2^{-2} + \ldots + b_n \times 2^{-n} \right)}$

o/p voltage (analog)

Adv.:

→ Wide range of resistor values X needed.

→ Only 2 resistance values ⇒ easier to build.

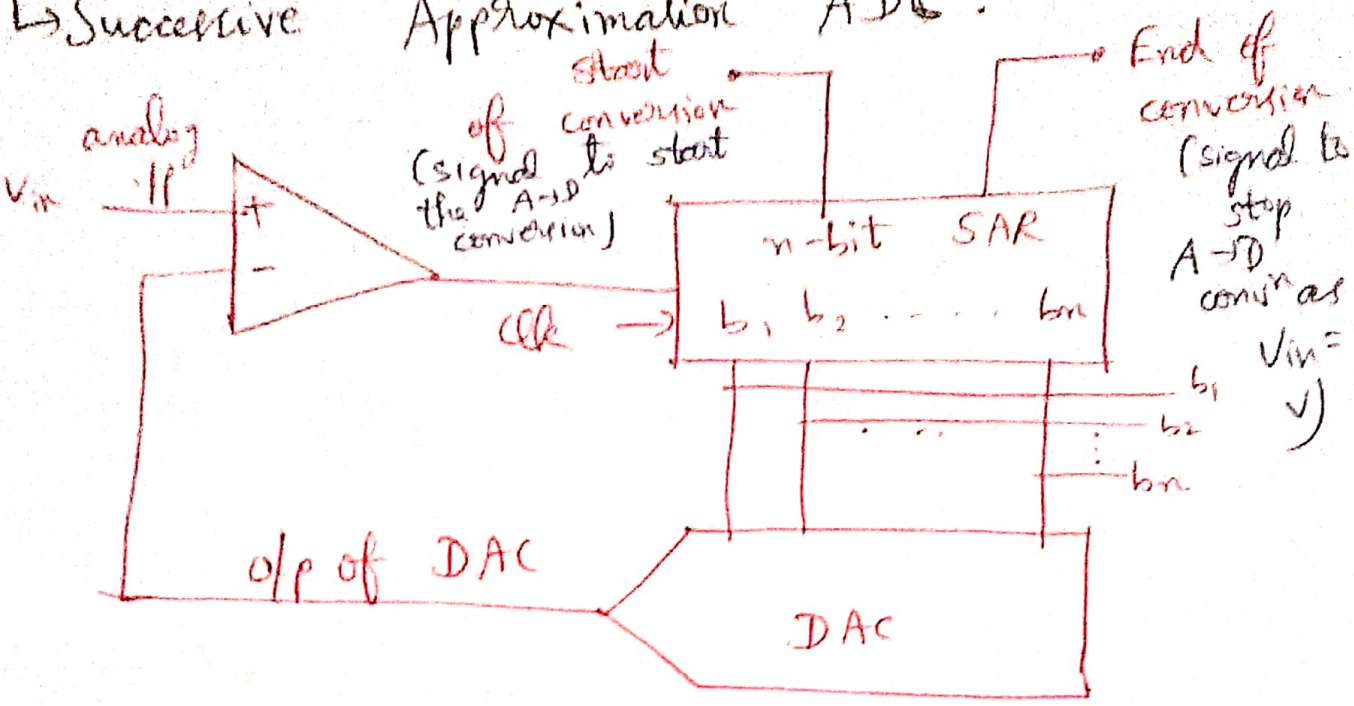
→ Node voltages remain unch. even when bin. i/ps change.

→ No. of bits ↑ ⇒ easier to expand by adding 1 more R & 2R set.

Types of ADCs.

(A/D Converter)

↳ Successive Approximation ADC:



⇒ SAR → Successive approximation register (Clock given) → this ADC.

→ Comparator

→ DAC

→ i/p to DAC such that o/p of DAC = $\pm \frac{1}{2}$ LSB

→ Eg: 3-bit SAR sets $b_1\ b_2\ b_3$ → DAC
1 0 0
to its corr. analog(V) → comparator compares V with V_{in}. $V_{in} > V$ → SAR sets $b_2 = 1$, $b_3 = 0$ or resets $b_2 = 0$, $b_3 = 1$. Technique successively for b_1, b_2 and corr. ~~analog~~ digital for V_{in} ✓.

→ n-bits ⇒ within n-clock cycles → conversion ✓.

→ Uses binary search technique.

→ $T_c = T(n+1)$ → T_c = time to convert, T = time period of clock, n = no. of bits.

Flash ADC (|| ^{el} Comparator Type ADC) :

→ fastest conversion → named so (flash).

→ simultaneously compare i/p signals with levels 1 LSB apart.

→ n-bit ⇒ $2^n - 1$ comparators are connected $||^{el}$ which compare i/p signal (V_A) simultaneously. ↓ connected to + of each comparator. (V)

→ $V_{REF} = 7V$. Voltage divider → divides the ref. voltage level → connected to −.

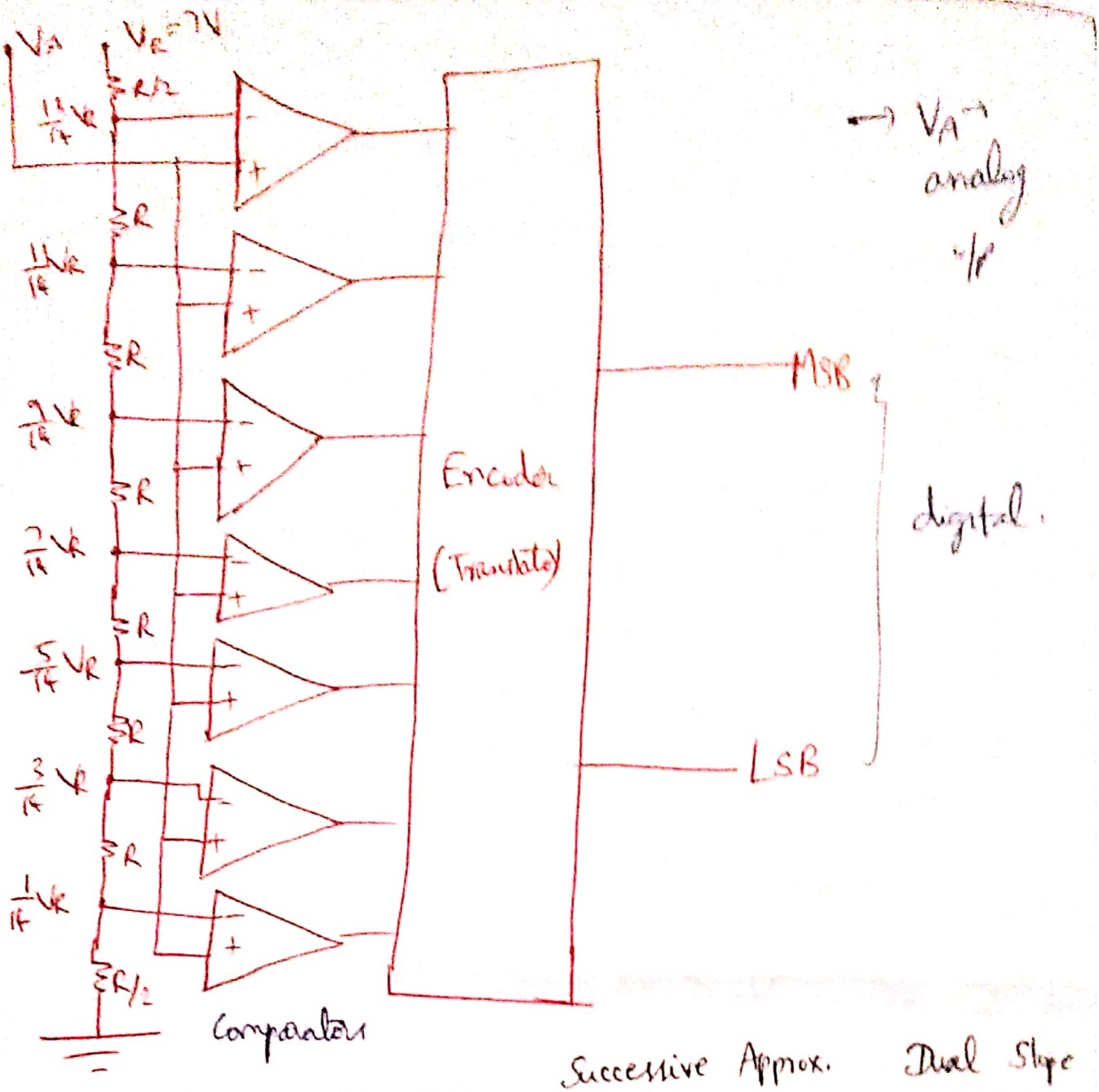
→ Quantisation error = $\pm \frac{1}{2}$ LSB.

→ Whenever $V > V_A$ → comparator o/p = 0 & off.

" $V \leq V_A$ → " " = 1

→ Code → converted to binary using encoder.

Scanned by CamScanner



Parameter	Flash ADC	Successive Approx. ADC	Dual Slope ADC.
Speed →	Fastest	Fast	Slow
Accuracy →	↓	Medium	↑
Cost →	↑	Medium	↓
Resolution →	Upto 2^8	Upto 2^{18}	~~Upto~~ $\geq 2^{16}$.
i/p hold time →	very ↓	depends on no of bits but ~~of~~ flash ADC.	↑
appⁿ's →	↑ speed, (1) digital storage oscilloscope, (2) Fibre optics	data acquisition	↑ accuracy, resolⁿ. Speed is not 1st priority.