Bus in Computer Architecture

INTRODUCTION

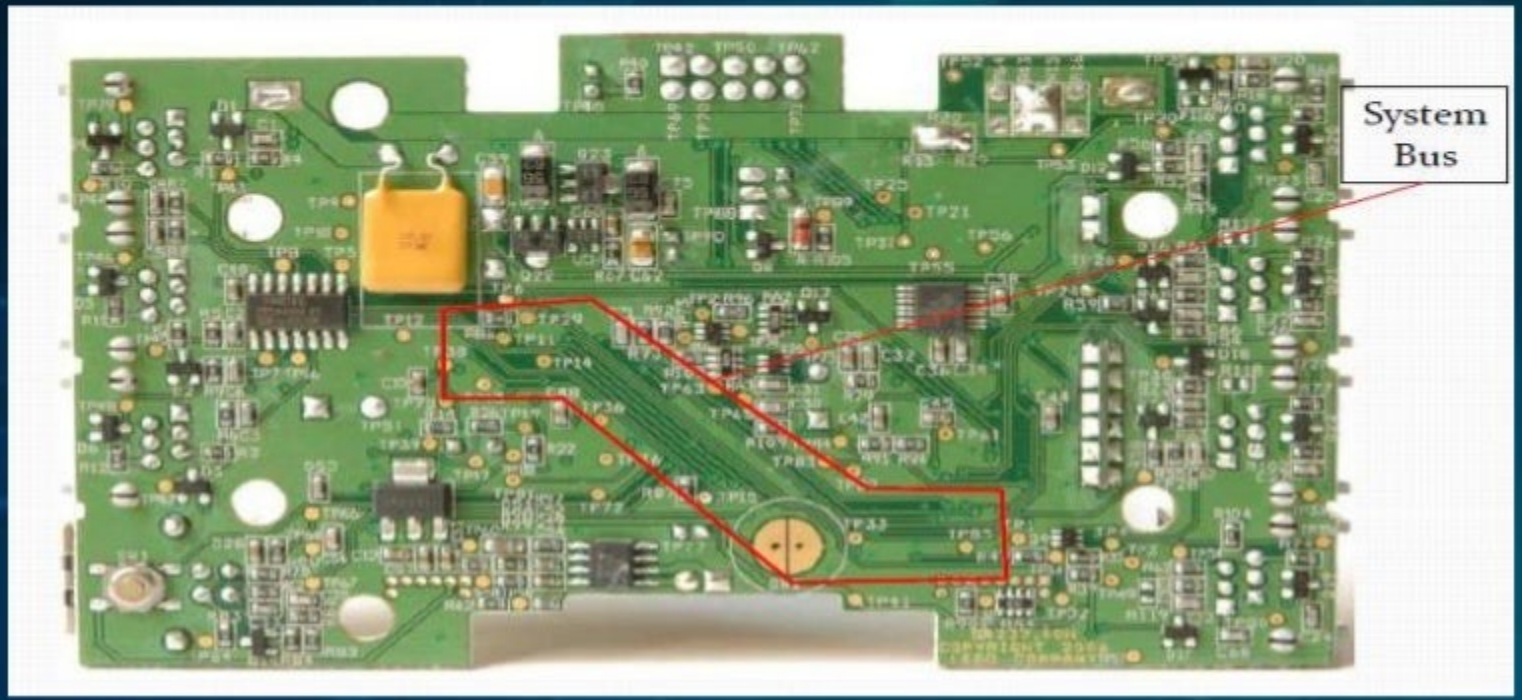
- The CPU sends various data values, instructions and information to all the devices and components inside the computer.

- If you look at the bottom of a motherboard you'll see a whole network of lines or electronic pathways that join the different components together.

- This network of wires or electronic pathways is called the '**Bus**'.

INTRODUCTION (cont'd)

- Bottom of motherboard



BUS

- A bus is a communication pathway connecting two or more devices.
- A key characteristic of a bus is that it is a shared transmission medium.
- Multiple devices connect to the bus, and a signal transmitted by any one device is available for reception by all other devices attached to the bus.
- If two devices transmit during the same time period, their signals will overlap and become garbled. Thus, only one device at a time can successfully transmit.

BUS cont'd

- Typically, a bus consists of multiple communication pathways, or lines. Each line is capable of transmitting signals representing binary 1 and binary 0.
- several lines of a bus can be used to transmit binary digits simultaneously (in parallel).
- For example, an 8-bit unit of data can be transmitted over eight bus lines.
- Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy.

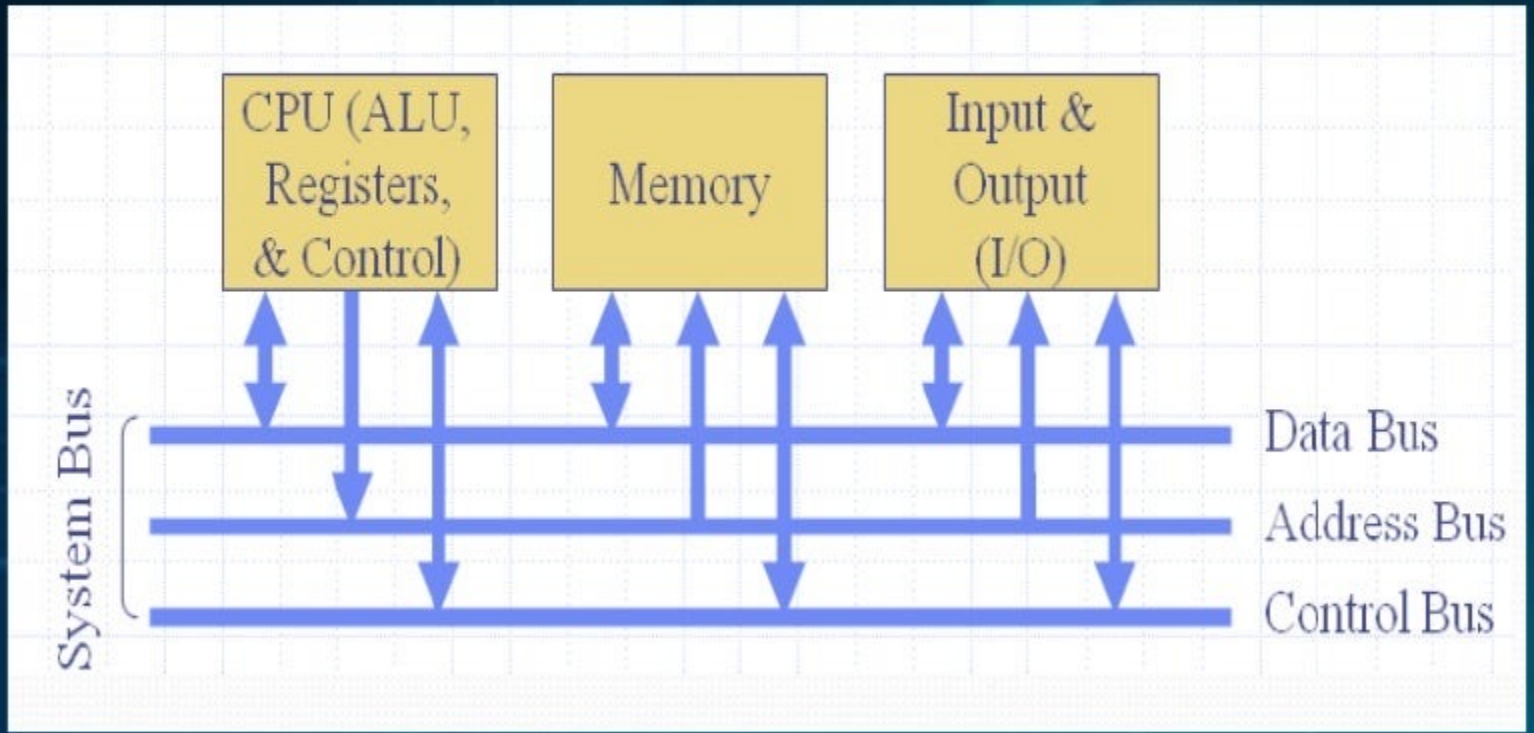
SYSTEM BUS

- A bus that connects major computer components (processor, memory, I/O) is called a **system bus.**
- A system bus consists, typically, of from about fifty to hundreds of separate lines. Each line is assigned a particular meaning or function
- **System bus** usually is separated into three functional groups .

1. ***Data Bus***
2. ***Address Bus***
3. ***Control Bus***

- In addition, there may be power distribution lines that supply power to the attached modules.

SYSTEM BUS MODEL



DATA BUS

- A collection of wires through which data is transmitted from one part of a computer to another.
- Data Bus can be thought of as a highway on which data travels within a computer.
- This bus connects all the computer components to the CPU and main memory.
- The data bus may consist of 32, 64, 128, or even more separate lines.
- The number of lines being referred to as the *width* of the data bus. Because each line can carry only 1 bit at a time, the number of lines determines how many bits can be transferred at a time.

DATA BUS cont'd

- It is a bidirectional bus.
- The size (width) of bus determines how much data can be transmitted at one time.
- E.g.
  - A 16-bit bus can transmit 16 bits (2 bytes)of data at a time.
  - 32-bit bus can transmit 32 bits(4 bytes) at a time.
- The size (width) of bus is a critical parameter in determining system performance.
- The wider the data bus, the better, but they are expensive.

ADDRESS BUS

- A collection of wires used to identify particular location in main memory is called **Address Bus**.
- Or in other words, the information used to describe the memory locations travels along the address bus.
- Clearly, the width of the **address bus** determines the maximum possible memory capacity of the system.
- N address lines directly address 2^N memory locations.

ADDRESS BUS cont'd

- It is an unidirectional bus.
- The CPU sends address to a particular memory locations and *I/O* ports.
- The address bus consists of 16 , 20 , 24 or more parallel signal lines.

ADDRESS BUS cont'd

- 8086: 20 address lines
  - Could address 1 MB of memory
- Pentium: 32 address lines
  - Could address 4 GB of memory
- Itanium: 64 address lines
  - Could address 264 bytes of memory

CONTROL BUS

- Because the data and address lines are shared by all components, there must be a means of controlling their use.
- The control lines regulates the activity on the bus.
- Control signals transmit both command and timing information among system modules.
- The control bus carries signals that report the status of various devices.

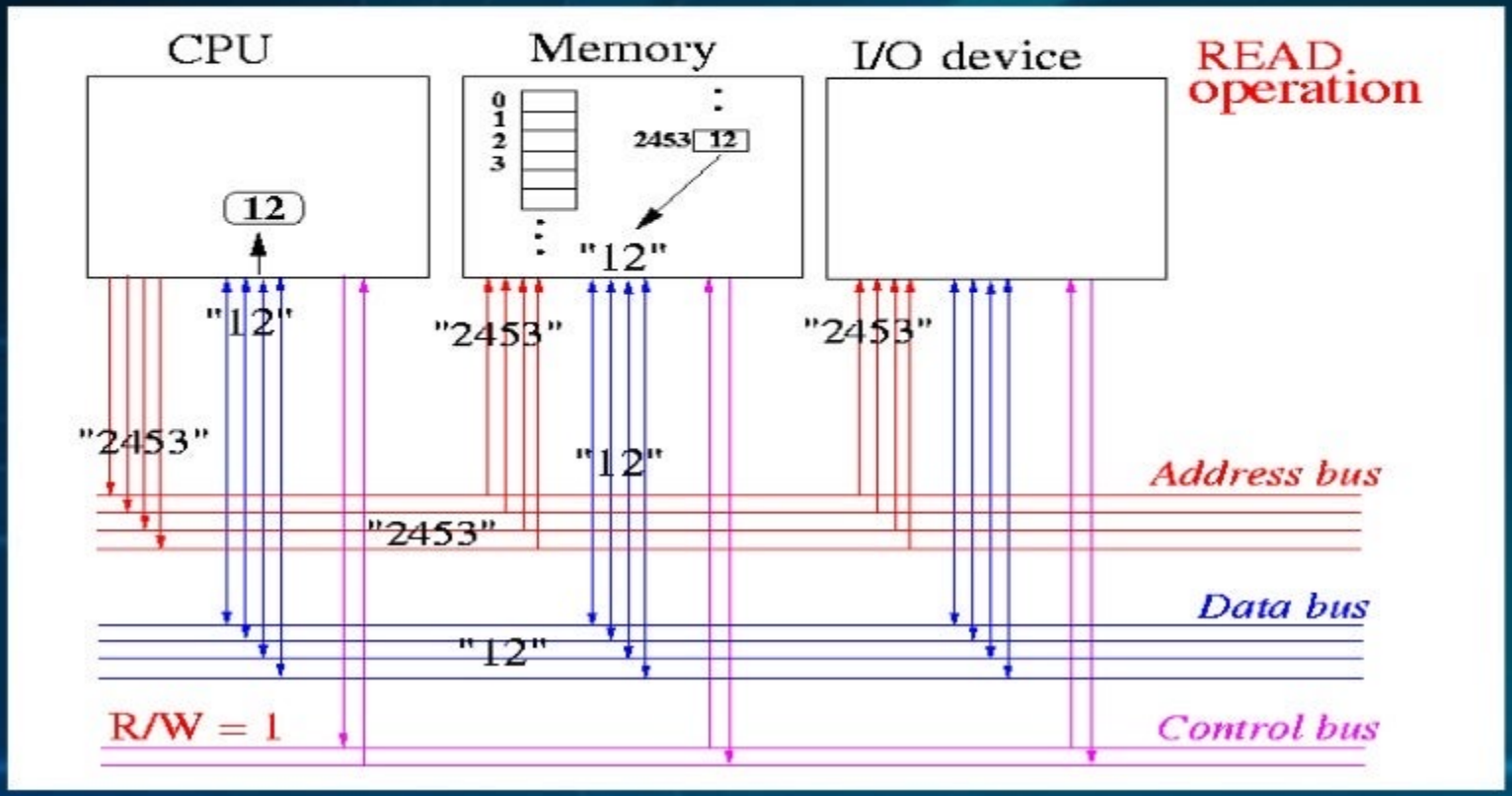
CONTROL BUS

- Typical control bus signals are :

- ***Memory Read*** : causes data from the addressed location to be placed on the data bus.
- ***Memory Write :*** causes data on the bus to be written into the addressed location
- **I/O write:** causes data on the bus to be output to the addressed I/O port
- **I/O read:** causes data from the addressed I/O port to be placed on the bus

Example : Memory Read

- The following figure shows how the CPU reads the value 12 from the memory location 2453:



Example: Memory Read cont'd

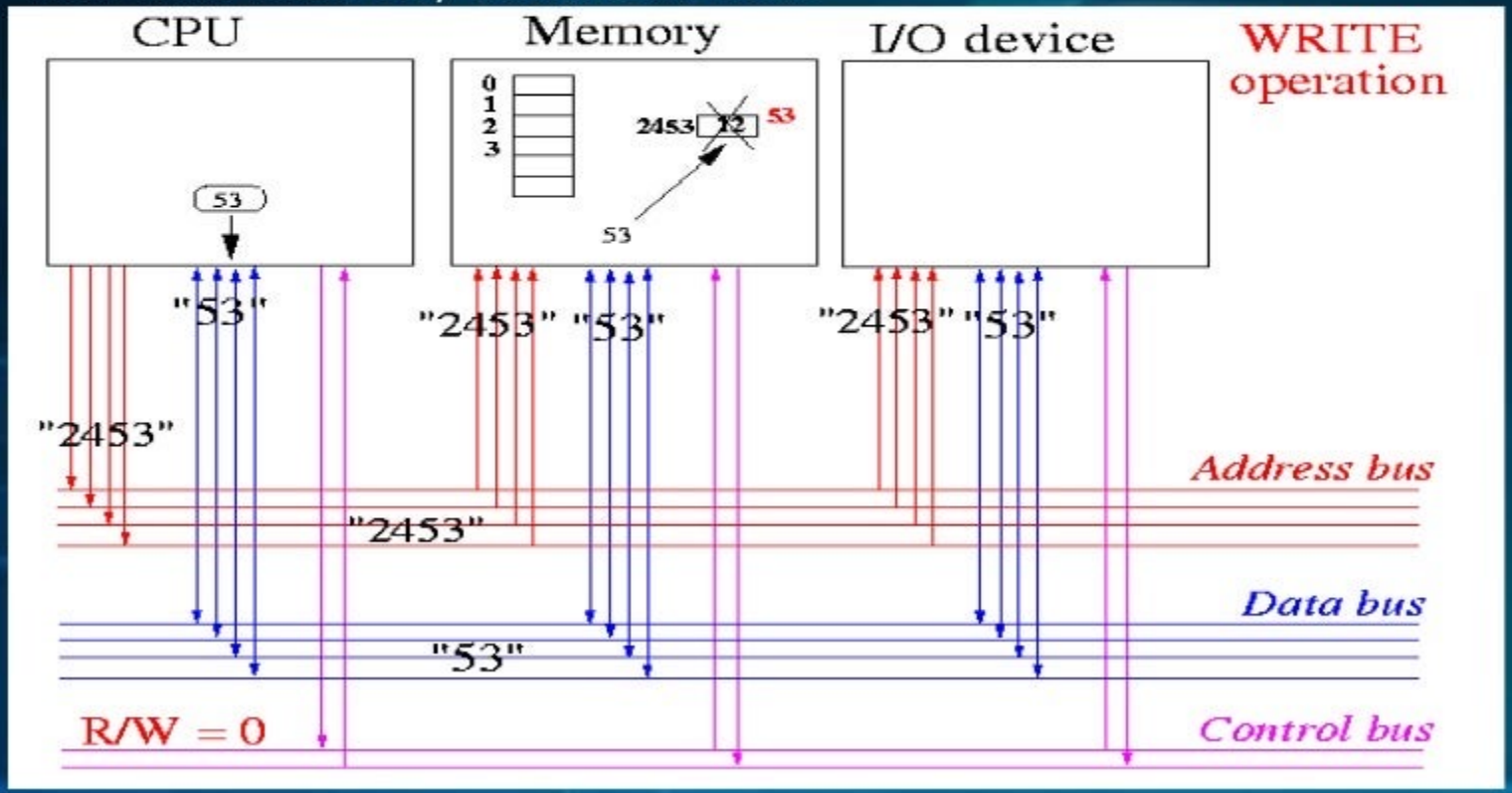
- CPU sends out the address value 2453 on the **address bus**
- Simultaneously, CPU sends out the signal **R/W = 1** on the **control bus,** which indicates a **READ** operation
- CPU then waits for the data from memory on the **data bus**
- The **R/W = 1** signal and the address bus value 2453 will cause the memory to retrieve the value at memory location 2453 to be sent out on the data bus

Memory Read a Closer look

- Address of next instruction is in PC
- Address (MAR) is placed on address bus
- Control unit issues READ command
- Result (data from memory) appears on data bus
- Data from data bus copied into MBR
- PC incremented by 1 .
- Data (instruction) moved from MBR to IR
- MBR is now free for further data fetches

Example: Memory Write

- The following figure shows how the CPU writes the value 53 from the memory location 2453:



Example: Memory Write cont'd

- CPU sends out the address value 2453 on the **address bus**
- Simultaneously, CPU also sends out the value 53 on the **data bus**
- And the signal **R/W = 0** on the **control bus** which indicating a WRITE operation
- The **R/W = 0** signal along with the address bus value 2453 and data bus value 53 will cause the memory to store the value 53 at the location 2453...

Control Bus cont'd

- Control lines also include :

- **Transfer ACK:** indicates that data have been accepted from or placed on the bus.
- **Bus request:** indicates that a module needs to gain control of the bus.
- **Bus grant:** indicates that a requesting module has been granted control of the bus.

Control Bus cont'd

- **Interrupt request:** indicates that an interrupt is pending.
- **Interrupt ACK:** acknowledges that the pending interrupt has been recognized.
- **Reset:** initializes all modules.

Bus Design Issues

- Need to consider several design issues :

* Bus width
  - » Data and address buses.
* Bus type
  - » Dedicated or multiplexed.
* Bus operations
  - » Read, write, block transfer, interrupt, …
* Bus arbitration
  - » Centralized or distributed.
* Bus timing
  - » Synchronous or asynchronous

Bus Operations

- Basic operations
  - Read and write.
- Block transfer operations.
  - Read or write several contiguous memory locations.
  - Example: cache line fill.
- Interrupt operation.