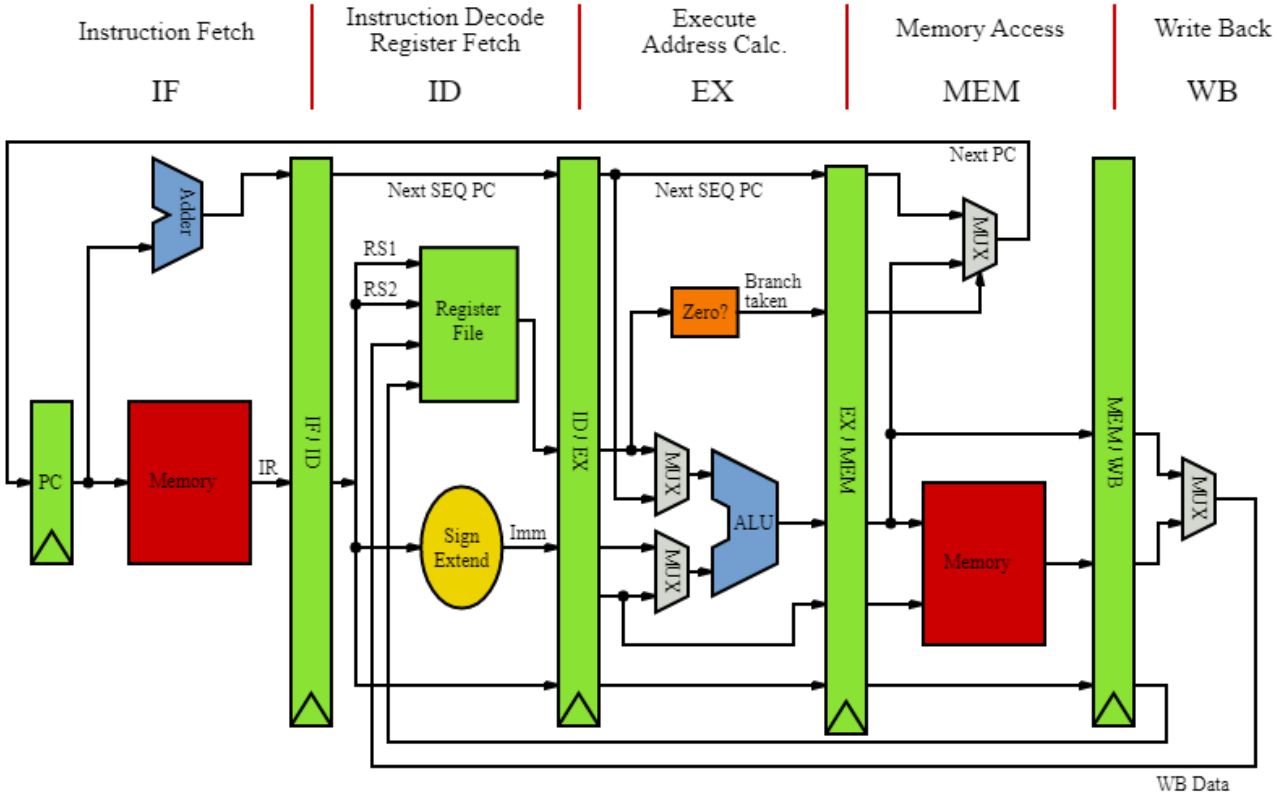
STUDY ON PROCESSORS

MIPS:

MIPS (Microprocessor without Interlocked Pipelined Stages) is a family of reduced instruction set computer (RISC) instruction set architectures, developed by MIPS Computer Systems, now MIPS Technologies.

The key concepts of the MIPS architecture are:

- Five-stage execution pipeline: fetch, decode, execute, memory-access, write-result.
- Regular instruction set, all instructions are 32-bit.
- Three-operand arithmetical and logical instructions.
- 32 general-purpose registers of 32-bits each.
- No status register or instruction side-effects.
- No complex instructions (like stack management, string operations, etc.)
- Only the load and store instruction access memory.
- Memory-management unit maps virtual to actual physical addresses.

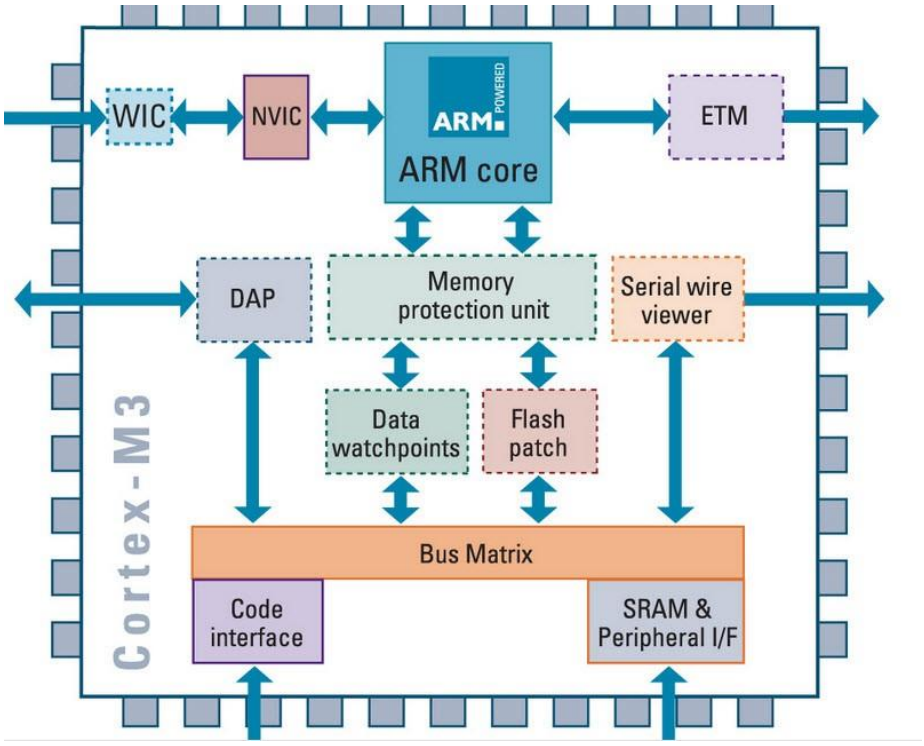


ARM:

ARM (formerly an acronym for Advanced RISC Machines and originally Acorn RISC Machine) is a family of reduced instruction set computer instruction set architectures for computer processors, configured for various environments.

The key concepts of the ARM architecture are:

- Load/store-based architecture.
- Single-cycle instruction execution.
- Consistent 16x32 bit register file.
- Link register.
- Easy decoding and pipelining.
- Power-indexed addressing modes.
- Fixed 32-bit instruction set.
- An orthogonal instruction set.
- Hardware virtualization support.

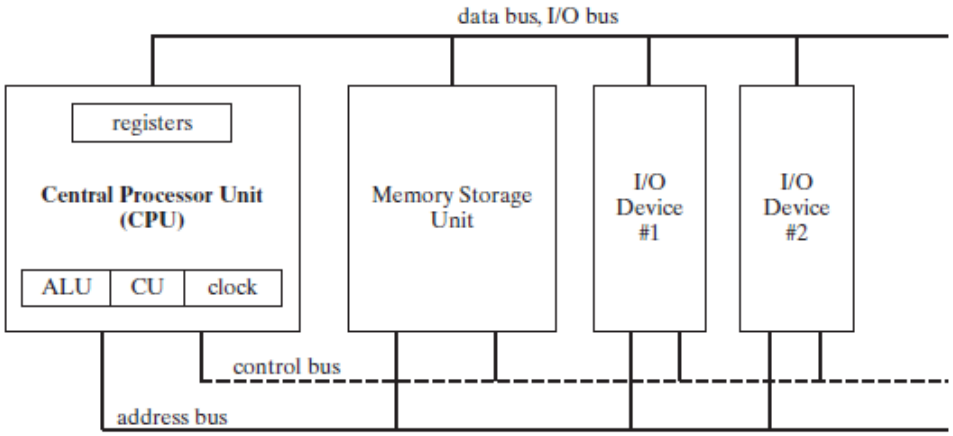


x86:

x86 is a family of complex instruction set computer (CISC) instruction set architectures initially developed by Intel based on the Intel 8086 microprocessor and its 8088 variant.

The key concepts of the x86 architecture are:

- The X86 instruction set allows for dynamic lengths for instructions.
- These registers on 32-bit x86 are in fact 32 bits or 4 bytes in size.
- The X86 CPU architecture uses little-endian ordering for memory storage.
- It contained write protect feature and offered a built in math co-processor that offloaded complex math operations from the main CPU.
- It has an addressable physical memory of 4 GB and data transfer width of 32-bits.



The registers are encoded using the 4-bit values in the X.Reg column of the following table. *X.Reg* is in binary.

X.Reg	8-bit GP	16-bit GP	32-bit GP	64-bit GP	80-bit x87	64-bit MMX	128-bit XMM	256-bit YMM	16-bit Segment	32-bit Control	32-bit Debug
0.000 (0)	AL	AX	EAX	RAX	ST0	MMX0	XMM0	YMM0	ES	CR0	DR0
0.001 (1)	CL	CX	ECX	RCX	ST1	MMX1	XMM1	YMM1	CS	CR1	DR1
0.010 (2)	DL	DX	EDX	RDX	ST2	MMX2	XMM2	YMM2	SS	CR2	DR2
0.011 (3)	BL	BX	EBX	RBX	ST3	MMX3	XMM3	YMM3	DS	CR3	DR3
0.100 (4)	AH, SPL[1]	SP	ESP	RSP	ST4	MMX4	XMM4	YMM4	FS	CR4	DR4
0.101 (5)	CH, BPL[1]	BP	EBP	RBP	ST5	MMX5	XMM5	YMM5	GS	CR5	DR5
0.110 (6)	DH, SIL[1]	SI	ESI	RSI	ST6	MMX6	XMM6	YMM6	-	CR6	DR6
0.111 (7)	BH, DIL[1]	DI	EDI	RDI	ST7	MMX7	XMM7	YMM7	-	CR7	DR7
1.000 (8)	R8L	R8W	R8D	R8	-	MMX0	XMM8	YMM8	ES	CR8	DR8
1.001 (9)	R9L	R9W	R9D	R9	-	MMX1	XMM9	YMM9	CS	CR9	DR9
1.010 (10)	R10L	R10W	R10D	R10	-	MMX2	XMM10	YMM10	SS	CR10	DR10
1.011 (11)	R11L	R11W	R11D	R11	-	MMX3	XMM11	YMM11	DS	CR11	DR11
1.100 (12)	R12L	R12W	R12D	R12	-	MMX4	XMM12	YMM12	FS	CR12	DR12
1.101 (13)	R13L	R13W	R13D	R13	-	MMX5	XMM13	YMM13	GS	CR13	DR13
1.110 (14)	R14L	R14W	R14D	R14	-	MMX6	XMM14	YMM14	-	CR14	DR14
1.111 (15)	R15L	R15W	R15D	R15	-	MMX7	XMM15	YMM15	-	CR15	DR15

1: When any REX prefix is used, SPL, BPL, SIL and DIL are used. Otherwise, without any REX prefix AH, CH, DH and BH are used.

x86_64:

x86-64 (also known as x64, x86_64, AMD64, and Intel 64) is a 64-bit version of the x86 instruction set, first released in 1999. It introduced two new modes of operation, 64-bit mode and compatibility mode, along with a new 4-level paging mode.

The key concepts of the x86 architecture are:

- 64-bit integer capability
- Additional registers & Additional XMM (SSE) registers
- Larger virtual address space
- Larger physical address space
- Larger physical address space in legacy mode
- Instruction pointer relative data access
- SSE instructions
- No-Execute bit
- Removal of older features