Bus Structure

Bus structures and organizations

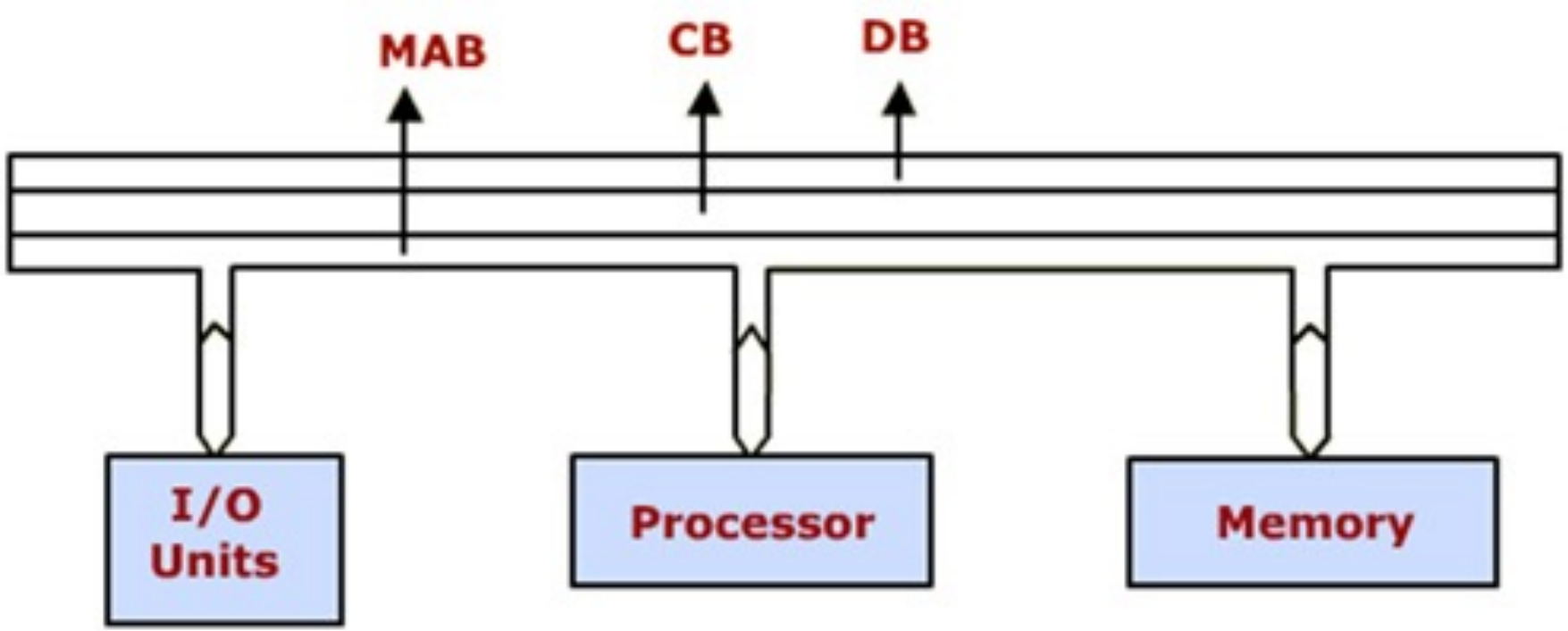
Two types of Bus organizations:

- Single Bus organization
- Two bus Organization

Single Bus Structure

- Three units share the single bus. At any given point of time, information can be transferred between any two units
- Here I/O units use the same memory address space (Memory mapped I/O)
- So no special instructions are required to address the I/O, it can be accessed like a memory location
- Since all the devices do not operate at the same speed, it is necessary to smooth out the differences in timings among all the devices. A common approach used is to include buffer registers with the devices to hold the information during transfers
- Ex: Communication between the processor and printer

Single bus structure



Single - Bus Organization

Two Bus/Double Bus structure

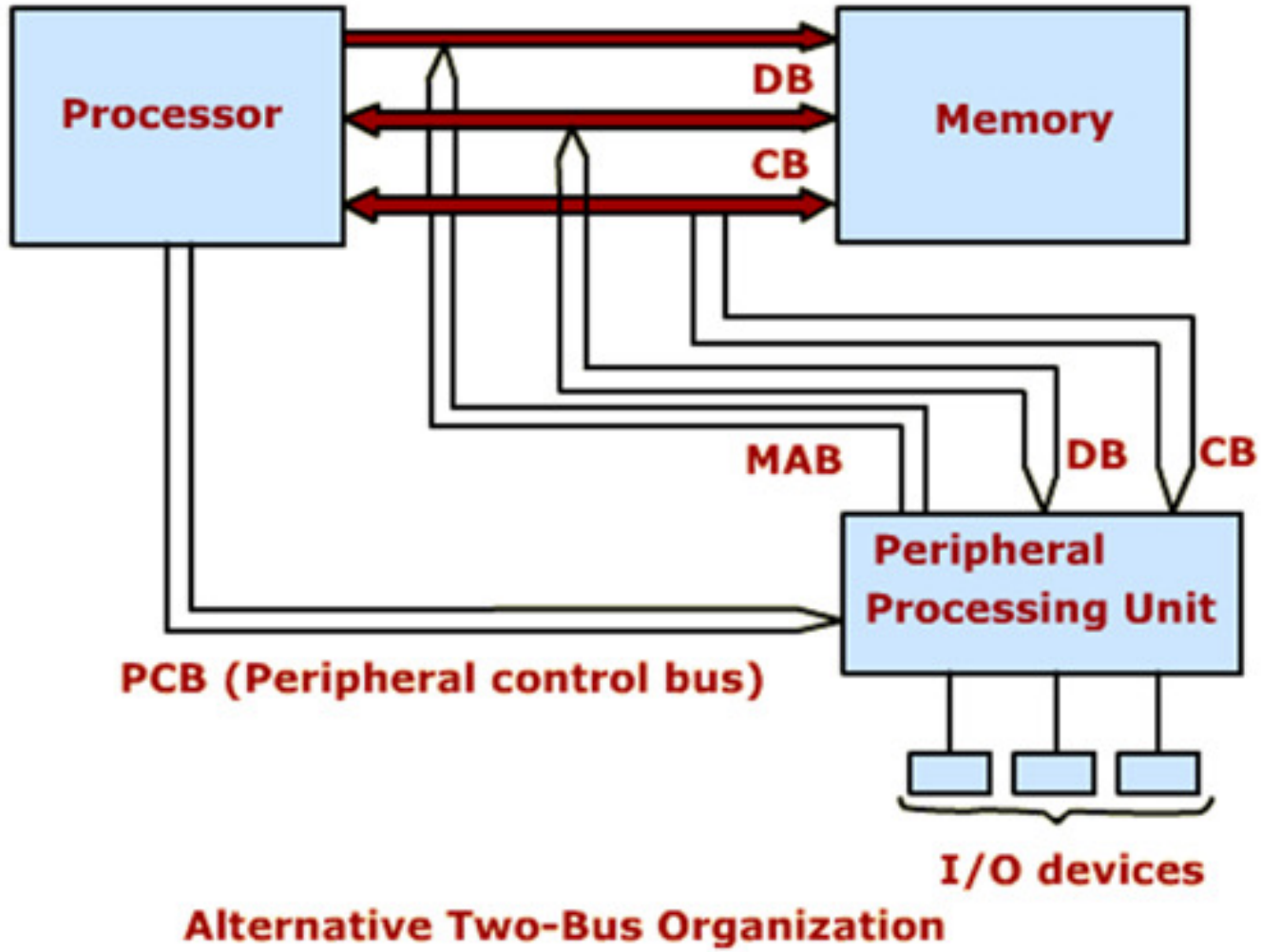
- Various units are connected through two independent buses
- I/O units are connected to the processor though an I/O bus and Memory is connected to the processor through the memory bus
- I/O bus consists of address, data and control bus
- Memory bus also consists of address, data and control bus
- In this type of arrangements processor completely supervises the transfer of information to and from I/O units. All the information is first taken to processor and from there to the memory . Such kind of transfers are called as program controlled transfer

Two Bus/Double Bus structure

Alternative Two-bus architecture

- In this I/O units are directly connected to the memory and not to the processor
- The I/O units are connected to special interface logic known as Direct Memory Access (DMA) or an I/O channel. This is also called as Peripheral Processor Unit (PPU)
- In this the data from the I/O device is directly sent to memory bypassing the processor.

Alternative Two-bus architecture



Bus Standards

- ISA (Industry standard Architecture)
  - -Developed by IBM
  - -Speed is 8 MHz
  - -16 bit Interface
- EISA (Extended Industry Standard Architecture)
- VESA (Video Electronics Industry Standard Architecture)
- PCI (Peripheral Component Interconnect)
  - -Developed by Intel
  - -Speed is 33MHz,Also available in 66MHz speed
  - -64 bit interface

Single Bus Structure	Double Bus Structure
One common bus is used for communication between peripherals and processor.	Two buses are used, one for communication from peripherals and other for processor.
Instructions and data both are transferred in same bus.	Instructions and data both are transferred in different buses.
Its performance is low.	Its performance is high.
Cost of single bus structure is low.	Cost of double bus structure is high.
Number of cycles for execution is more.	Number of cycles for execution is less.
Execution of process is slow.	Execution of process is fast.
Number of registers associated are less.	Number of registers associated are more.
At a time single operand can be read from bus.	At a time two operands can be read.

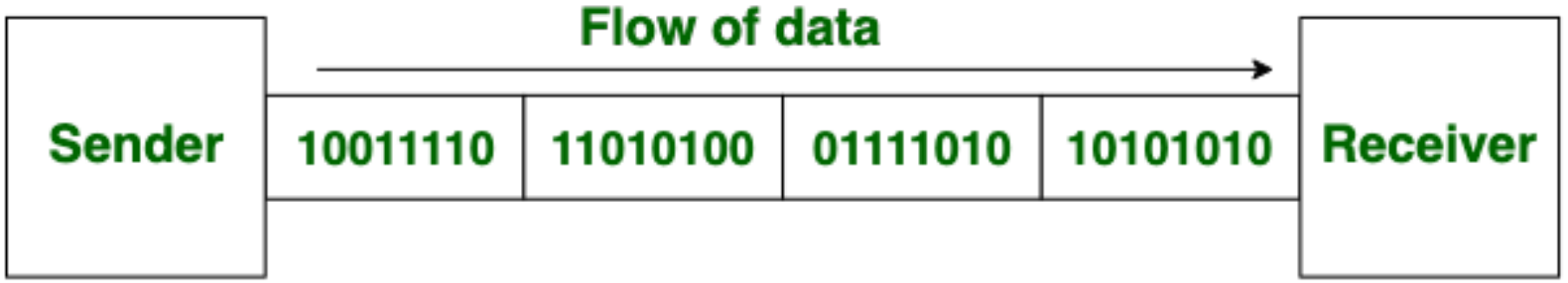
Synchronous and Asynchronous bus

Synchronous bus:

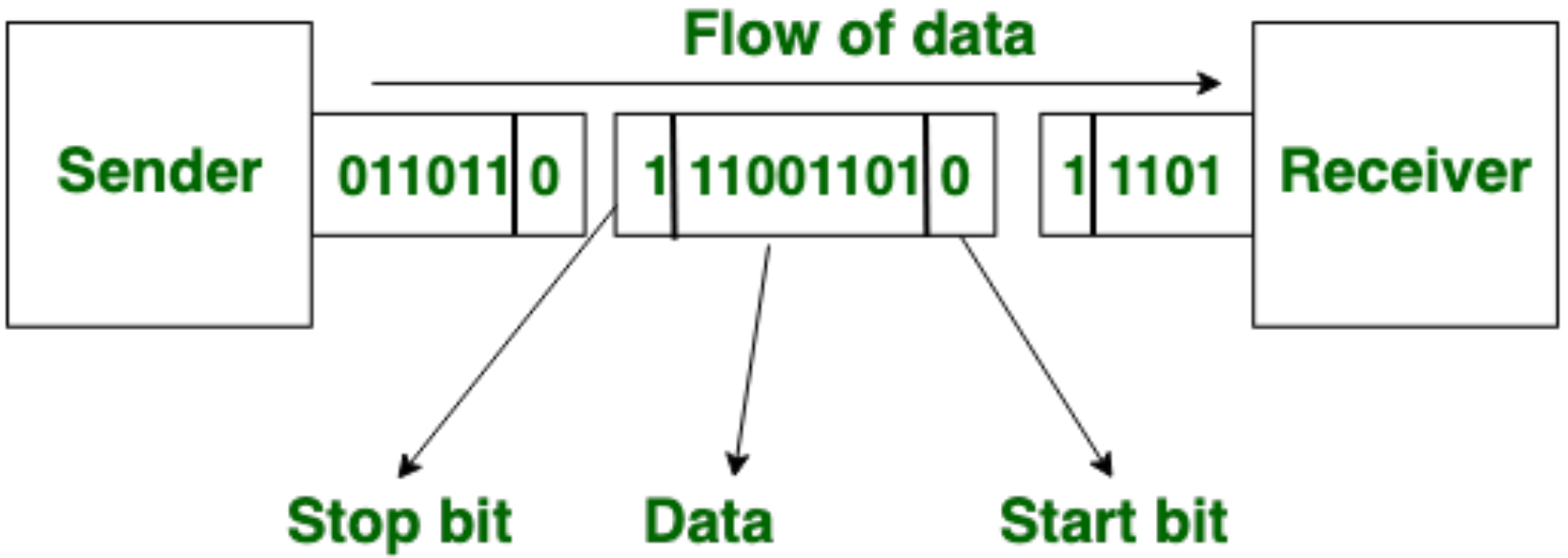
- Transmitter and receivers are synchronized of clock.
- Data bits are transmitted with synchronization of clock.
- Character is received at constant Rate.
- Data transfer takes place in block.
- Start and stop bit are not required to establish communication of each character.
- Used in high – speed transmission.
- Processor to memory buses are now normally synchronous.

Asynchronous bus

- Transmitters and receivers are not synchronized by clock.
- Since the bus is not clocked devices of varying speeds can be on the same bus.
- Bit’s of data are transmitted at constant rate.
- Character may arrive at any rate at receiver.
- Data transfer is character oriented.
- Start and stop bits are required to establish communication of each character.
- Used in low – speed transmission.
- Common is a handshaking protocol



Synchronous Transmission



Asynchronous Transmission