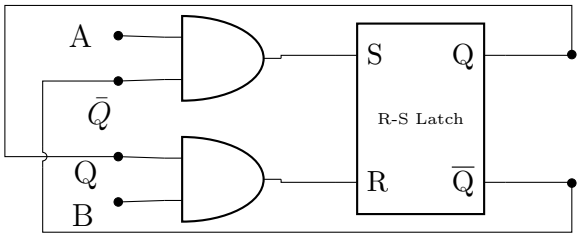
1. The two inputs A and B are connected to to an R-S latch via two AND gates as shown in the figure. If $A = 1$ and $B = 0$, the output $Q\bar{Q}$ is



(GATE-IN2017)

(a) 00

(b) 10

(c) 01

(d) 11