ABSTRACT

The machine positioning errors in modern day CNC machine tools are measured offline using a laser interferometer at rapid feedrate and corrections are fed into CNC system. This approach doesn't take care of positioning errors occurring due to different feedrates leading to different patterns of temperature rise and also servo related errors. Hence it conforms the existing methods are appropriate but not optimal. Using Adaptive Real-Time Compensation method, errors are monitored and compensated during the machining process, which takes care of geometric errors, servo errors and thermal errors.

This work is concerned with enhancing the positional accuracy of ultra precision machine tools through compensating positional error using algorithm based on Neural Networks. An ARM7 Micro-Controller based embedded controller has been designed and developed to compute Thermal error compensation value basically meant for Machine Tool Applications. The controller has an interface to Temperature sensors on one end and Computerized Numerical Controller (CNC) on the other end. This controller has an interface to connect about 8 Temperature sensors.

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NOMENCLATURES

I/O	Input/output
A/D	Analog and Digital
PLL	Phase Lock Loop
MMR	Memory Management Register
RTD	Resistance Temperature Dependant
PT100	Platinum material with 100Ω at 0°C
JTAG	Joint Test Action Group
CNC	Computerized Numerical Control
ISP	In Serial Programming
IAP	In-Application Programming
PAC	Programmable Counter Array
WDT	Watchdog timer
FIQ	Fast Interrupt Request
SOIC	Small Outline Integrated Circuit
TSSOP	Thin Shrink Small Outline Package
GPIO	General Purpose Input Output
LQFP	Low Profile Quad Flat Pack packages
MSPS	Million samples per second
UART	Universal Asynchronous Receiver/Transmitter

ALE	Address Latch Enable
TTL	Transistor–transistor logic
CMOS	Complementary Metal–Oxide–Semiconductor
SPI	Serial Peripheral Interface
lsb	Least Significant Bit

CHAPTER-1 INTRODUCTION

The main reasons for dimensional and geometric errors in workpieces produced on machine tools include low static stiffness of the machine structure, low dynamic performance of feed drives, tool wear and thermal deformations of the tool, machine and workpiece. Among which, the thermal error is the most important source, which significantly influences the machining accuracy of the machine tools. Thermally induced deformations in machine tools lead to thermal drift displacements between tool and workpiece, as shown in Fig. 1 (M.Weck, 1995). There have been many research reports in this subject over the past years. A reduction of the thermo displacements of more than 80% of the initial value is possible (C.Brecher, 2004,Jan Ni, 1997,S.Yang, 1997,N.Srinivasa, 1996,R.Ramesh, 2002,H.Yang, 2003,H.J.Pahk, 2003). Some of them utilize various sophisticated models, which do not meet industrial requirements in terms of the cost and simplicity. In addition, many researches follow the current ISO 230-3 international standard that still specifies to experimentally generate the thermal error model of the machine tool under non-cutting (air-cutting) condition (ISO 230-3, 1994). The proposed 5-channel non-contact displacement setup by ISO is shown in Fig. 2. It, in fact, does not exactly reflect the real phenomenon in industrial practice, where any machine tool must cut the metal to produce the part. Therefore, thermal error of the machine tool should be paid with more attention under the real-cutting condition (K.C.Fan, 1995, J.S.Chen, 1996 and 1997, K.G.Ahn, 1999). Major considerations are not only to the effectiveness and applicability but also its cost and simplicity in the model generation and error compensation within a very short time.

Major barriers hindering the development and practical implementation of precision machining specifically include:

Inaccurate and non-robust prediction model for thermal errors. Thermal errors have become the major contributor to the inaccuracy of machine tools. Time-variant thermal errors are more elusive to model than geometric errors.The robustness of the

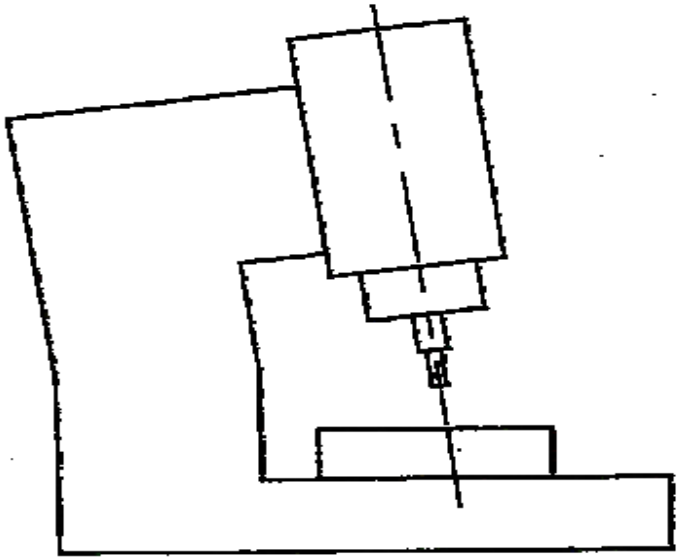


Figure 1. 1: Sketch of C shape machine tool with thermal distortion

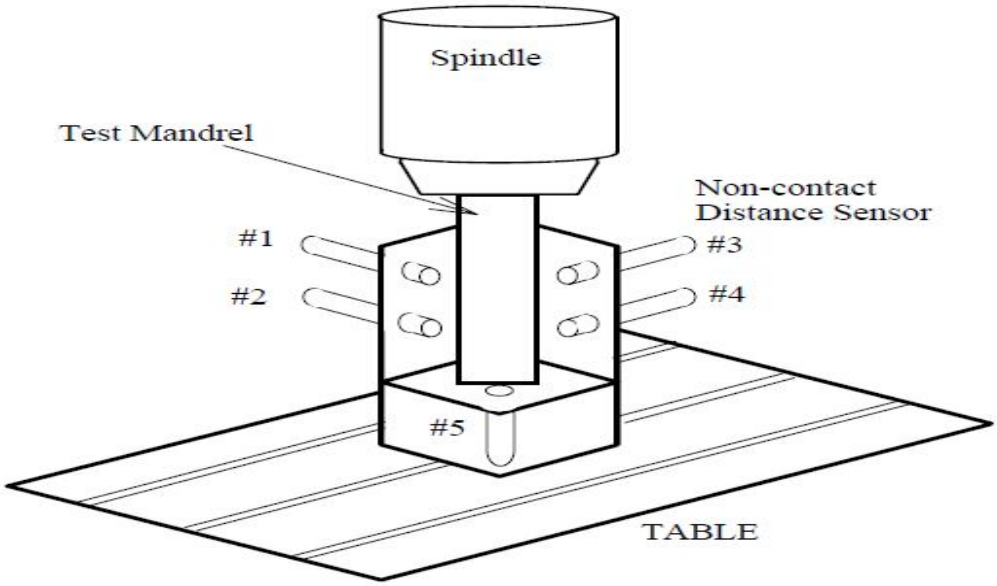


Figure 1. 2: Non-cutting test of spindle thermal drift

thermal error model under various working conditions depends on the thoroughness of the training process and the length of characterization time. A model estimated under one working condition may not be applicable under other working conditions.

1.1. Objective

In this report, a fast and low cost thermal error measurement and compensation system is proposed. The thermal sensor RTD (PT100) was used for measuring temperature, which maintains high accuracy for a long period. With the proper selection of sensor locations, the thermal error of any particular machine can be modeled by a linear function with least temperature terms. The diagnosed error model could be stored in a developed single board from which the compensation commands could drive the CNC controller to implement real-time error compensation without interrupting the existing NC program.

To provide thermal compensation to CNC machine there are different ways

1) It is necessary to open the CNC machine and make changes in parameters within the CNC Control flow command and then provide thermal compensation.

2) Above method is risky as factory settings are going to be change.

In this thermal compensation is provided based on the thermal error algorithm.

So, Second method is followed and its main advantage is that this circuit can be used for any CNC machine wherever displacement operation is performed using motor.

In second, difficulty lies in adding and removing counting pulses from feedback signal, because pulses comes with very high speed and this operation has to be performed in microseconds.

1.2. Basic Machine Tool Error Reduction

1.2.1 Error Sources

Machined part accuracy is essentially determined by machine tool performance from the point of view of compliance to tolerance, surface definition, etc. Accuracy is one of the most important performance measures, the ability to

control errors to optimize performance while maintaining cost is crucial in the machine tool industry.

In general, there are two basic categories of errors, quasi-static errors and dynamic errors. Quasi-static errors are errors in the machine, fixturing, tooling, and workpiece that occur relatively slowly (Slocum, 1992). Sources of this type of errors include geometric errors, kinematic errors, thermal errors, cutting force induced errors, etc. Geometric errors are defined as errors in the form of individual machine components. Kinematic errors are caused by misaligned components in the trajectory. Thermal errors are induced by thermo-elastic deformations due to internal and external heat sources of a machine tool. As heat generation at contact points is unavoidable, thermal errors are one of the most difficult error sources to completely eliminate.

Dynamic errors are, on the other hand, primarily caused by structural vibration, spindle error motion, controller errors, etc. They are more dependent on the particular operating conditions of the machine. Overall, quasi-static errors account for about 70 percent of the total errors of a machine (Bryan, 1990).

1.2.2 Error Reduction Methods

Error avoidance and error compensation are the two basic approaches to improve the machine tool accuracy (Ni, 1997). The general approach to apply error avoidance is to build an accurate machine during its design and manufacturing stage so that the error sources could be kept to a minimum extent. Good rules of thumb such as reasonable assignment of stiffness, proper addition of damping, careful selection of materials, symmetrical structure design, and the like are extensively adopted. Error avoidance by the refinement of a machine from its basic structure or the control of working environment is generally accepted as the most desirable way to eliminate errors. This approach, however, has two inevitable drawbacks. On the one hand, it is impossible to eliminate all the errors solely by

design and manufacturing techniques; on the other hand, the machining costs rise exponentially as the level of precision requirement is tightened.

Unlike error avoidance, no attempts are made to avoid errors for error compensation. Rather, errors are allowed to manifest themselves, and then be measured and corrected. As the accuracy of a machine tool is affected by various error sources, error compensation places more emphasis on the interactive impact rather than individual errors. The basic idea of error compensation does not aim at reducing the absolute value of errors, but the effects of these errors on the machining accuracy and final dimensions of produced parts. Error compensation gains its importance because design and operating specifications are either difficult to realize or subtly contradictory to each other. Moreover, compensation is considered as an efficient method for periodic machine accuracy enhancement during the machine utilization over the years.

Nevertheless, there also exist limitations in error compensation techniques. The degree to which machining accuracy can be achieved by error compensation is highly dependent on the repeatability of the machine itself and the method selected to demonstrate the interconnection between different errors. The former is closely related to the design and fabrication of the machine, in other words, error avoidance approach sets the bottom line of the performance improvement that can be obtained through error compensation. The latter highly depends on the insight into the influences of errors on the machining accuracy, which could not be easily embraced in mathematical models.

1.3. Thermal Error Compensation

The thermal error is one of the most significant factors influencing the machine tool accuracy (Bryan, 1990). With the improvement of machine tool positioning accuracy and machining performances, thermal errors become even more significant.

Most machine tools are unavoidably subject to continuously varying operating conditions. The internally generated heat and environment temperature gradient

render the machine tool exposed to complex and changing temperature distributions. As mentioned by Bryan (1990), there are six main thermal error sources: (1) heat generated from the cutting process, (2) by the machine energy loss, (3) hydraulic oil, coolant, and cooling systems, (4) room environment, (5) people, and (6) thermal memory from previous environment. The thermal deformation errors thus caused are even more difficult to quantify and predict if the complicated structure of a machine tool is taken into account.

Thermal errors can be divided into two categories, position independent thermal errors (PITE) and position dependent thermal errors (PDTE) (Chen et al., 1993). PITE change as a function of temperature but not the axis position. The effect of PITE on component accuracy is strongly dependent on the rate of change of the PITE relative to the time taken to produce a part. PDTE change as a function of axis position as well as temperature. They effectively alter the linear positioning of the machine. To simplify the problem and determine the most suitable thermal error compensation techniques, it is useful to differentiate these two kinds of thermal errors.

Researchers have been investigating the influences of thermal errors on the machine tool accuracy and seeking solutions to reduce these errors for decades. Special approaches pertaining to the thermal error avoidance include: (1) reducing and relocating heat sources (Donaldson and Thompson, 1986), (2) rearranging the machine tool structure to achieve thermal robustness (Spur et al., 1988), and (3) using materials that have strong thermal stiffness (Suh and Lee, 2004). Controlling the environmental temperature is also helpful in reducing thermal errors, because daily environment temperature fluctuation is one of the major heat disturbances. For the implementation of thermal error compensation, besides the common approach of moving machine slides through sending compensatory signals to CNC controller, artificially controlled heat sources on machine tool structures are employed to offset

the thermal bending effects, thus eliminating the thermal errors (Sata et al., 1975; Hatamura et al., 1993; Fraser et al., 1999c).

1.3.1 Thermal Error Identification

Thermal error identification is one of the crucial steps for a successful thermal error modeling and compensation. There are two basic error identification categories: workspace measurement approach and error synthesis approach (Yang, 2002).

In workspace measurement approach, the required compensation values are determined by making direct measurements of the thermal errors between the tool tip and workpiece during machining (Yandayan and Burdekin, 1997). Normal machining process is usually stopped and a probe is used to measure a datum or reference point on the machine; error maps are then generated associated with different machine temperature status and axis positions.

Chen (1996b) developed a quick setup and multiple-error measurement system with on-line probes. Measurements were performed at several selected points, and the thermal errors at any location of the working zone were interpolated in between. Direct measurement is very effective in correcting slowly changing thermal errors, but has the disadvantages of requiring potentially expensive additional measurement equipment and intruding into the machining process, thus reducing the production efficiency.

In error synthesis approach, the resultant thermal errors at the tool tip are computed by combining the measurement of the distortion of each individual machine element along the kinematic chain of a machine tool. This method gives the comprehensive evidence of the accuracy of each machine element, but is generally time consuming.

A laser interferometer and non-contact capacitance sensors are usually used to directly measure the thermal errors, such as the linear and angular errors of

moving axis under changing temperature fields and the thermal expansion of the rotating spindle (Donmez et al., 1986; Chen et al., 1993; Lo et al., 1995). Because there are many thermal error components to be measured separately, the labor-intensive calibration procedures must be repeated several times. In addition, the interactive impact between the thermal error sources is sometimes ignored. Reference artifacts or gauges with known dimensions are also exploited for the thermal error identification. Error components are inversely estimated based on the comparison of the measurement results and the reference values (Ziegert and Kalle, 1994; Li et al, 1997; Kim and Chung, 2004). A large number of equation derivations and parameter estimation make this method relatively complicated. The derived relationship between the machine error components and the aggregate thermal errors might not be able to accurately predict the dimensional accuracy of the finished parts.

"Part-oriented" identification techniques were developed to relate the part-feature errors of a part family with machine tool errors. Mou et al. (1995a and 1995b) presented a feature-based analysis technique to relate the dimensional and form errors of manufactured features to the machine tool thermal errors. This approach dealt with mathematic models and measurements closely related to the real parts. This method is applicable for the mass or batch production, where the machine tools are dedicated to a particular part family. Therefore, only a limited number of part-feature related machine tool errors are important and need to be identified.

1.3.2 Thermal Error Modeling

For most thermal error compensation systems, mathematical models are necessary to relate the thermal errors to other variables that are easier to measure. Although the use of variables such as spindle speed (Li et al, 1997; Lim and Meng, 1997) and strain gauges measurement (Hatamura et al., 1993) have been reported in the literature, temperature measurements at certain key positions on

the machine tool structures are most widely utilized. Consequently, mathematical models describing the relationships between the thermal errors and the temperature measurements become essentially important. Various thermal error models underlining the thermo-elastic relationship have been investigated and applied for the thermal error compensation. They are categorized into two groups: time independent static models and time dependent dynamic models (Yang, 2002).

For time independent static model, only current temperature measurements are taken as the model inputs. Donmez et al. (1986) derived a polynomial function of the temperature rise at the spindle bearings to predict the spindle tilt-up error of a turning machine. Chen and Chiou (1995) compared the thermal error modeling effects by using multiple regression analysis (MRA) and artificial neural network. In recent years, different types of neural network have been employed in the thermal error modeling (Veldhuis and Elbestawi, 1995), including cerebellar model articulation controller (CMAC) neural network (Yang et al., 1996), fuzzy ARTMAP neural network (Srinivasa and Ziegert, 1997), and the like. Ramesh et al. (2003a and 2003b) utilized the Bayesian network and support vector machine (SVM) model to classify the thermal errorsdepending on the operation conditions and develop the mapping of the thermal errors with the machine tool temperature profile.

For time dependent dynamic models, time is either explicitly taken as the model inputs (Kim and Cho, 1997) or implicitly inferred by including previous temperature measurement. Janeczko (1989) observed that the spindle thermal expansion has a lagging characteristic compared with the collected temperature at certain sensor locations, so an exponential function, including time constant and expansion length, was developed to estimate spindle thermal expansion errors. Moriwaki (1998) experimentally determined the transfer functions between the spindle rotation speeds and thermal displacement, and between the air

temperature and thermal displacement, respectively. Convolution was used to determine the time domain thermal deformation based on the linear system assumption, and model adaptation was performed for different spindle speeds.

Fraser et al. (1998a, 1998b, 1999a, 1999b and 1999c) proposed a generalized modeling approach to model the thermal-elastic relationship. Inverse heat conduction problem (IHCP) was resolved to identify the heat sources from temperature reading and then system model was derived to predict thermal deformation according to these heat sources. The generalized model for the thermal deformation process and generalized transfer functions of the dynamic thermal deformation process in the *S*-domain were determined for the purpose of control system design.

Wang et al. (1998) presented a systematic methodology for the thermal error correction of a machine tool. The thermal deformation was modeled using the grey system theory to dynamically predict the thermal errors. Unfortunately, some short-term dynamics of the system were lost due to the properties of Accumulated Generating Operation (AGO). Therefore, the model obtained under one particular operating condition was not robust under other conditions.

Yang and Ni (2003) proposed an Output Error (OE) model to describe the dynamic nature of machine tool thermal errors by considering the time series of both temperature inputs and thermal deformation outputs for model estimation. This approach significantly improved the accuracy and robustness of thermal error models. Yang and Ni (2005a) presented a recursive model adaption mechanism based on the Kalman filter technique with multiple-sampling horizons to update the thermal error model during continuous changes of manufacturing conditions such as system reconfiguration or performance degradation over a long period.

The abovementioned approaches are empirical and highly dependent on the model training conditions. Numerical methods, such as the finite difference method (FDM) and the finite element method (FEM) are also utilized for the development of thermal error models. The numerical methods are powerful tools in simulating the practical heat transfer and thermo-elastic processes, where analytical solutions to temperature fields and thermal deformations are prohibited due to the complexity of machine tool structures.

Attia and Kops (1981a) approximated the thermal behaviours and deformations of a machine tool structure in response to the effect of fixed joints using the FEM. Moriwaki (1988) used the FDM to predict and compensate for the thermal deformations of a hydrostatically supported precision spindle. Lingard et al. (1991) analyzed the temperature perturbation effects on a high precision CMM using the FEM. Jedrzejewski and Modrzycki (1992) applied the FEM to optimize the thermal behaviour of a machine tool under various service conditions.

The absolute accuracy of the numerical methods is limited by several complex uncertainty factors, such as geometrical dimensions, boundary conditions, and machine joints. However, the limitations with respect to the reliability of quantitative results cannot reduce the impact of numerical methods on the qualitative evaluation of machine tool accuracy (Weck et al, 1995). The FEM is capable of making important contributions in deciding the initial temperature sensor locations for the subsequent thermal error modeling (Bryan, 1990).

1.3.3 Temperature Sensor Placement

For those thermal error models with temperature as inputs, the locations of temperature sensors play a vital role in determining the accuracy, efficiency and robustness of the derived models. Generally speaking, to put a large number of temperature sensors onto the machine structure can improve the accuracy and

robustness of the thermal error model. Balsamo et al. (1990) initially used nearly 100 temperature sensors to predict the thermal deformations of a CMM.

However, it is always an engineering concern to reduce the number of temperature sensors. Some researchers chose the variables based on their experiences with the potential heat sources and machine tool thermal deformations (Donmez et al., 1986; Moriwaki, 1988). Correlation coefficients between thermal errors and temperature variables were exploited to select highly correlated temperature variables for modeling (Kurtoglu, 1990). Chen et al. (1996b) used a standard step-wise regression method to find better linear models with multiple temperature variables. The most strongly correlated temperature variables were first included; then one temperature variable was either added or subtracted at a time based on the statistical significance evaluation of that variable. Lo et al. (1999) used an objective function formulated by a modified model adequacy criterion based on the Mallow's to select the temperature variables.

In most researches, complete information of the dynamic characteristics of the temperature fields and the thermal errors is not considered in determining the temperature sensor locations. If temperature sensors are not placed within the significant sensing areas of a machine tool structure, the resultant thermal error models cannot be robust under various operating conditions. Ma (2001) proposed an optimization method to locate temperature sensors. The basic rule for selecting optimal sensor locations is that the smaller the frequency of the thermal load is, the farther the sensor should be mounted away from the heat source. This method is theoretically appealing, but has not yet been applied and validated through practical experiments. Therefore, it is still necessary to develop a systematic methodology for optimizing the temperature sensor locations so that the waste of time and resources can be reduced.

CHAPTER 2 SYSTEM OVERVIEW

2.1 Basic Block Diagram

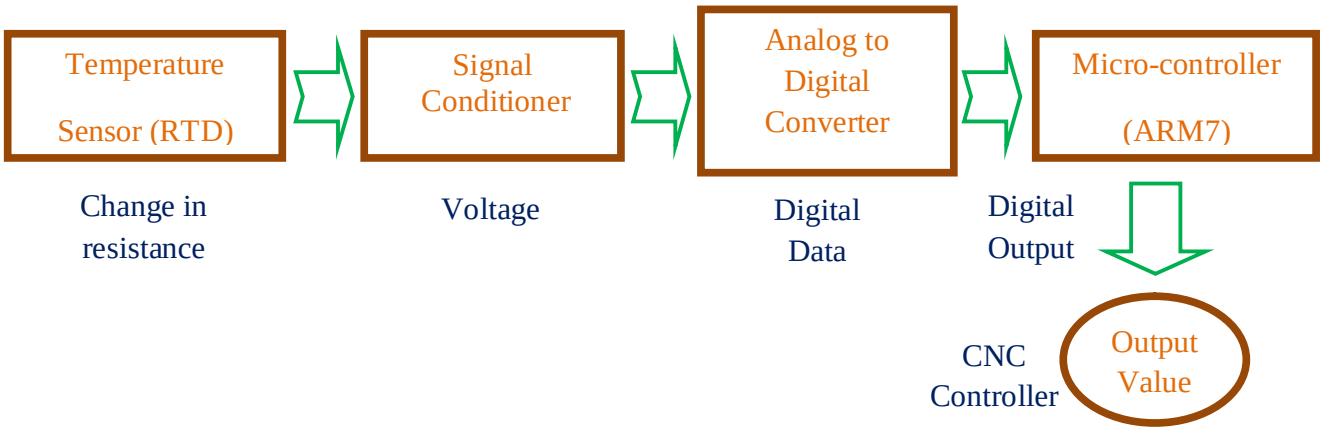


Figure 2. 1 Basic Block Diagram

In this project, Temperature sensor signal is taken from RTD (PT100) and then it is given to Signal Conditioner for improving the strength of signal and then it is given to Analog to Digital (A/D) Converter

In A/D Converter the analog data is converted to digital data because micro-controller understands the language of digital i.e.0&1.

Micro-controller takes digital data from A/D Converter and then generates digital output based on Thermal Compensation Algorithm.

2.2 Micro-controller

The required specifications of the Micro-controller are:

1) Frequency range minimum 20MHz operating

2) Minimum SPI interface.

3) Minimum 32KB of ROM

4) Minimum 4KB of RAM

5) If possible JTAG (joint test action group) supportable.

The required specifications of the A/D Converter are:

1) Minimum 12 bit

2)16 channels

3) SPI interface

4) Operating frequency.

After doing Literature survey on various Micro-controller and A/D converter following 2 best solutions was proposed

1) **P89V51RD2**

Specification:

- 80C51 Central Processing Unit
- 5 V Operating voltage from 0 to 40 MHz
- 64kB of on-chip Flash program memory with ISP (In-System Programming) and IAP (In-Application Programming)
- Supports 12-clock (default) or 6-clock mode selection via software or ISP
- SPI (Serial Peripheral Interface) and enhanced UART
- PCA (Programmable Counter Array) with PWM and Capture/Compare functions

- Four 8-bit I/O ports with three high-current Port 1 pins (16 mA each)
- Three 16-bit timers/counters
- Programmable Watchdog timer (WDT)
- Eight interrupt sources with four priority levels
- Second DPTR register
- Low EMI mode (ALE inhibit)
- TTL- and CMOS-compatible logic levels

Problem Faced: - 1) RAM was less i.e. 1KB, we required minimum 4KB RAM

2) JTAG supportability was not there.

The above problem is solved by using Microchip 23K640 which has following specification

- 64K bits(8KB) SRAM
- 8 pin/TSSOP,8pin/SOIC
- -40 to 125 degree C
- 20MHz Operating frequency

AD7490:

It's a 12 bit analog to digital converter with16 channels

Other specifications are

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.7 V-5.25 V

- Low power at maximum throughput rates 5.4mW maximum at 870kSPS with 3V supplies 12.5mW maximum at 1MSPS with 5V supplies.
- 16 (single-ended) inputs with sequencer

By using ADuC7026 microcontroller there will be no need of using external ADC and External RAM

ADuC7026:

Following are the specification of arm microcontroller

- Analog I/O
  - Multichannel, 12-bit, 1 MSPS ADC Up to 16 ADC channels
  - Fully differential and single-ended modes 0 to VREF analog input range
  - 12-bit voltage output DACs Up to 4 DAC outputs available1
  - On-chip voltage reference
  - On-chip temperature sensor (±3°C)
  - Voltage comparator
- Microcontroller
  - ARM7TDMI core, 16-bit/32-bit RISC architecture
  - JTAG port supports code download and debug
- Clocking options
  - Trimmed on-chip oscillator (±3%)
  - External watch crystal

- External clock source up to 44 MHz
- 41.78 MHz PLL with programmable divider

- Memory
  - 62 kB flash/EE memory, 8 kB SRAM
  - In-circuit download, JTAG-based debug
  - Software triggered in-circuit reprogrammability
- On-chip peripherals
  - UART, 2 × I2C® and SPI® serial I/O
  - Up to 40-pin GPIO port1
  - 4 × general-purpose timers
  - Wake-up and watchdog timers (WDT)
  - Power supply monitor
  - Three-phase, 16-bit PWM generator
  - Programmable logic array (PLA)
  - External memory interface, up to 512 kB
- Power
  - Specified for 3 V operation
  - Active mode: 11 mA @ 5 MHz; 40 mA @ 41.78 MHz
- Packages and temperature range
  - From 40-lead 6 mm × 6 mm LFCSP to 80-lead LQFP1

- Fully specified for –40°C to +125°C operation

2.3 Temperature Sensors

Temperature sensors are divided into two types contact type and non-contact type.

Contact type Temperature Sensors:-

As the name suggest it is in contact with the object whose temperature we want to measure, they are different types of temperature sensors available in the market they are.

- Thermocouples
- Resistance temperature detectors(RTD)
- Thermistors
- Bi-metallic strip
- Semiconductor temperature sensors

Thermocouples:

Thermocouple works on the principle of seebeck effect. They are classified based on the two materials that make up the thermocouple. They consist of two junctions: cold junction and hot junction. The voltage developed between two junctions called seebeck voltage. Voltage is in the order of millivolts

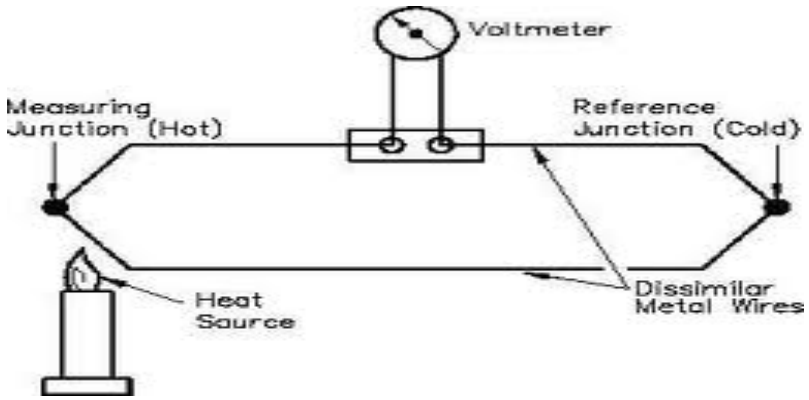


Figure 2. 2: Thermocouple

The voltage generated by the thermocouple is given by the equation:

$$V=S\times\Delta T$$

Where,

V=Voltage measured (V)

S=Seebeck Coefficient (V/°C)

ΔT=difference in temperature between two junctions

Hence the unknown temperature can be calculated using the equation,

$$T=T\ ref+V/S\ in\ ℃$$

Advantages

- Self-powered
- Simple in construction
- Wide Temperature range
- Wide Variety
- Inexpensive

Disadvantage

- Low voltage
- Less Stable
- Reference required

RTDs:

- They work on the principle of positive temperature coefficient
- RTDs are used to measure the temperature ranging from –

  196 to 482 **°C**

- Common resistance Materials for RTDs:
  - Platinum
  - Nickel
  - Copper
  - Balco
  - Tungsten

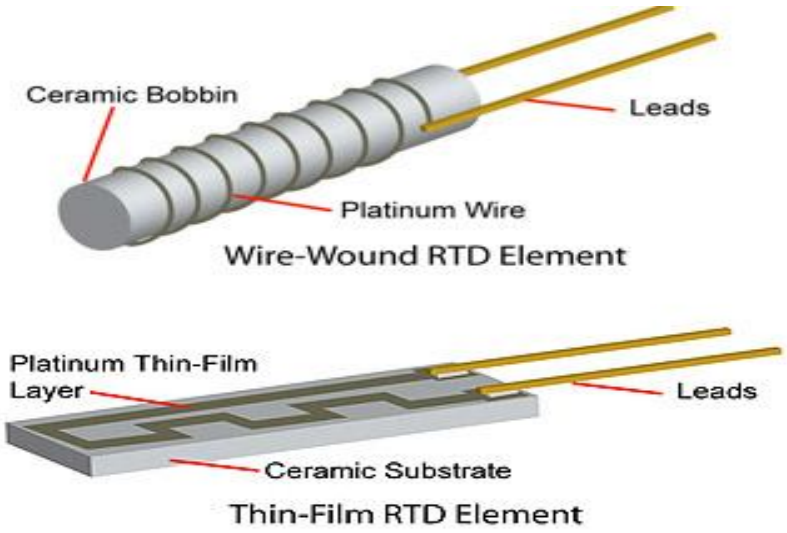


Figure 2. 3: RTD Element

- $R(T)=R0\times(1+a\times T+b\times T^2)$

R (T) = Resistance at temperature T

R0 = Resistance at Nominal Temperature

a and b are Calibration constants,

Where

$a=3.9692\times10^{-3}$ /°C

$b=-5.8495\times10^{-7}$/°C

The relationship between voltage and RTDs resistance is given by:

$V= (Vref\times R (T))/(R (0) +R (T))$

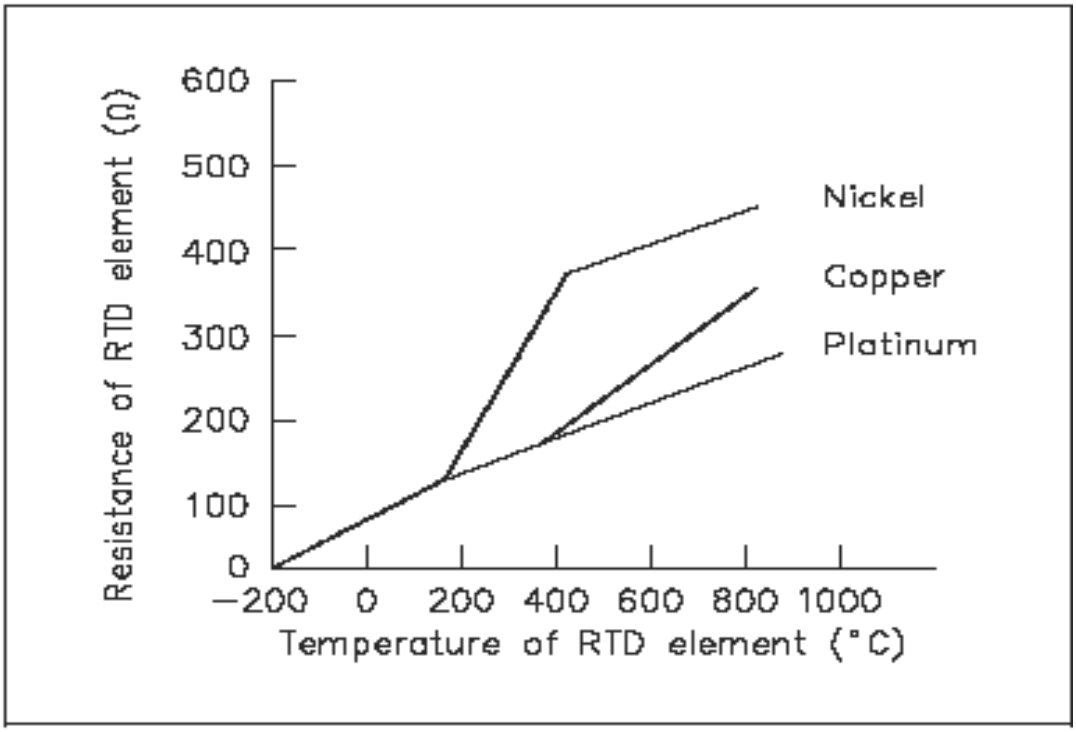


Figure 2. 4: Temperature characteristic of RTD for different element

Advantage

- Stable output for a long period of time
- Accurate reading over narrow temperature range
- Linear output

Disadvantages

- Smaller temperature range when compared to thermocouples
- No self-powered
- Self-heating

Thermistors:

- These are similar to RTDs
- These work on negative temperature coefficient
- These are made up of semiconductor devices
- Variation is non linear
- Thermistors are used to measure the temperatures ranging from -45to 260 °C

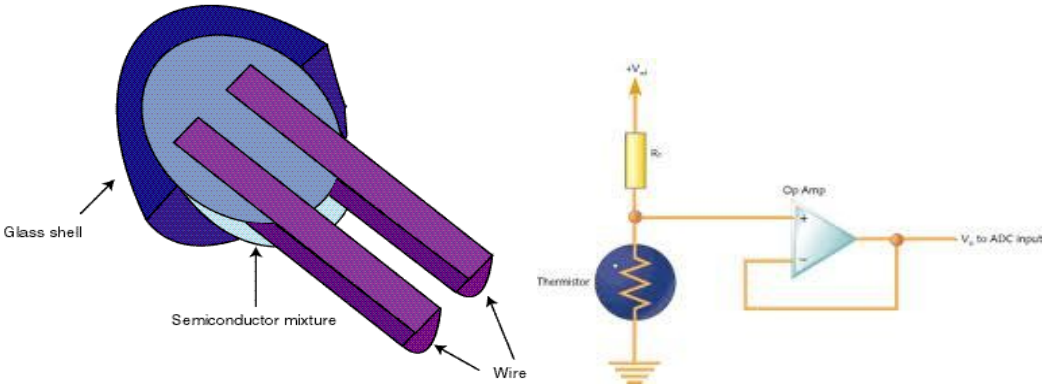


Figure 2. 5: Thermistor and its electrical equivalent circuit.

$R=R0\times e^{b(1/T-1/T0)}$

Where,

R =Resistance at temperature T (in deg.Kelvin)

R0=Resistance at an arbitrary reference

Temperature T0 in **°K**

b=Calibration constant (4600>b>3500 °K)

Advantage

- High output
- Fast response

Disadvantage

- Limited temperature range
- Not Self powered
- Self-heating

Bimetallic strip:

- A BI-metallic strip consists of two strips of different materials but of equal length
- These two strips are riveted together at different points along their lengths
  - welding process
  - Rivets
  - Bolts
  - Adhesive

Non-Contact type Temperature Sensors:

- Non-contact type temperature sensors are used to measure the temperature of an object without contact.
- The measurement devices, which require direct contact with the measured media
- Non-contact methods of temperature measurement are efficient when contact methods are impossible or impractical

- Non-contact type temperature sensor measure temperature by way of the infrared radiation of an object.
- Types of non-contact type sensors:

1. IR temperature sensor.
2. Optical pyrometers.

After doing research on different types of temperature sensor RTD (PT100) got selected because of following condition:

- Very Accurate and Stable
- Reasonably Linear
- Good Repeatability

CHAPTER 3 HARDWARE SETUP

3.1. Signal Conditioning Circuit

After selecting temperature sensor RTD (PT100), Signal conditioning circuit is designed. The acronym “RTD” is derived from the term “Resistance Temperature Detector”. The most stable, linear and repeatable RTD is made of platinum metal. The temperature coefficient of the RTD element is positive and almost constant. Typical RTD elements are specified with 0°C values of 50, 100, 200, 500, 1000 or 2000Ω. Of these options, the 100Ω platinum RTD is the most stable over time and linear over temperature. The RTD element requires a current excitation. If the magnitude of the current source is too high, the element will dissipate power and start to self-heat. Consequently, care should be taken to insure that less than 1 mA of current is used to excite the RTD element.

An approximation to the platinum RTD resistance change over temperature can be calculated by using the constant a = 0.00385Ω/Ω/°C (European curve, ITS-90). This constant is easily used to estimate the absolute resistance of the RTD at temperatures between -100°C and +200°C (with a nominal error smaller than 3.1°C).

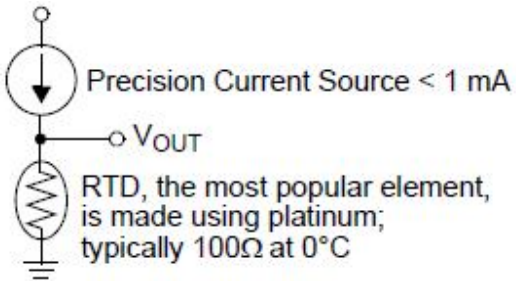


Figure 3. 1: RTD Temperature-sensing Elements use Current Excitation**.**

$$RTD(T) \approx RTD(0)(1 + T \times \alpha) \quad (1)$$

Where:

RTD (T) = the RTD element's resistance (Ω) at Temperature *T*

RTD (0) = the RTD element's resistance (Ω) at Temperature 0°C

T = the RTD element's temperature (°C),

$\alpha = 0.00385\ \Omega/\Omega/°C$

If a higher accuracy temperature measurement is required, or a greater temperature range is measured, the standard formula below (Calendar-Van Dusen Equation) can be used in a calculation in the controller engine or be used to generate a look-up table.

$$RTD(T) = RTD(0)(1 + AT + BT^2 + CT^3(T - 100)) \quad (2)$$

Where:

RTD (T) = the RTD element's resistance at T (Ω),

RTD0 = the RTD element's resistance at 0°C (Ω),

T = the RTD element's temperature (°C) and

A, B, C = are constants derived from resistance measurements at multiple temperatures.

The ITS-90 standard values are:

RTD (0) = 100Ω

$A = 3.9083 \times 10^{-3}$ °C-1

$B = -5.775 \times 10^{-7}$ °C-2

$$C = -4.183 \times 10^{-12}\ °C\text{-}4,\ T < 0°C$$

$$= 0,\ T \geq 0°C$$

$V_{OUTA1} = V_{REFGA1} + V_{OUTA2}$

Where:

V_{OUTA1} = A1's output voltage

V_{OUTA2} = A2's output voltage

V_{REF} = Reference voltage at the input

GA1 = Differential Gain

= 1V/V

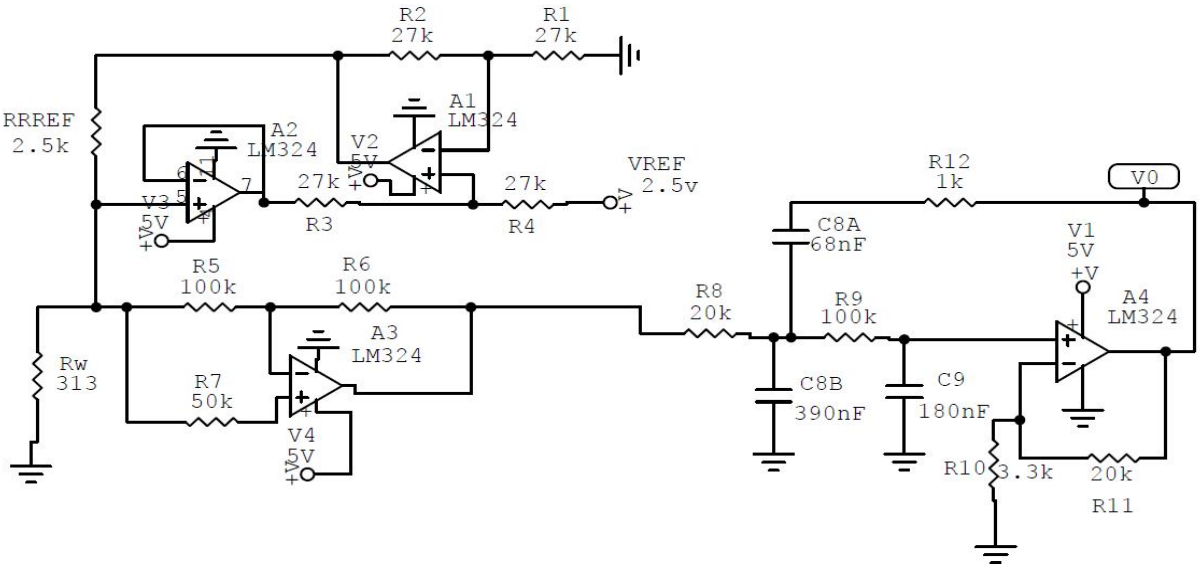


Figure 3. 2: RTD element measure temperatures from 0°C to 300°C range

Changes in resistance of the RTD element over temperature are usually digitized through an A/D conversion, as shown in Figure 9. The current excitation circuit excites the RTD element. The magnitude of the current source can be : tuned to 1 mA or less by adjusting RREF. The voltage drop across the RTD element is sensed by

A3, then gained and filtered by A4. With this circuit, a 3-wire RTD element is selected. This configuration minimizes errors due to wire resistance and wire resistance drift over temperature. In this circuit, the RTD element equals 100Ω at 0°C. If the RTD is used to sense temperature over the range of -200°C to 600°C, the resistance produced by the RTD would be nominally between 18.5Ω and 313.7Ω, giving a voltage across the RTD between 18.5 mV and 313.7 mV. Since the resistance range is relatively low, wire resistance and wire resistance change over temperature can skew the measurement of the RTD element. Consequently, a 3- ire RTD device is used to reduce these errors.

The errors contributed by the wire resistances, RW1 and RW3, are subtracted from the signal with op amp A3. In this configuration, R1 and R2 are equal and are relatively high. The value of R1 is selected to ensure that the leakage currents through the resistor do not introduce errors to the current in the RTD element.

The transfer function of this portion of the circuit is

EQUATION 4:

$$V_{RREF} = V_{OUTA1} - V2$$

Where:

V2 = Voltage at A2's input

VRREF = Voltage across RREF

EQUATION 5:

$$I_{RREF} = V_{RREF} / R_{REF}$$

IRREF = 1 mA

EQUATION 6:

$$V_{OUTA3} = (V_{IN} - V_{W1})(1 + R6/R5) - V_{IN}(R6/R5)$$

Where:

VIN = VW1+VRTD+VW3,

VWx= the voltage drop across the wires to

and from the RTD and

VOUTA3 = the voltage at the output of A3

EQUATION 7:

VOUTA3 = VRTD

Where:

R5 = R6

RW1 = RW3

The voltage signal at the output of A3 is filtered with a 2nd order, low pass filter created with A4, R8, C8A, C8B, R9 and C9. It is designed to have a Bessel response and a bandwidth of 10 Hz. R10 and R11 set a gain of 7.47 V/V. It reduces noise and prevents aliasing of higher frequency signals. This filter uses a Sallen-Key topology specially designed for high gain. The capacitor divider formed by C8A and C8B improve this filter's sensitivity to component variations; the filter can be unproduceable without this improvement. R12 isolates A4's output from the capacitive load formed by the series connection of C8A and C8B; it also improves performance at higher frequencies.

The voltage at A4's output is nominally between 0.138V and 2.343V, which is less than VREF (2.5V).

3.2 Power Supply Circuit

The +24VDC supply is regulated using the Linear Voltage Regulator TPS5045 and TPS70358. The 3.3 V, 2.5V regulator output is used to drive the digital side of

the board directly. The 3.3 V and 5V supply is also filtered and then used to supply the analog side of the board.

When on, the LED (D3) indicates that a valid 3.3 V supply is being driven from the regulator circuit. All active components are decoupled with 0.1 μF,16VDC at device supply pins to ground.

3.3 ARM7 Microcontroller Circuit

3.3.1 Crystal Circuit

The board is fitted with a 32.768 kHz crystal, from which the on-chip PLL circuit can generate a 41.78 MHz clock.

3.3.2 Reset Push Buttons

A reset push button is provided to allow the user to reset the part manually. When the button is pushed, the reset pin of the ADuC7026 is pulled to DGND. Because the reset pin on the ADuC7026 is Schmidt triggered internally, there is no need to use an external Schmidt trigger on this pin.

3.3.3 Analog I/O Connections

All analog I/O connections are brought out on Header J3.

ADC0 and ADC1 are buffered using an AD8606 to evaluate single-ended and pseudo differential mode. A potentiometer can be connected to ADC0 (buffered).

ADC3 and ADC4 can be buffered with a single-ended to differential op amp on-board, with the AD8132 used to evaluate the ADC in fully differential mode.

ADC2 and ADC5 to ADC11 are not buffered.

DAC1 can be used to control the brightness of the LED D1, when connected via the S1 switch

3.4 Output Driver Circuit

The output of ADuC7026 is 3.3V, so in order to avoid load on microcontroller ULN2803 is being used in our circuit.

i. U20 is used to drive relay circuit at the output which is connected as input to the CNC machine.

ii. U22 is used to generate 5V output from 3.3V which is a input from ADuC7026 which is given as input to second PCB Circuit board.

iii. U21 is used to generate 3.3V from 5V output of second PCB circuit board.

ULN2803 specifications are as follows

ULN2803 is High Voltage, High Current Darlington array.

Featuring continuous load current ratings to 500 mA for each of the drivers, the Series ULN28xxA/LW and ULQ28xxA/LW high voltage, high-current Darlington arrays are ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads. Typical power loads totaling over 260 W (350 mA x 8, 95 V) can be controlled at an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters. All devices feature open-collector outputs with integral clamp diodes.

The ULx2803A, ULx2803LW, ULx2823A, and ULN2823LWhave series input resistors selected for operation directly with 5 V TTL or CMOS. These devices will handle numerous interface needs particularly those beyond the capabilities of standard logic buffers. The ULx2804A, ULx2804LW, ULx2824A, and ULN2824LWhave series input resistors for operation directly from 6 V to 15

VCMOS or PMOS logic outputs. The ULx2803A/LW and ULx2804A/LW are the standard Darlington arrays. The outputs are capable of sinking 500 mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The ULx2823A/LW and ULx2824A/LW will withstand 95 V in the OFF state.

These Darlington arrays are furnished in 18-pin dual in-line plastic packages (suffix ‘A’) or 18-lead small-outline plastic packages (suffix ‘LW’). All devices are pinned with outputs opposite inputs to facilitate ease of circuit board layout. Prefix ‘ULN’ devices are rated for operation over the temperature range of -20°C to +85°C; prefix‘ULQ’ devices are rated for operation to -40°C.

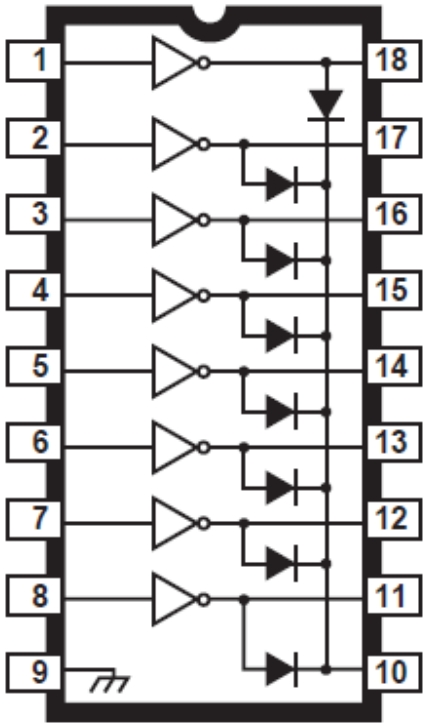


Figure 3. 3:ULN2803A pin diagram

Features

1. TTL, DTL, PMOS, or CMOS Compatible Inputs
2. Output Current to 500 mA
3. Output Voltage to 95 V
4. Transient-Protected Outputs
5. Dual In-Line Package or Wide-Body Small-Outline Package

3.5 Emulation Interface

Nonintrusive emulation and download are possible on the ADuC7026, via JTAG, by connecting a JTAG emulator to the J4 connector

JTAG is also widely used for IC debug ports. In the embedded processor market, essentially all modern processors support JTAG when they have enough pins. Embedded systems development relies on debuggers talking to chips with JTAG to perform operations like single stepping and break pointing. Digital electronics products such as cell phones or a wireless access point generally have no other debug or test interfaces.

3.5.1 Electrical characteristics

A JTAG interface is a special four/five-pin interface added to a chip, designed so that multiple chips on a board can have their JTAG lines daisy-chained together if specific conditions are met,[4] and a test probe need only connect to a single "JTAG port" to have access to all chips on a circuit board.

The connector pins are

1. **TDI** (Test Data In)
2. **TDO** (Test Data Out)
3. **TCK** (Test Clock)

4. **TMS** (Test Mode Select)

5. **TRST** (Test Reset) optional.

Test reset signal is not shown in the image.

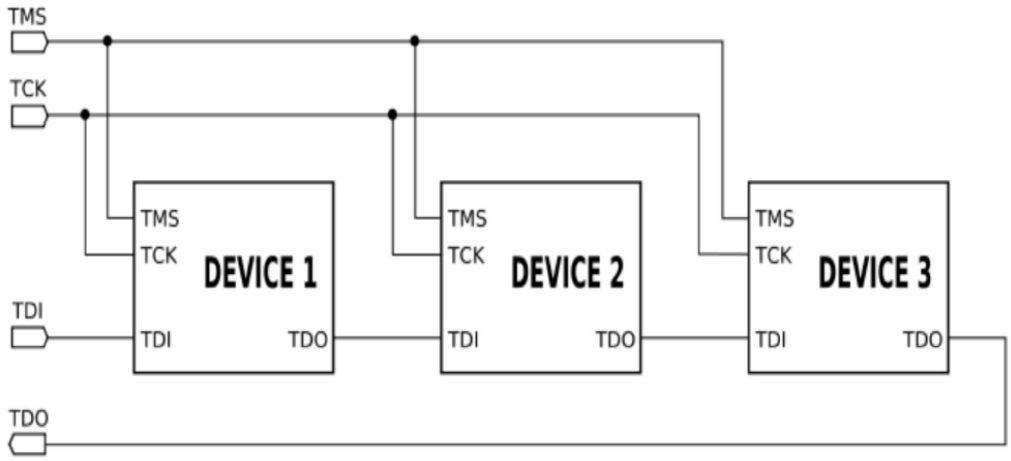


Figure 3. 4: JTAG Connections to more than one device

Since only one data line is available, the protocol is serial. The clock input is at the TCK pin. Clocking changes on TMS steps through a standardized JTAG state machine. The JTAG state machine can reset, access an instruction register, or access data selected by the instruction register.

One bit of data is transferred in and out per TCK clock pulse at the TDI and TDO pins, respectively. Different instructions can be loaded. Instructions for typical ICs might read the chip ID, sample input pins, drive (or float) output pins, manipulate chip functions, or bypass (pipe TDI to TDO to logically shorten chains of multiple chips). The operating frequency of TCK varies depending on all chips in the chain (lowest speed must be used), but it is typically 10-100 MHz (100-10 ns per bit).

The TRST pin is an optional active-low reset to the test logic - usually asynchronous, but sometimes synchronous, depending on the chip. If the pin is not

available, the test logic can be reset by switching to the reset state synchronously, using TCK and TMS. Note that resetting test logic doesn't necessarily imply resetting anything else. There are generally some processor-specific JTAG operations which can reset all or part of the chip being debugged.

As with any clocked signal, data presented to TDI must be valid for some chip-specific *Setup* time before and *Hold* time after the relevant (here, rising) clock edge. TDO data is valid for some chip-specific time after the falling edge of TCK. In short, there are some constraints on signal timings.

TCK frequencies vary based on chip, board, and adapter capabilities and state. One chip might support a 40 MHz JTAG clock, but only if it's using a 200 MHz clock for non-JTAG operations; and it might need to use a much slower clock when it's in a low power mode. Accordingly, some JTAG adapters support *adaptive clocking* using an RTCK (Return TCK) signal. Faster TCK frequencies are most useful when JTAG is used to transfer lots of data, such as when storing a system image into NAND flash.

JTAG platforms often add signals to the handful defined by the IEEE 1149.1 specification. A System Reset (SRST) signal is quite common, letting debuggers reset the whole system, not just the parts with JTAG support. Sometimes there are event signals used to trigger activity by the host or by the device being monitored through JTAG; or, perhaps, additional control lines.

Even though few consumer products provide an explicit JTAG port connector, the connections are often available on the printed circuit board as a remnant from development prototyping and/or production. When exploited, these connections often provide the most viable means for reverse engineering.

3.5.2 Communications model

In JTAG, devices expose one or more *test access ports* (TAPs). The picture above shows three TAPs, which might be individual chips or might be modules inside one

chip. A daisy chain of TAPs is called a *scan chain*, or (loosely) a target. Scan chains can be arbitrarily long, but in practice twenty TAPs is unusually long[*citation needed*].

To use JTAG, a host is connected to the target's JTAG signals (TMS, TCK, TDI, TDO, etc.) through some kind of *JTAG adapter*, which may need to handle issues like level shifting and galvanic isolation. The adapter connects to the host using some interface such as USB, PCI, Ethernet, and so forth.

CHAPTER 4 SOFTWARE DEVELOPMENTS

4.1 OVERVIEW OF THE ARM7TDMI CORE

The ARM7 core is a 32-bit Reduced Instruction Set Computer (RISC). It uses a single 32-bit bus for instruction and data. The length of the data can be 8, 16 or 32 bits and the length of the instruction word is 32 bits.

The ARM7TDMI is an ARM7 core with 4 additional features:

- **T** support for the Thumb (16 bit) instruction set.
- **D** support for debug
- **M** support for long multiplies
- **I** include the Embedded ICE module to support embedded system debugging.

4.1.1. Thumb mode (T)

An ARM instruction is 32-bits long. The ARM7TDMIprocessor supports a second instruction set that has been compressed into 16-bits, the Thumb instruction set. Faster execution from 16-bit memory and greater code density can usually be achieved by using the Thumb instruction set instead of the ARM instruction set, which makes the ARM7TDMI core particularly suitable for embedded applications.

However the Thumb mode has two limitations:

- Thumb code usually uses more instructions for the same job, so ARM code is usually best for maximizing the performance of the time-critical code.
- The Thumb instruction set does not include some instructions that are needed for exception handling, so ARM code needs to be used for exception handling.

See ARM7TDMI User Guide for details on the core architecture, the programming model and both the ARM and ARM Thumb instruction sets.

4.1.2. Long Multiply (M)

The ARM7TDMI instruction set includes four extra instructions which perform 32-bit by 32-bit multiplication with64-bit result and 32-bit by 32-bit multiplication-accumulation (MAC) with 64-bit result.

4.1.3. Embedded ICE (I)

Embedded ICE provides integrated on-chip support for the core. The Embedded ICE module contains the breakpoint and watch point registers which allow code to be halted for debugging purposes. These registers are controlled through the JTAG test port.

When a breakpoint or watch point is encountered, the processor halts and enters debug state. Once in a debug state, the processor registers may be inspected as well as the Flash/EE, the SRAM and the Memory Mapped Registers.

4.1.4. Exceptions

ARM supports five types of exceptions, and a privileged processing mode for each type. The five types of exceptions are:

- Normal interrupt or IRQ. It is provided to service general purpose interrupt handling of internal and external events.
- Fast interrupt or FIQ. It is provided to service data transfer or communication channel with low latency. FIQ has priority over IRQ
- Memory abort.
- Attempted execution of an undefined instruction.
- Software interrupt (SWI) instruction which can be used to make a call to an operating system.

Typically the programmer will define interrupts as IRQ but for higher priority interrupt, i.e. faster response time, the programmer can define interrupt as FIQ.

4.1.5. ARM Registers

ARM7TDMI has a total of 37 registers, of which 31 are general purpose registers and six are status registers. Each operating mode has dedicated banked registers.

When writing user-level programs, 15 general purpose 32-bitregisters (r0 to r14), the program counter (r15) and the current program status register (CPSR) are usable. The remaining registers are used only for system-level programming and for exception handling.

When an exception occurs, some of the standard registers are replaced with registers specific to the exception mode. All exception modes have replacement banked registers for the stack pointer (r13) and the link register (r14) as represented in Figure 12. The fast interrupt mode has more registers (8 to 12) for fast interrupt processing, so that the interrupt processing can begin without the need to save or restore these registers and thus save critical time in the interrupt handling process.

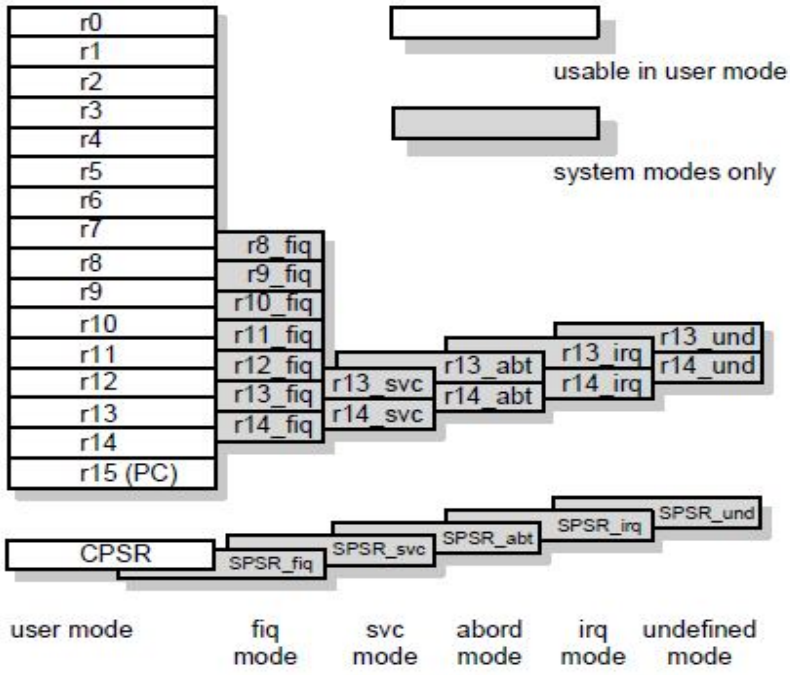


Figure 4. 1: Register Organisation

4.1.6. Interrupt latency

The worst case latency for an FIQ consists of the longest time the request can take to pass through the synchronizer, plus the time for the longest instruction to complete (the longest instruction is an LDM) which loads all the registers including the PC, plus the time for the data abort entry, plus the time for FIQ entry. At the end of this time, the ARM7TDMI will be executing the instruction at 0x1C (FIQ interrupt vector address). The maximum total time are 41 processor cycles, which is just over 909 nanoseconds in a system using a continuous 45MHz processor clock. The maximum IRQ latency calculation is similar, but must allow for the fact that FIQ has higher priority and could delay entry into the IRQ handling routine for an arbitrary length of time.

The minimum latency for FIQ or IRQ interrupts is five cycles in total which consists of the shortest time the request can take through the synchronizer plus the time to enter the exception mode.

Note that the ARM7TDMI will always be run in ARM (32-bit) mode when in privileged modes, i.e. when executing interrupt service routines.

4.2 OSCILLATOR AND PLL - POWER CONTROL

The ADuC702x integrates a 32.768 kHz oscillator, a clock divider and a PLL. The PLL locks onto a multiple (1376) of the internal oscillator to provide a stable 45MHz clock for the system. The core can operate at this frequency, or at binary submultiples of it, to allow power saving. The default core clock is the PLL clock divided by 8 (CD = 3) or 5MHz. The core clock frequency can be output on the ECLK pin as described Figure13. A power down mode is available on the ADuC702x.

The operating mode, clocking mode and programmable clock divider are controlled via two MMRs, PLLCON and POWCON.PLLCON controls operating mode of the clock system while POWCON controls the core clock frequency and the power down mode.

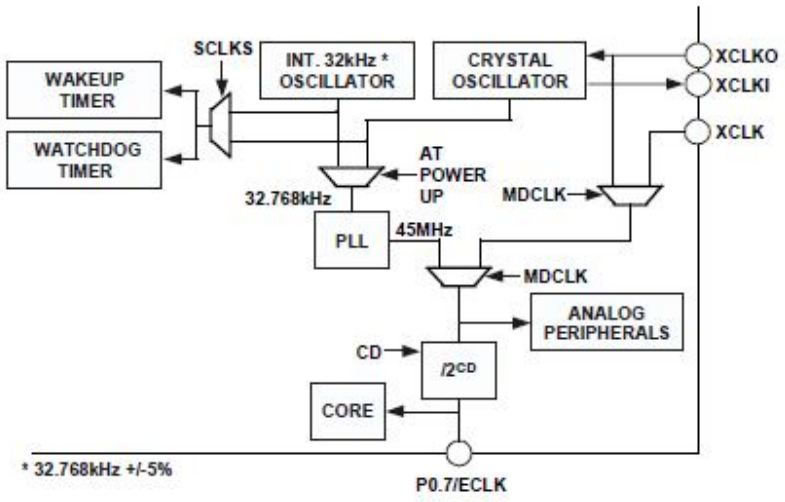


Figure 4. 2: Clocking system

A certain sequence has to be followed to write in the PLLCON and POWCON registers, to prevent accidental programming.

4.3 ADC CIRCUIT INFORMATION

The Analog Digital Converter (ADC) incorporates a fast, multichannel, 12-bit ADC. It can operate from 2.7V to 3.6V supplies and is capable of providing a throughput of up to 1MSPS when the clock source is 45MHz. This block provides the user with multi-channel multiplexer, differential track-and-hold, on-chip reference and ADC.

The ADC consists of a 12-bit successive-approximation converter based around two capacitor DACs. It can operate in one of three different modes, depending on the input signal configuration:

- *fully differential mode*, for small and balanced signals
- *single-ended mode*, for any single-ended signals
- *Pseudo-differential mode*, for any single-ended signals, taking advantage of the common mode rejection offered by the pseudo differential input.

The converter accepts an analog input range of 0 to VREF when operating in single-ended mode or pseudo-differential mode. In fully differential mode, the input signal must be balanced around a common mode voltage VCM, in the range 0V to AVDD and with maximum amplitude of 2 VREF (see Figure 14).

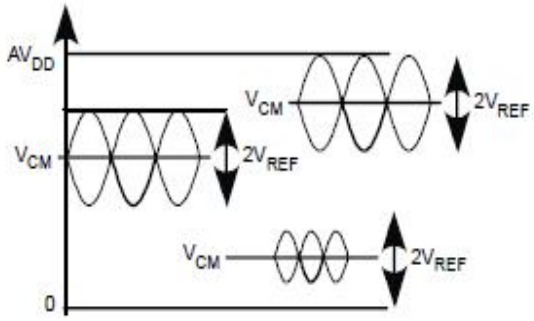


Figure 4. 3: Examples of balanced signals for fully differential mode

A high precision, low drift and factory calibrated 2.5 V reference is provided on-chip. An external reference cans also be connected as described later.

Single or continuous conversion modes can be initiated in software. An external CONVSTART pin, an output generated from the on-chip PLA or a Timer1 or a Timer2 overflow can also be used to generate a repetitive trigger for ADC conversions.

A voltage output from an on-chip bandgap reference proportional to absolute temperature can also be routed through the front end ADC multiplexer (effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

4.3.1. ADC TRANSFER FUNCTION

In pseudo-differential or single-ended mode, the input range is0 V to VREF. The output coding is straight binary in pseudo differential and single-ended modes with 1 LSB = FS/4096 or2.5 V/4096 = 0.61 mV or 610 µV when VREF = 2.5 V. The ideal code transitions occur midway between successive integer LSB values (i.e. 1/2 LSB, 3/2 LSBs, 5/2 LSBs. . . FS –3/2 LSBs). The ideal input/output transfer characteristic is shown in Figure 15.

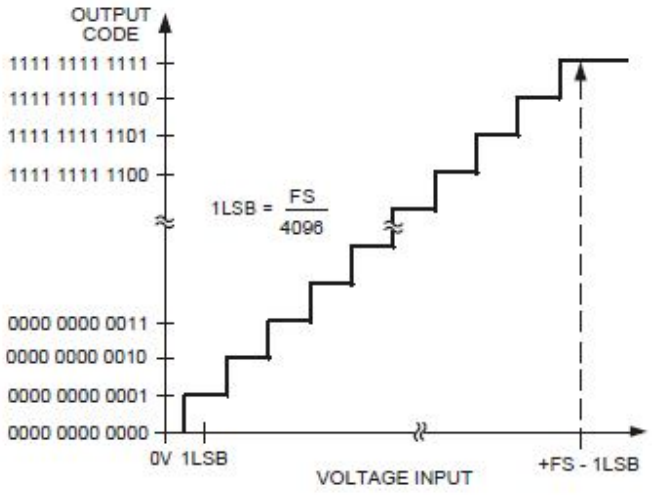


Figure 4. 4: ADC transfer function in pseudo differential mode or single-ended Mode

4.3.2. TYPICAL OPERATION

Once configured via the ADC control and channel selection registers, the ADC will convert the analog input and provide a12-bit result in the ADC data register.

The top 4 bits are the sign bits and the 12-bit result is placed from bit 16 to 27 as shown in Figure 16. Again, it should be noted that in fully differential mode, the result is represented in two's complement format and in pseudo differential and single ended mode, the result is represented in straight binary format.

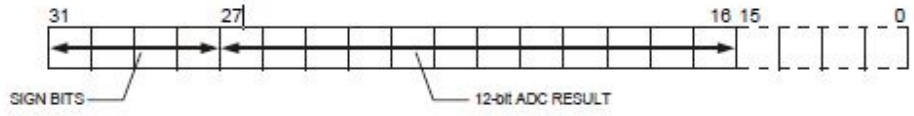


Figure 4. 5: ADC Result Format

4.3.3. ADC MMRS interface

The ADC is controlled and configured via a number of MMRs that are listed below and described in detail in the following:

- **ADCCON:** ADC Control Register allows the programmer to enable the ADC peripheral, to select the mode of operation of the ADC, either Single-ended, pseudo-differential or fully differential mode and the conversion type.
- **ADCCP:** ADC positive Channel selection Register
- **ADCCN:** ADC negative Channel selection Register
- **ADCSTA:** ADC Status Register indicates when an ADC conversion result is ready. The ADCSTA register contains only one bit, bit (bit 0), representing the status of the ADC. This bit is set at the end of an ADC conversions generating an ADC interrupt; it is cleared automatically by reading the ADCDAT MMR. When the ADC is performing a conversion, the status of the ADC can be read externally via the ADCBusy pin. This pin is high during a conversion. When the conversion is finished, ADCBusy goes back low. This information can be available on P0.3 (see chapter on GPIO) if enabled in ADCCON register.

- **ADCDAT:** ADC Data Result Register, hold the 12-bit ADC result as shown Figure 10
- **ADCRST:** ADC Reset Register. Resets all the ADC registers to their default value.
- **ADCOF:** Offset calibration register. 10-bit register
- **ADCGN:** Gain calibration register. 10-bit register

4.3.4. CONVERTER OPERATION

The ADC incorporates a successive approximation (SAR) architecture involving a charge-sampled input stage. This architecture is described below for the three different modes of operation.

Single-ended mode

In Single-ended mode, SW2 is always connected internally to ground. The VIN- pin can be floating. The input signal range on VIN+ is 0V to VREF.

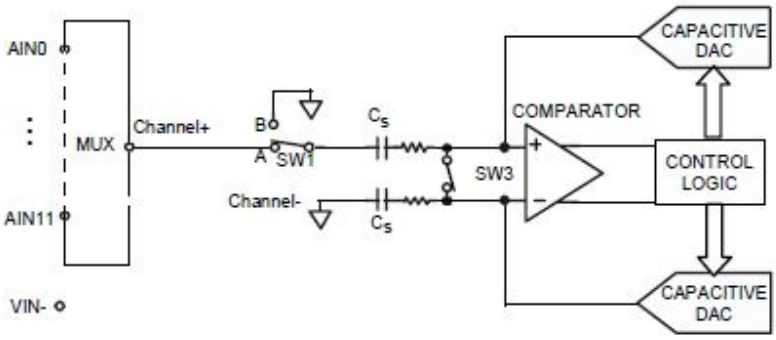


Figure 4. 6: ADC in single-ended mode

4.3.5. ADC CALIBRATION

System calibration or device calibration are performed in software. Two 10-bit registers are available for calibration, ADCOF and ADCGN.

For offset error correction, either an external pin must be tied to AGND (system calibration) or the internal AGND channel must be selected (device calibration). A software loop must be implemented to tweak the value in ADCOF register each time until the transition of ADCDAT reads code 0 to 1. Offset error correction is done digitally and has a resolution of 0.25 lsb and a range of +/- 3.125% of VREF.

For gain error correction, either an external pin must be tied to VREF (system calibration) or the internal reference channel must be selected (device calibration). A software loop must be implemented to tweak the value in ADCGN register each time until the transition of ADCDAT reads code 4094 to 4095.Similar to the offset calibration, the gain calibration resolution is 0.25 lsb with a range of +/- 3% of VREF.

4.3.5. TEMPERATURE SENSOR

The ADuC702x provides a voltage output from an on-chip bandgap reference proportional to absolute temperature. It can also be routed through the front end ADC multiplexer(effectively an additional ADC channel input) facilitating an internal temperature sensor channel, measuring die temperature to an accuracy of ±3°C.

4.3.5. BANDGAP REFERENCE

The ADuC702x provides an on-chip bandgap reference of 2.5V, which can be used for the ADC and for the DAC. This internal reference also appears on the VREF pin. When using the internal reference, a capacitor of 0.47μF must be connected from the external VREF pin to AGND, to ensure stability and fast response during ADC conversions. This reference can also be connected to an external pin (VREF) and used as a reference for other circuits in the system. An external buffer would be required because of the low drive capability of the VREF output. Aprogrammable option also allows an external reference input on the VREF pin. The bandgap reference interface consists on a 8-bit MMR,REFCON.

4.4 PROCESSOR REFERENCE PERIPHERALS

4.4.1. INTERRUPT SYSTEM

There are 24 interrupt sources on the ADuC702x which are controlled by the Interrupt Controller. Most interrupts are generated from the on-chip peripherals like ADC, UART, etc. and two additional interrupt sources are generated from external interrupt request pins, XIRQ0 and XIRQ1. TheARM7TDMI CPU core will only recognize interrupts as one of two types, a normal interrupt request IRQ and a fast interrupt request FIQ. All the interrupts can be masked separately.

The control and configuration of the interrupt system is managed through nine interrupt-related registers, four dedicated to IRQ, four dedicated to FIQ. An additional MMR is used to select the programmed interrupt source. The bits in each IRQ and FIQ register represent the same interrupt source

IRQ

The IRQ is the exception signal to enter the IRQ mode of the processor. It is used to service general purpose interrupt handling of internal and external events.

The four 32-bit registers dedicated to IRQ are:

- **IRQSIG**, reflects the status of the different IRQ sources. If a peripheral generate an IRQ signal, the corresponding bit in the IRQSIG will be set, otherwise it is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read-only.
- **IRQEN**, provides the value of the current enable mask. When bit is set to 1, the source request is enabled to create an IRQ exception. When bit is set to 0, the source request is disabled or masked which will not create an IRQ exception.
- **IRQCLR**, (write-only register) allows clearing the IRQEN register in order to mask an interrupt source. Each bit set to 1 will clear the corresponding bit in the IRQEN register without affecting the remaining bits. The pair of registers

IRQEN and IRQCLR allows independent manipulation of the enable mask without requiring an atomic read-modify write.

- **IRQSTA**, (read-only register) provides the current enabled IRQ source status. When set to 1 that source should generate an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine. All 32 bits are logically ORed to create the IRQ signal to the ARM7TDMI core.

FIQ

The FIQ (Fast Interrupt reQuest) is the exception signal to enter the FIQ mode of the processor. It is provided to service data transferor communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface providing the second level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ, FIQSIG, FIQEN, FIQCLR and FIQSTA. Bit 31 to 1 of FIQSTA are logically ORed to create the FIQ signal to the core and the bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR will not allow an interrupt source to be enabled in both IRQ and FIQ masks. A bit set to ‘1’in FIQEN will, as a side-effect, clear the same bit in IRQEN. A bit set to ‘1’ in IRQEN will, as a side-effect, clear the same bit in FIQEN. An interrupt source can be disabled in both IRQEN and FIQEN masks.

Programmed interrupts

As the programmed interrupts are non-mask-able, they are controlled by another register, SWICFG, which write into both IRQSTA and IRQSIG registers or/and FIQSTA and FIQSIG registers at the same time.

The 32-bit register dedicated to software interrupt is SWICFG. This MMR allows the control of programmed source interrupt.

Note that any interrupt signal must be active for at least the equivalent of the interrupt latency time, to be detected by the interrupt controller and to be detected by user in the IRQSTA/FIQSTA register.

4.4.2. TIMERS

The ADuC702x has four general purpose Timer/Counters:

- Timer0,
- Timer1,
- Timer2 or Wake-up Timer,
- Timer3 or Watchdog Timer.

The four timers in their normal mode of operation can be either free-running or periodic.

- In free-running mode the counter decrements/increments from the maximum/minimum value until zero/full scale and starts again at the maximum /minimum value.
- In periodic mode the counter decrements/increments from the value in the Load Register(TxLD MMR,) until zero/full scale and starts again at the value stored in the Load Register.

The value of a counter can be read at any time by accessing its value register (TxVAL). Timers are started by writing in the Control register of the corresponding timer (TxCON).

In normal mode, an IRQ is generated each time the value of the counter reaches zero, if counting down, or full-scale, if counting up. An IRQ can be cleared by writing any value to Clear register of the particular timer (TxCLRI).

Timer0 – RTOS timer

Timer0 is a general purpose 16-bit count-down timer with aprogrammable prescaler. The prescaler source is the core clock frequency and can be scaled by factors of 1, 16 or 256.

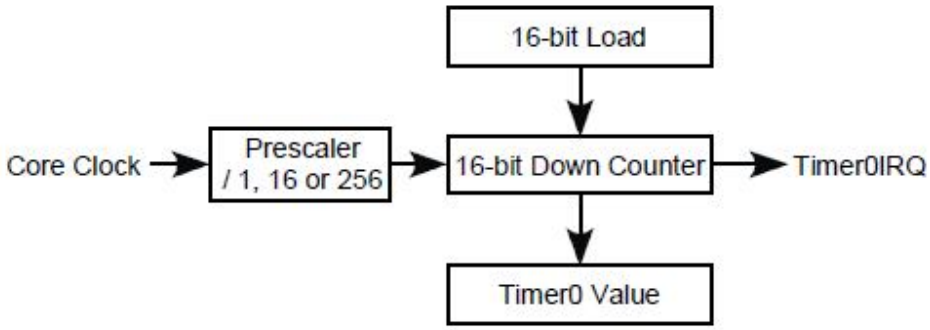


Figure 4. 7: Timer 0 block diagram

Timer0 interface consists in four MMRS:

- **T0LD** and **T0VAL** are 16-bit registers (bit 0 to 15) and hold 16-bit unsigned integers. T0VAL is read-only.
- **T0CLRI** is an 8-bit register. Writing any value to this register will clear the interrupt
- **T0CON** is the configuration MMR.

Timer1

Timer1 is a 32-bit general purpose timer, count-down or countup,with a programmable prescaler. The prescaler source can be the 32 kHz Oscillator, the core clock frequency, or an external GPIO, P1.0 or P0.6. This source can be scaled by a factor of 1,16, 256 or 32768.

The counter can be formatted as a standard 32-bit value or as Hours: Minutes: Seconds: Hundreths.

Timer1 has a capture register (T1CAP), which can be triggered by a selected IRQ source initial assertion. This feature can be used to determine the assertion of an event with more accuracy than the precision allowed by the RTOS timer at the time the IRQ is serviced.

Timer 1 can be used to start ADC conversions as shown in theblock diagram Figure 19.

Timer1 interface consists in five MMRS:

- **T1LD**, **T1VAL** and **T1CAP** are 32-bit registers and hold 32-bit unsigned integers. T1VAL and T1CAP are read-only.
- **T1CLRI** is an 8-bit register. Writing any value to this register will clear the timer1 interrupt.
- **T1CON** is the configuration MMR.

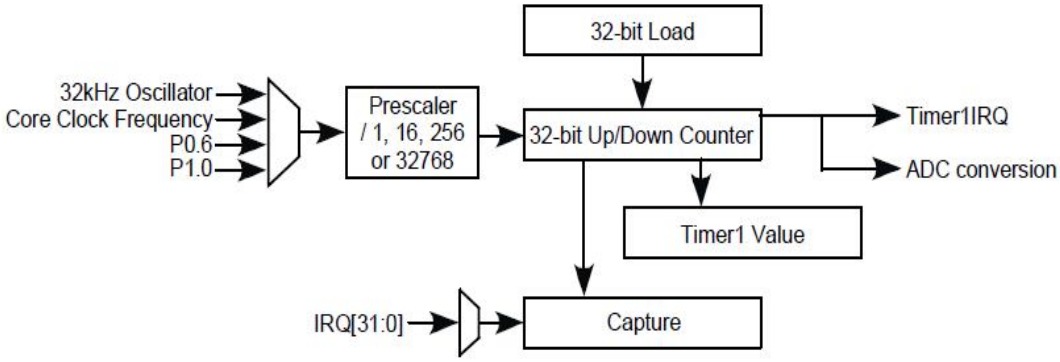


Figure 4. 8: Timer 1 block diagram

Timer2 - Wake-Up Timer

Timer2 is a 32-bit wake-up timer, count-down or count-up, with a programmable prescaler. It is clocked directly by the internal 32.768 kHz oscillator. The wake-up timer will continue to run when the core clock is disabled. The clock source cans be scaled by a factor of 1, 16, 256 or 32768.

The counter can be formatted as plain 32-bit value or as Hours: Minutes: Seconds: Hundreths.

Timer 2 can be used to start ADC conversions as shown in the block diagram Figure 20.

Timer2 interface consists in four MMRS:

- **T2LD** and **T2VAL** are 32-bit registers and hold 32-bit unsigned integers. T2VAL is read-only.
- **T2CLRI** is an 8-bit register. Writing any value to this register will clear the timer2 interrupt.

- **T2CON** is the configuration MMR.

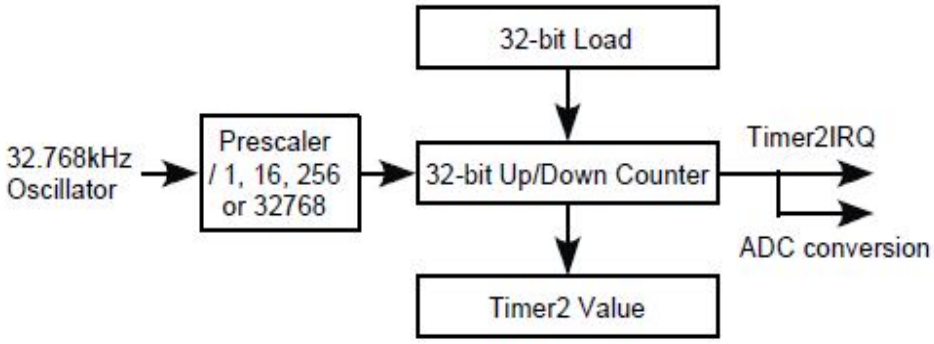


Figure 4. 9: Timer 2 block diagram

Timer3 - Watchdog Timer

Timer3 has two modes of operation, normal mode and watchdog mode. The Watchdog timer is used to recover froman illegal software state. Once enabled it requires periodic servicing to prevent it from forcing a reset of the processor.

Normal mode*:*

The Timer3 in normal mode is identical to Timer0 except for the clock source and the count-up functionality. The clock source is 32 kHz from the PLL and can be scaled by a factor of 1, 16 or 256.

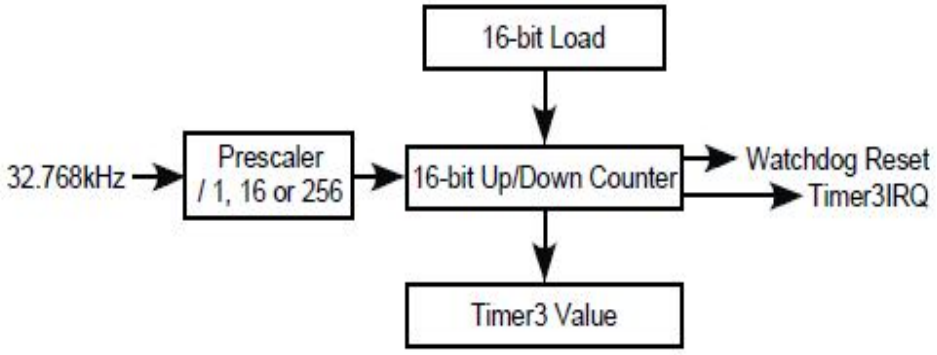


Figure 4. 10: Timer 3 block diagram

Watchdog mode:

Watchdog mode is entered by setting bit 5 in T3CON MMR.Timer3 decrements from the value present in T3LD Register until zero. T3LD is used as timeout. The timeout can be 512seconds maximum, using the maximum prescaler, /256, full scale in T3LD. Timer3 is clocked by the internal 32 kHz crystal when operating in the Watchdog mode.

If the timer reaches 0, a reset or an interrupt occurs, depending on bit 1 in T3CON register. To avoid reset or interrupt, any value must be written to T3ICLR before the expiration period. This reloads the counter with T3LD and begins a new timeout period.

As soon watchdog mode is entered, T3LD and T3CON are write-protected. These two registers cannot be modified until are set clears the watchdog enable bit and causes Timer3 to exit Watchdog mode.

CHAPTER 5 EXPERIMENTATION WORK

5.1 Signal Conditioning Results

The designed Signal conditioner circuit is simulated and the simulated result is V0 in millivolts (mV). The developed PCB is checked by comparing the results with simulated results and result is V1 in millivolts (mV).

Following are Simulated results V0 (mV) and Experimental results V1 (mV).

R(Ω)	V0(mV)	V1(mV)
18.5	359.5	132.9
20	366.1	136.9
40	439.5	248.4
60	528	356.1
80	632.4	463.4
100	750.7	567.5
120	879.2	672
135	979.8	752
150	1083	859
170	1222	952
200	1432	1113
240	1714	1332
260	1855	1441
280	1996	1549

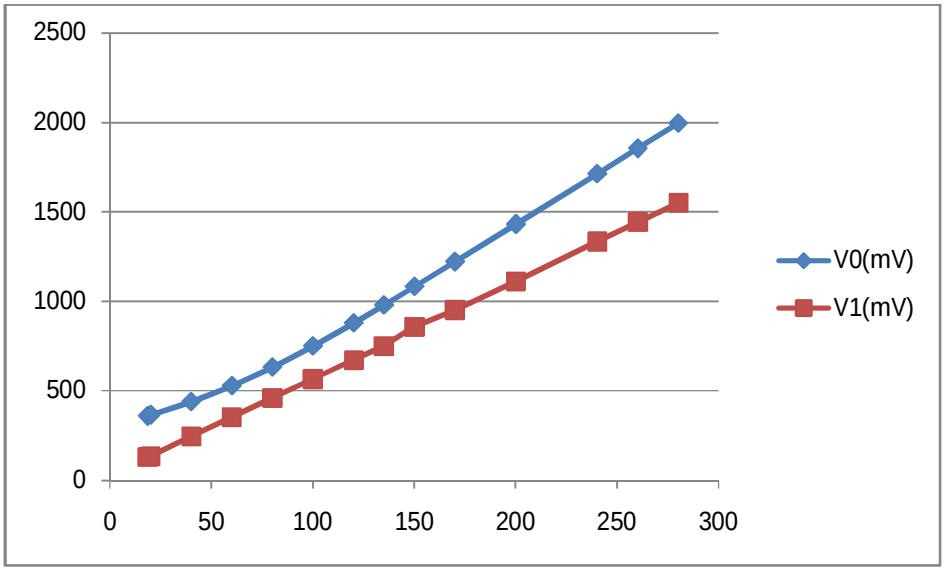


Figure 5. 1: Change in Resistance (RL) Vs signal conditioning output (VO) and practical output (V1)

By comparing the simulation result with the experimental result the graph comes linear with constant linear error value.

The design Signal Conditioning Circuit for RTD is used to sense temperature over the range of 0°C to 300°C, the resistance produced by the RTD would be nominally between 18.5Ω and 285.2Ω, giving a voltage across the RTD between 18.5 mV and 285.2 mV.

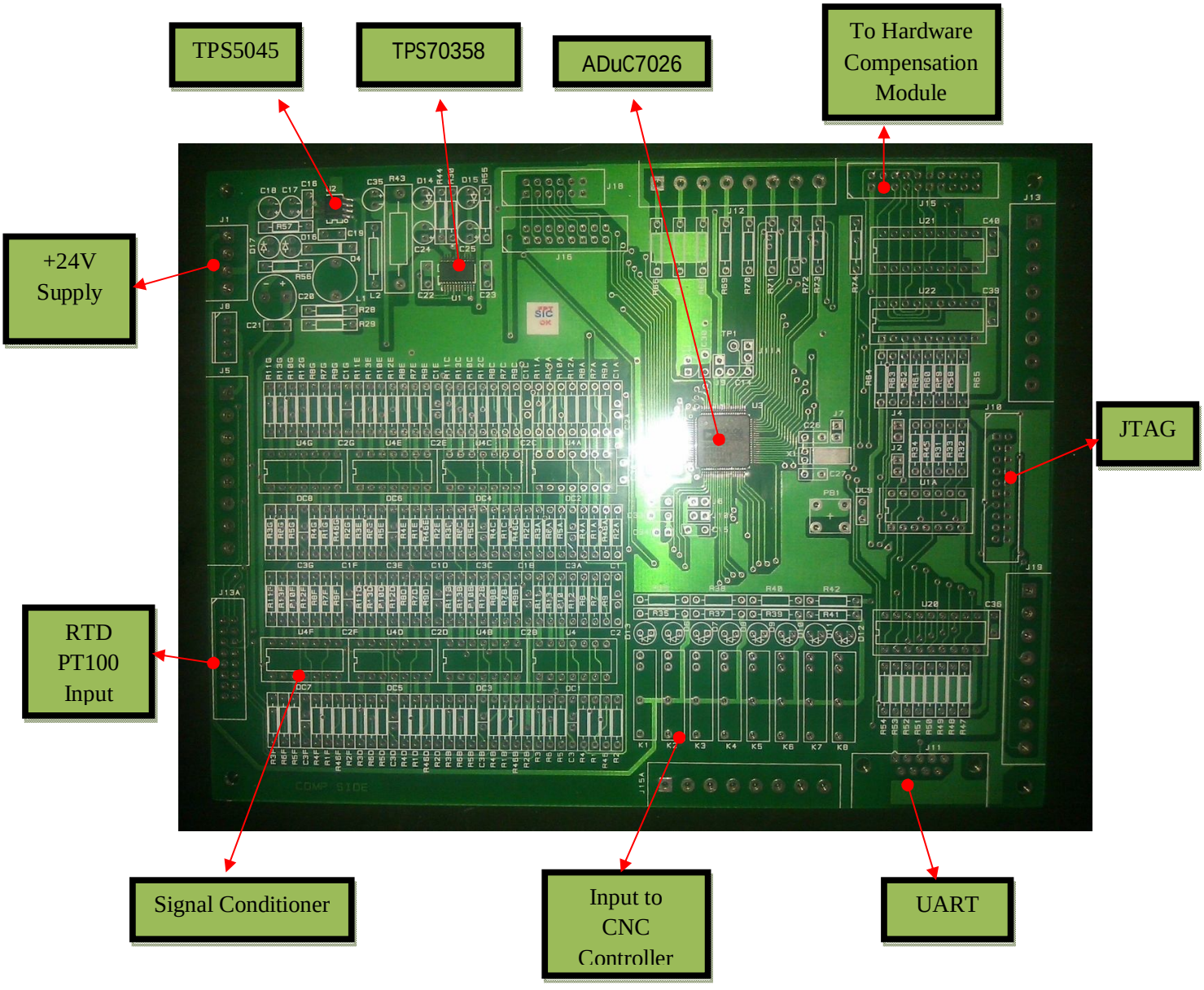
The voltage output of signal conditioner is nominally between 0.1329V and 1.574V, which is less than VREF (2.5V) .The 12-bit A/D converter gives a nominal temperature resolution of 0.129°C/lsb.

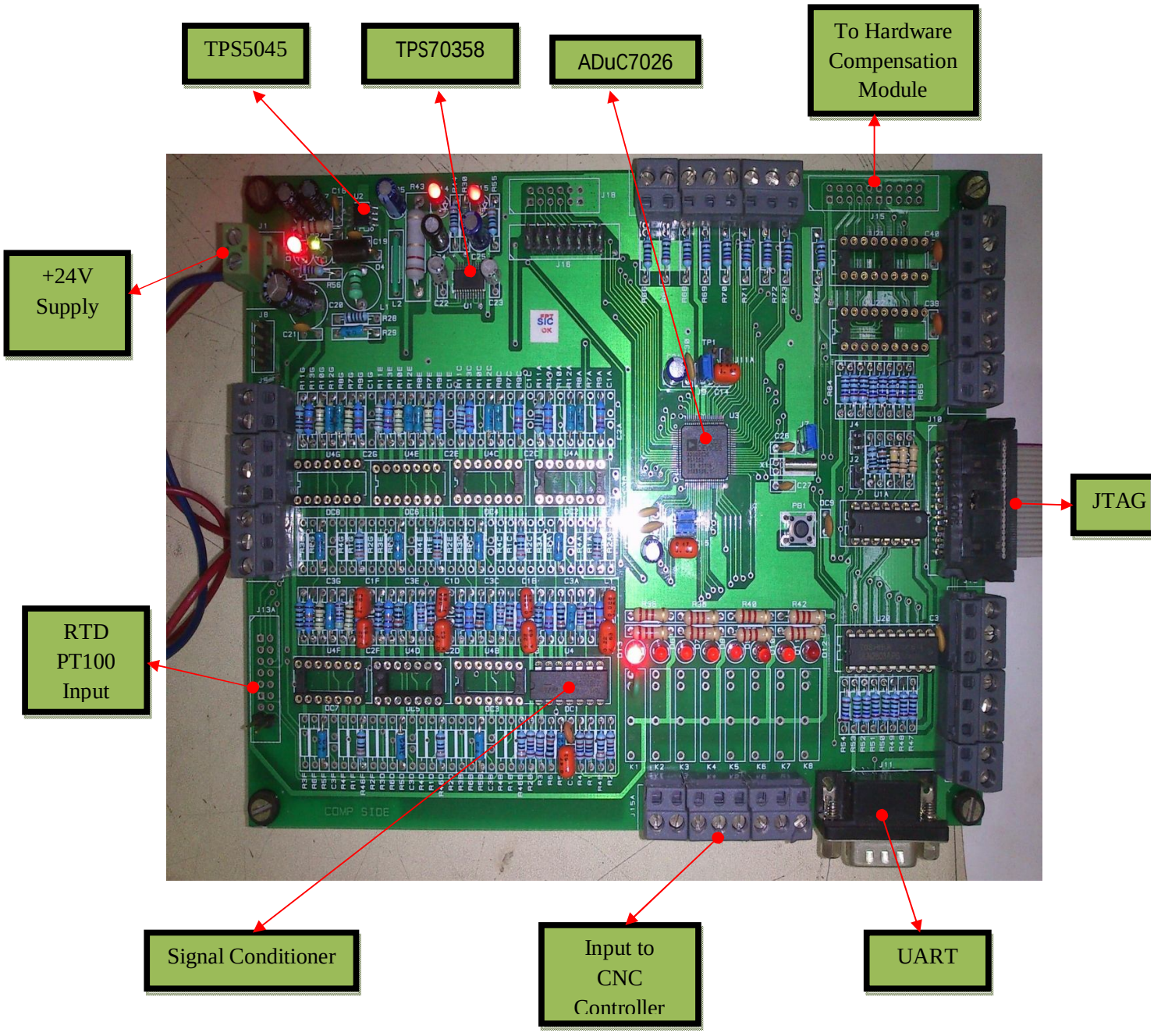
5.2 ANN Simulation Results

X	Z	T1	T2	T3	T4	T5	T6	T7
1.03E+01	-1.17E+01	26.611	23.485	26.682	25.127	27.773	27.282	34.205
1.03E+01	-1.17E+01	26.611	23.485	26.717	25.127	27.79	27.282	34.205
1.03E+01	-1.17E+01	26.611	23.485	26.717	25.127	27.79	27.282	34.222
1.03E+01	-1.16E+01	26.611	23.503	26.753	25.127	27.79	27.282	34.222
1.03E+01	-1.16E+01	26.611	23.503	26.753	25.127	27.825	27.282	34.222
1.03E+01	-1.16E+01	26.629	23.503	26.753	25.127	27.825	27.282	34.238
1.03E+01	-1.16E+01	26.629	23.503	26.806	25.127	27.825	27.282	34.238
1.03E+01	-1.16E+01	26.629	23.503	26.806	25.127	27.843	27.299	34.238
1.03E+01	-1.16E+01	26.646	23.522	26.806	25.127	27.843	27.299	34.238
1.03E+01	-1.16E+01	26.646	23.522	26.841	25.127	27.86	27.299	34.238
1.03E+01	-1.16E+01	26.664	23.522	26.841	25.127	27.86	27.299	34.255
1.03E+01	-1.16E+01	26.664	23.522	26.876	25.145	27.86	27.299	34.255
1.03E+01	-1.16E+01	26.664	23.522	26.876	25.145	27.878	27.299	34.255
1.03E+01	-1.16E+01	26.682	23.522	26.876	25.145	27.878	27.299	34.288
1.03E+01	-1.16E+01	26.682	23.522	26.912	25.145	27.878	27.299	34.288
1.03E+01	-1.16E+01	26.682	23.522	26.912	25.145	27.86	27.317	34.322
1.03E+01	-1.16E+01	26.699	23.54	26.912	25.145	27.86	27.317	34.322
1.03E+01	-1.16E+01	26.699	23.54	26.965	25.145	27.86	27.317	34.322
1.03E+01	-1.16E+01	26.699	23.54	26.965	25.145	27.86	27.317	34.338
1.03E+01	-1.16E+01	26.717	23.559	27.088	25.145	27.86	27.317	34.338

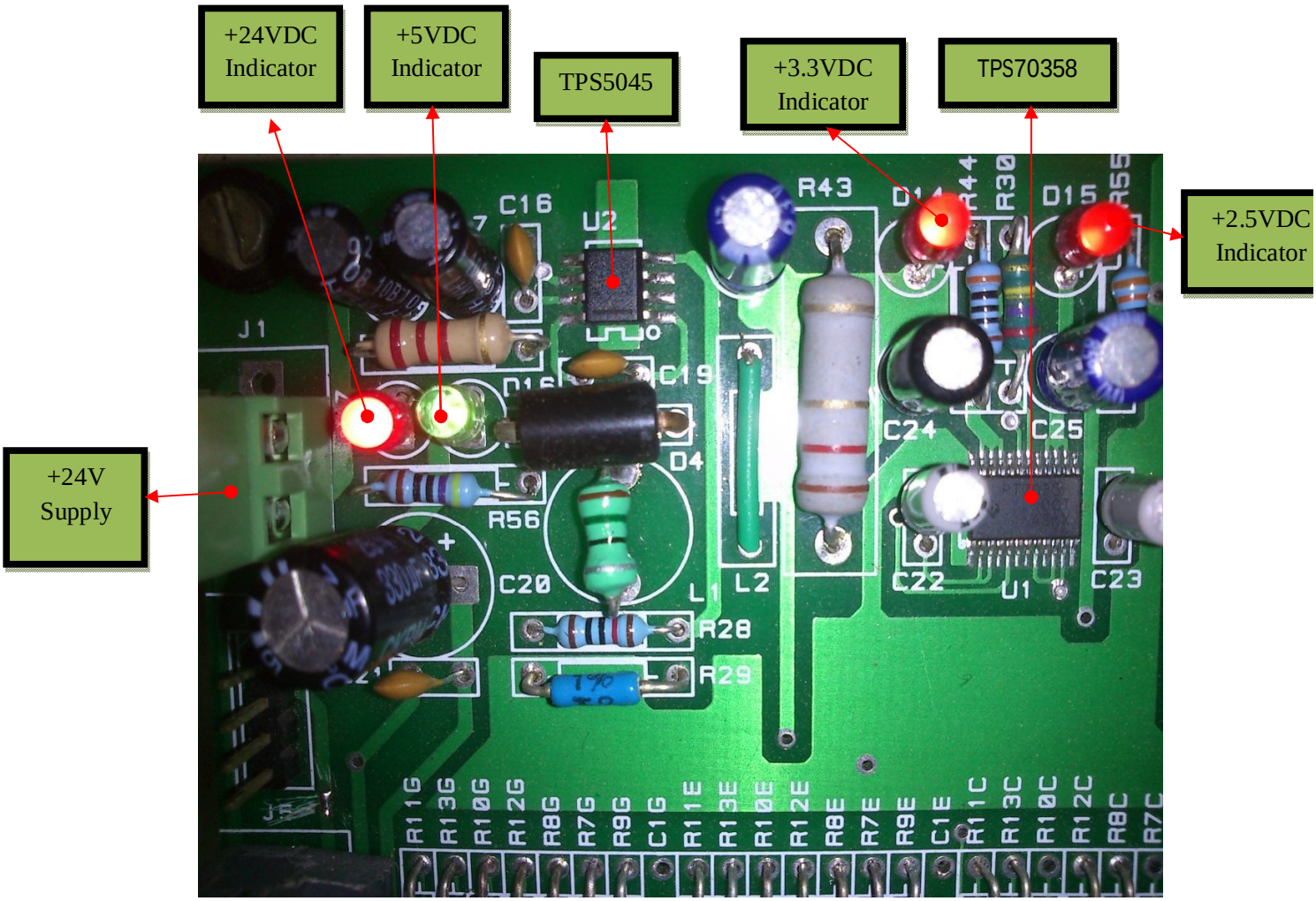
1.03E+01	-1.15E+01	26.717	23.559	27.088	25.145	27.878	27.317	34.338
1.03E+01	-1.15E+01	26.912	23.559	27.088	25.145	27.878	27.334	34.372
1.03E+01	-1.15E+01	26.912	23.559	27.106	25.145	27.878	27.334	34.372
1.03E+01	-1.15E+01	26.912	23.559	27.106	25.235	27.878	27.334	34.372
1.02E+01	-1.15E+01	26.912	23.559	27.106	25.235	27.878	27.334	34.388
1.03E+01	-1.15E+01	26.912	23.577	27.123	25.235	27.878	27.334	34.388
1.03E+01	-1.15E+01	26.912	23.577	27.123	25.235	27.878	27.352	34.421
1.02E+01	-1.15E+01	26.894	23.577	27.123	25.235	27.878	27.352	34.421
1.02E+01	-1.15E+01	26.894	23.577	27.141	25.217	27.878	27.352	34.421
1.02E+01	-1.15E+01	26.894	23.577	27.141	25.217	27.878	27.352	34.421

Printed Circuit Board (PCB):




TPS5045
TPS70358
ADuC7026
To Hardware Compensation Module
+24V Supply
JTAG
RTD PT100 Input
Signal Conditioner
Input to CNC Controller
UART

Power Supply Output:



CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1. Conclusion

A proto-type PCB was manufactured so as to Test the functionality of the designed Hardware. The PCB is assembled and tested for the following functionalities.

- Power Supply module generating 5V DC, 3.3V DC and 2.5V DC supply from 24VDC power supply.
- JTAG Emulator Interface.
- Resistive Temperature Detecting RTD Interface with Signal Conditioning and (PT100) as the sensing element
- UART Communication Interface
- General Purpose Input / Output Interface
- An Interface to Communicate with Computerized Numerical Controller (CNC) with a Relay Logic and so on

The developed PCB Module functionality is

All the above mentioned functionalities are tested and found to be working satisfactorily.

Problem faced on developed the hardware module.

- Due to some problem inductor L1 15 uH was not working may be due to faulty component reason. so the output of TPS5450 was not coming then we change that and we got the required output as 4.987V~5V
- Due to bad shouldering the IC TPS70358 got spoiled and capacitor C25 was grounded and so it was not charging at all. Due to that it was loading the IC TPS5450 and ADuC7026 was getting somewhat heat up.

The solution we were having was to change the IC or to use the new PCB board, we choose second option because we were not having facilities to shoulder SMD IC. On second PCB we got the required output as 2.5V and 3.3V.

- Due to bad code flashing in arm micro-controller, it was showing error as "**could not stop arm device**" while doing flashing for other code.

The problem was solved by full erase chip and the procedure followed was

1. Power off the device.
2. Power on the device while holding the reset button on the target.
3. Start µVision with a STR9 project (and the correct Flash algorithm) and select from the µVision menu **Flash — Erase**.
4. Wait at least 0.5 second, but not more then 1.5 seconds.
5. Release the Reset button on the target.
6. Flash will be erased (with the bad code) and JTAG will be fully functional again.

6.2. Future work

This module will be interfaced with general purpose CNC Controllers for applying Thermal Error Compensation. Currently this module is going to be integrated with iUPTM (Intelligent Ultra Precision diamond Turning Machine) in few months.

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