Assignment (Verilog - 4) (Array)

1) Array is a the collection of homogeneous datatypes. Ex. Array of vectors
Array of integers.

Declaration : datatype [width-1:0] array_name [depth-1:0];

MSB LSB

Ex. reg [15:0] mem [3:0];

has depth = 3-0+1 = 4

height = 15-0+1 = 16

2) Array

→ It is a variable that can hold multiple variables of same type

→ Collection of vectors
One kind of array.

Ex. reg [3:0] mem [3:0];
(→ It is a member 2-D - bit structure)

Vectors

→ It is a variable that can hold multiple bi

→ Collection of scalars = vecto

Ex. reg [3:0] a;

→ It is a register. (multiple bit unidirectional wire

3) reg [7:0] data [15:0]

⇓

means data = array_name.

depth = 15 - 0 + 1 = 16

width = 7 - 0 + 1 = 8

size = 16 × 8 = 128 bits

⇒ In each location/index, 8 bits are stored.

⇒ No. of locations in array = 16.

4) reg [31:0] data [63:0]

array_name = data

size = depth × width

= 64 × 32 = $2^{5+6} = 2^{11}$ = 2048 bits

locations in array = 64

bits in each location = 32

Entire array has = 2048 bits.

5) declaration :

size = 512 bits, each location store = 16 bit (width)

depth = $\frac{512}{16}$ = 32

∴ reg [15:0] mem [31:0];

5 - i) for (i = 0; i < DEPTH; i=i+1) begin

mem[i] = DEPTH'b0;

end

$display ("mem = %p", mem);

ii) for (i = 0; i < DEPTH; i=i+1) begin

if (i == 457) m[i] = DEPTH'hFFFF;

else ~~begin~~ m[i] = DEPTH'h0000;

end

// display it.

6 - same as

7) memory declaration :

reg [WIDTH-1:0] mem [DEPTH-1:0];

8) 16 kb memory = 16 x 1000 bytes.

= 16 x 8 x 1000 bits

= 128000 bits

width = 32.

depth = $\frac{128000}{32}$ = 4000

∴ reg [31:0] mem [3999:0];

9) byte addressed mem of 1KB size.

∴ width = 8.

depth = $\frac{1000 \times 8}{8}$ = 1000

∴ declar = reg [7:0] mem [999:0];

5.(iii) for (i=0; i < DEPTH ; i=i+1) begin

~~if (i >= 100; i <= 200; i=i+~~

if (i > 100 && i < 201)

m[i] = ~~DEPTH~~ $urandom_range(30,500);

else m[i] = DEPTH'h0000;

end