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**FINAL SEMESTER ASSESSMENT (FSA) B.TECH. (CSE)**

**III SEMESTER ‘A’ SECTION**

**UE18CS206 – DIGITAL DESIGN & COMPUTER ORGANIZATION LABORATORY**

**PROJECT REPORT**

**ON**

“DESIGN AND IMPLEMENTATION OF A RING AND JOHNSON COUNTER”

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1. **ABSTRACT OF THE PROJECT**

Two most important types of shift register counters are Johnson counter and Ring counter. These shift register counters with serial outputs are connected to serial inputs to produce particular pattern of sequences. These shift registers are used as counters because of the specified sequence of states.

* **RING COUNTER:-**

Ring counter is a basic application of shift registers. It is formed by the feedback of the output to its own input. This counter has N states where N denotes the number of **flip-flops** in the ring counter.

A 4 bit ring counter consists of 4 D-flipflops, FFA, FFB, FFC and FFD. Each of these D flip-flops has an input D and output Q. At first, a**RESET** signal is applied to the flip-flops to RESET the outputs to zero. Then a **preset** pulse is applied to the flip-flop FFA before the clock pulse is given. This step allows putting the value ‘1’ to the ring counter circuit. When each time the clock pulse is given, the counter circulates the data among all the four flip-flops.  Each output value of this counter has a frequency ¼ th of the main frequency value.

**Advantages**

* Can be implemented using D and JK flip-flops.
* It is a self-decoding circuit.

**Disadvantages**

* Only four of the 15 states are being utilized
* **JOHNSON COUNTER:-**

**Johnson Counter** also known as **Twisted Ring Counter**is another basic application of shift registers with a feedback. Here the feedback is given from the inverted output of the last flip flop to the input of the first flip-flop.Figure below shows a 4-bit Johnson counter. It consists of four flip-flops FF0, FF1, FF2 and FF3. Here the inverted output of the last flip-flop FF3 is given as feedback to the input of the first flip-flop FF0.  Here, at first four logic zeros will be passed to the flip-flops. When clock pulses are given  “1000”, “1100”, “1110”, “1111”, “0111”, “0011”, “0001”, “0000” outputs will be obtained  and the sequence will repeat for the next clock pulses.

**Advantages**

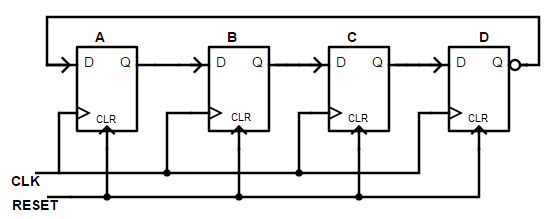
* More outputs than ring counter.

**Disadvantages**

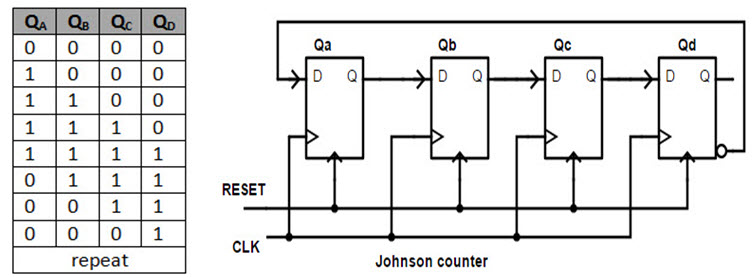
* Only 8 of the 15 states are being used.

**2. CIRCUIT DIAGRAM**

* **RING COUNTER:-**



* **JOHNSON COUNTER:-**



* 1. **MAIN VERILOG CODE**
* **RING COUNTER:-**

module four\_bit\_ring\_counter (

input clock,

input reset,

output [3:0] q

);

reg[3:0] a;

always @(posedge clock)

if (reset)

a = 4'b0001;

else

begin

a <= a>>1; // Notice the blocking assignment

a[3]<=a[0];

end

assign q = a;

endmodule

* **JOHNSON COUNTER:-**

module johnson\_ctr(clk,reset,out);

input clk,reset;

output [3:0] out;

reg [3:0] q;

always @(posedge clk)

begin

if(reset)

q=4'd0;

else

begin

//q[3]<=q[2];

//q[2]<=q[1];

//q[1]<=q[0];

q <= q>>1;

q[3]<=(~q[0]);

end

end

assign out=q;

endmodule

**4. TESTBENCH FILES**

* **RING COUNTER:-**

`timescale 1ns/1ps

module tb();

reg clk\_tb,clr\_tb;

wire [3:0]q\_tb;

ring\_count dut1(q\_tb,clk\_tb,clr\_tb);

initial begin $dumpfile("ringTest.vcd");

$dumpvars(0,tb);

end

initial

begin

$display(“time,\t clk\_tb,\t clr\_tb,\t q\_tb”);

$monitor(“%g,\t %b,\t %b,\t %b”,$time,clk\_tb,clr\_tb,q\_tb);

clr\_tb=1′b0;

#50 clr\_tb=1′b1;

#100 clr\_tb=1′b0;

end

always

begin

#50 clk\_tb=1′b1;

#50 clk\_tb=1′b0;

end

endmodule

* **JOHNSON COUNTER:-**

`timescale 1ns / 1ps

module tb();

reg clock;

reg reset;

wire[3:0] q;

initial begin $dumpfile("JohnTest.vcd"); $dumpvars(0,tb); end

johnson\_ctr r2 (

.clk(clock),

.reset(reset),

.out(q)

);

always #10 clock = ~clock;

initial begin

// Initialize Inputs

clock = 0;

reset = 0;

#5 reset = 1;

#20 reset = 0;

#500 $finish;

end

initial

begin

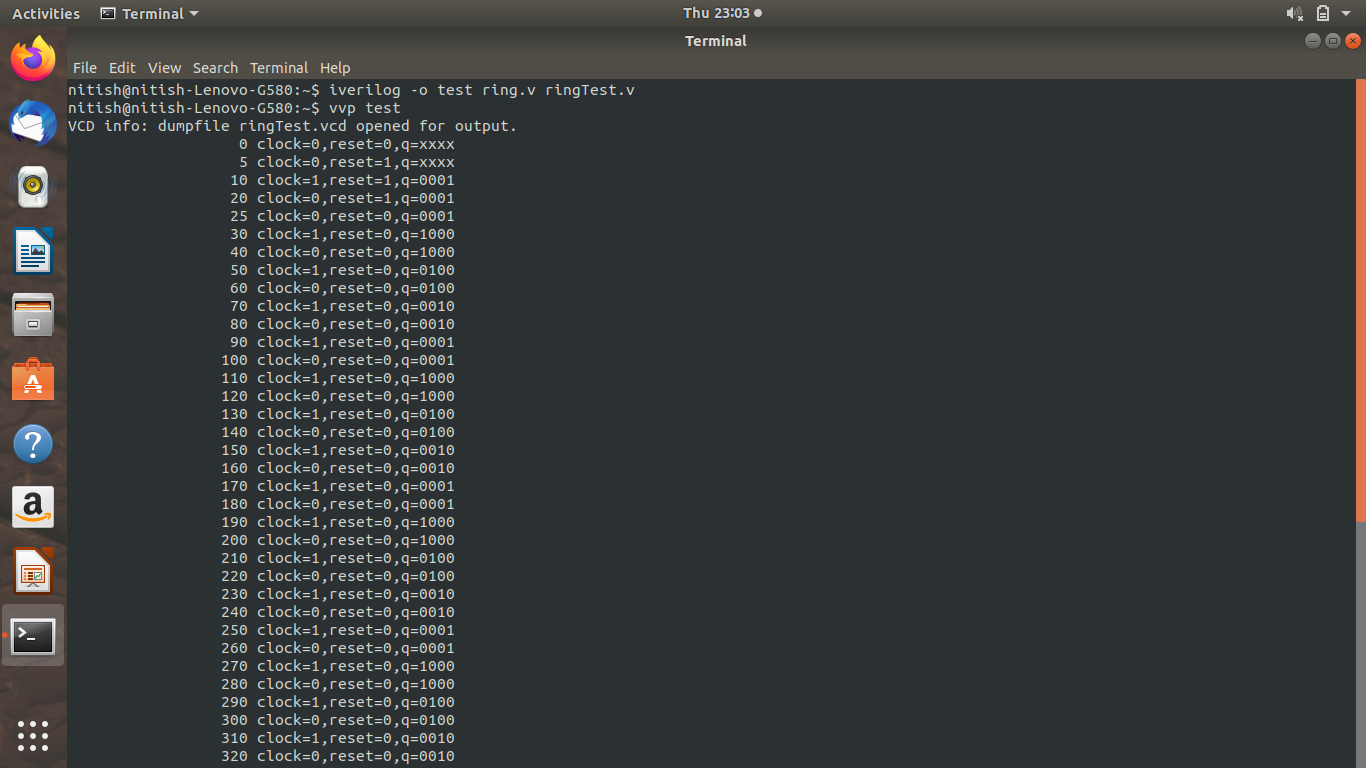
$monitor($time, "clock=%1b,reset=%1b,q=%4b",clock,reset,q);

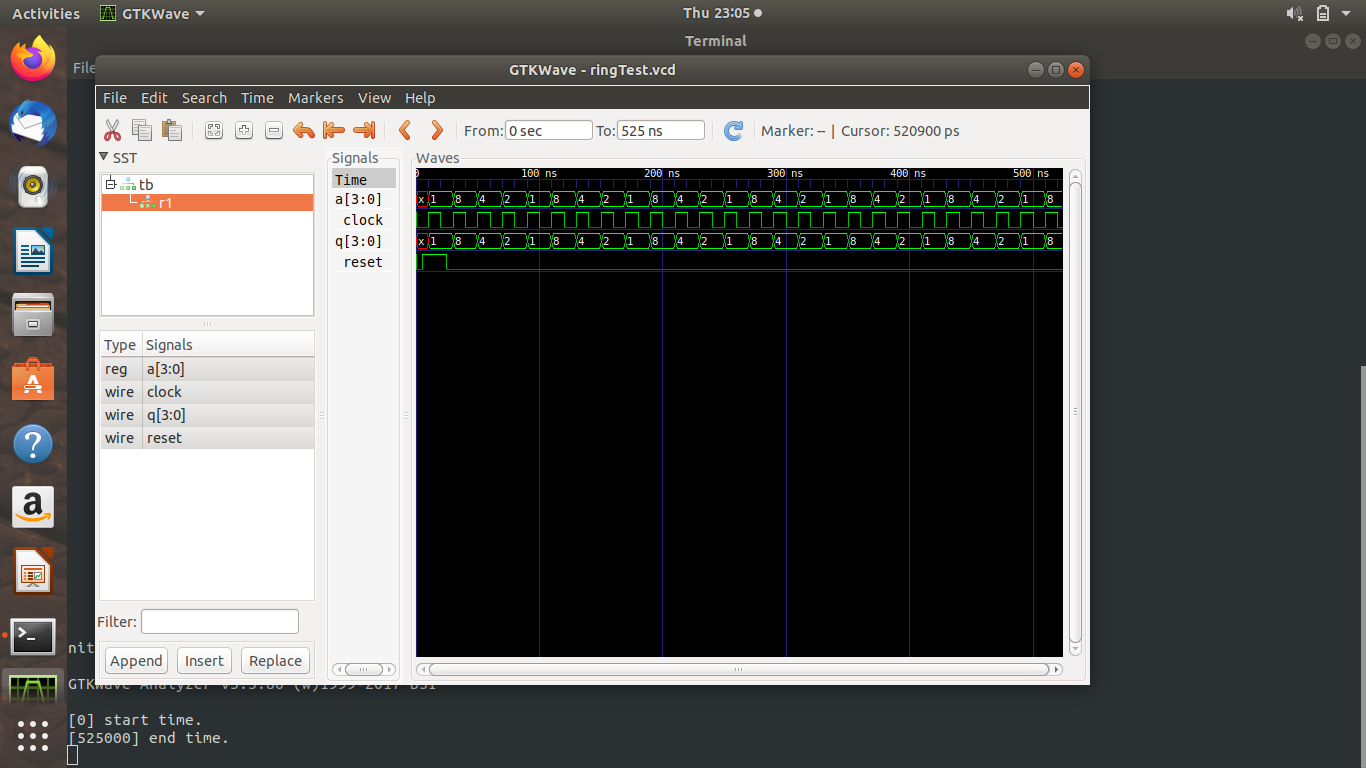
end

endmodule

**5. SCREENSHOTS OF THE OUTPUTS**

* **RING COUNTER:-**





* **JOHNSON COUNTER:-**

